Chapter 15
Coupling of Numerical and Symbolic Techniques for Model Order Reduction in Circuit Design

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Abstract In this paper, we will give a short motivation for the use of symbolic methods for model order reduction and present some of these techniques. Furthermore, we will discuss the hierarchy usually at hand for circuit design and present a workflow for the exploitation of this hierarchy. By applying it to a simple circuit example, we will show how model order reduction (MOR) methods can be profitably employed.

Keywords Model reduction · Symbolic model reduction · Hierarchical model reduction · Coupled symbolic-numerical model reduction · Structure preservation · Structure-exploiting model reduction · Structure-preserving model reduction · Analog circuit · Electrical circuit

15.1 Motivation

First, we will give a motivation for symbolic model order reduction methods (MOR methods) by using the example of the folded-cascode operational amplifier (see also [3]) depicted in Fig. 15.1. The original design showed an instability in the amplifier's small-signal behavior at a frequency of approximately 10 MHz (cf.

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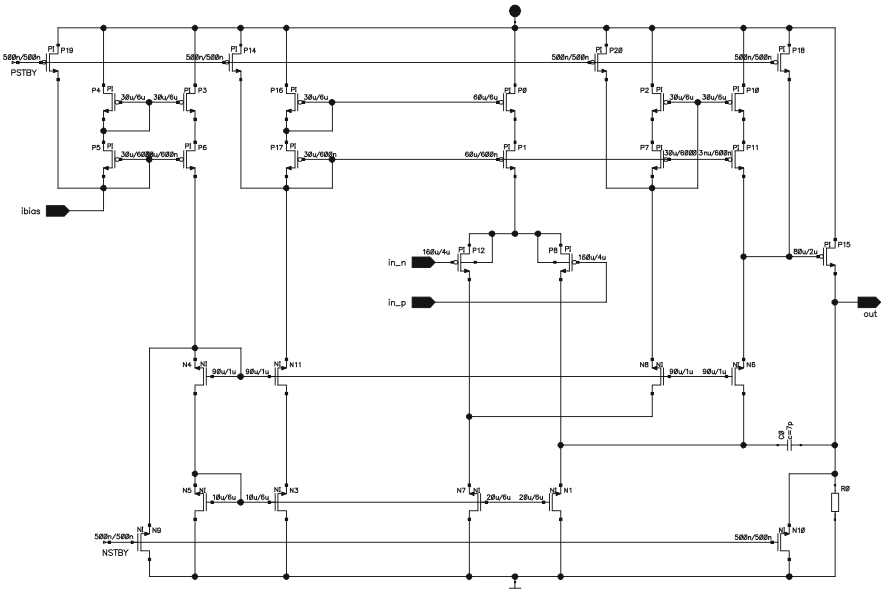

Fig. 15.1 Folded-cascode operational amplifier

Fig. 15.2, solid curves), visible by a resonance peak, which was caused by a pair of complex conjugate parasitic poles.

As a classic approach, one would have performed parameter variations and numerical simulations in a trial-and-error fashion to solve the underlying instability problem. But due to the fairly high number of parameters, this was not feasible here. However, a symbolic analysis of the amplifier allowed a computation of its transfer function. Since the exact symbolic transfer function consisted of more than $5 \cdot 10^{19}$ terms, a symbolic approximation was necessary, that further allowed a derivation of the formula for the dominant pole pair depicted in Fig. 15.3.

By interpretation of this formula, one detected that one of the circuit's components—a Gate-Source capacitance—had dominant influence with respect to the unstable behavior. By adding an additional capacitance, the original capacitance value could be modified such that the resonance could be damped (cf. frequency analysis in Fig. 15.2, dashed curves) and a stable behavior after a redesign of the amplifier was obtained (cf. transient analysis in Fig. 15.4, dotted curve).

It should be mentioned here that in this case symbolic MOR was used to improve the original design of the circuit and not the reduced model itself.

15.2 Symbolic Techniques

What in particular does nonlinear symbolic analysis aim for? Usually we start at a netlist description that is translated into an equation system (*differential-algebraic*

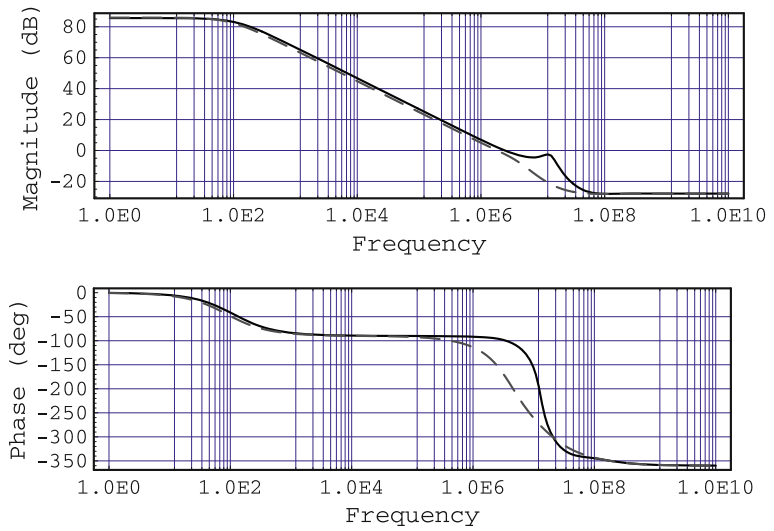

Fig. 15.2 The amplifier's transfer function: original (*solid*) and with an additional capacitance (*dashed*)

$$s_p^{1,2} == -\frac{(CC0 + CL)\ gm\$MN6}{2CC0CL} \pm \frac{\sqrt{Cgs\$MP15gm\$MN6\ (Cgs\$MP15\ (CC0 + CL)^2\ gm\$MN6 - 4CC0^2\ CLgm\$MP15)}}{2CC0Cgs\$MP15CL}$$

Fig. 15.3 Approximated formula for the dominant pole pair of the amplifier's transfer function

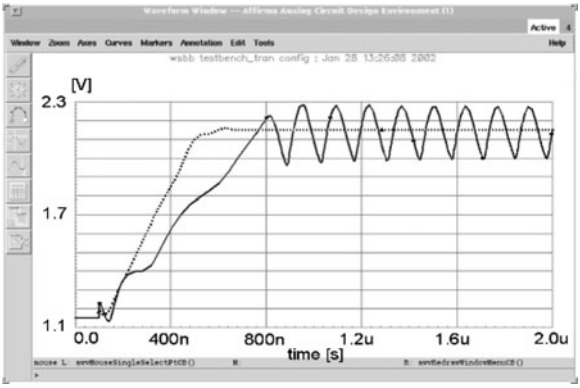

Fig. 15.4 Stable behavior (*dotted*) after redesign of the originally unstable behavior (*solid*)

equations, DAE) via standard graph theoretical methods like *modified nodal analysis* (MNA) or *sparse tableau analysis* (STA) (see e.g. [13]). Based on a *reference solution* of the original system, we can symbolically reduce it to a *simpler* form with less equations, less terms, less derivatives, and so on [14]. This simpler form represents a behavioral model for the original system, which can also be translated into a hardware description language (HDL) and then simulated using a circuit simulator.

The general workflow is as follows (see [11, 14]); according to a numerical analysis $A \in \{\text{AC analysis, DC analysis, transient analysis}\}$ and an input u we have a reference solution v_F for the output v of the original DAE system F, as well as a user-given error bound ε and an error function E to compute the actual error. This reference solution v_F is given by pairs of sampling points and interpolation values, hence the accuracy in comparison to the exact mathematical solution v depends on the numerical solver's choice of the step size. The complexity of F is reduced by iteratively applying reduction techniques R and comparing the (numerical) solution v_G of the so far reduced system G to the reference solution v_F. As long as the error is within the given bound, the performed reduction step is allowed, otherwise it is rejected.

In the following, four symbolic techniques will be explained [14]. They are implemented in *Analog Insydes* [18], an add-on for *Mathematica* [17]. Analog Insydes is developed by Fraunhofer ITWM in Kaiserslautern, Germany.

15.2.1 Algebraic Manipulations

The first symbolic reduction technique we want to present is a purely algebraic manipulation. Here, certain variables are eliminated and substituted in the remaining set of equations. Additionally, independent blocks of equations are removed, e.g.:

$$F: \left.\begin{array}{c} \cdots \\ y = f(x) \\ 0 = g(x,y) \\ \cdots \end{array}\right\} \Rightarrow \left\{\begin{array}{c} \cdots \\ 0 = g(x,f(x)) \\ \cdots \end{array}\right. : G$$

Obviously, this method is mathematically exact. Despite this, we have to be careful, since applying this method may lead to equations including a huge number of terms.

15.2.2 Branch Reductions

Using branch reductions, unused branches of piecewise-defined functions are detected and removed. Piecewise-defined functions occur, e.g., in the device model equations of transistors or diodes. Usually these components only work in a certain operating region that is contained, e.g., in the interval $[a, b]$, then branch reductions are possible:

$$f(x) = \begin{cases} f_1(x) & x < a \\ f_2(x) & a \le x \le b \\ f_3(x) & x > b \end{cases} \quad \Rightarrow f(x) = f_2(x) \text{ for all } x.$$

Here, f is to be considered as a function that is contained in at least one term in at least one of the equations of the DAE system F.

15.2.3 Term Substitutions

Here, an equation, which typically consists of a sum of products,[1] is considered, where certain terms are replaced by appropriate constant values, e.g. adequate average values. This technique can also be applied to different levels, e.g. when some of the summands are functions and their arguments themselves contain sums, and so on.

In the following example, the jth equation F_j in the equation system F is a sum of terms t_i, where the kth term t_k will be replaced by the constant κ:

$$F_j : \sum_{i=1}^{N} t_i(x) = 0 \Rightarrow G_j : \sum_{i=1, i\neq k}^{N} t_i(\widetilde{x}) + \kappa = 0.$$

This method obviously is not an exact one, since it alters the solution x of the original equation system. The solution of the approximated system is denoted by $\widetilde{x}$.

15.2.4 Term Reductions

This technique is a special case of term substitutions, since certain terms are replaced by zero, which means that they are cancelled:

$$F_j : \sum_{i=1}^{N} t_i(x) = 0 \Rightarrow G_j : \sum_{i=1, i\neq k}^{N} t_i(\widetilde{x}) = 0.$$

Concerning all the above techniques, we consider that as long as the error that is caused by applying these methods is within the user-given error bound, the corresponding reductions are valid.

15.3 Hierarchical Systems

Within the last few years the growing miniaturization of integrated circuits and increasing integration density of circuit components have led to nanoelectronic structures. It turns out that physical effects like thermic or electro-magnetic interactions cannot be neglected anymore. One also observes a very fast growing number of parameters for the device models for a single transistor within the last

[1] In MNA contributions of components to the system typically are of the form $A^T \cdot f(Bx)$, where A and B are incidence matrices describing the circuit topology and f is a function describing the behavior of the corresponding component. The same expression holds for submodels.

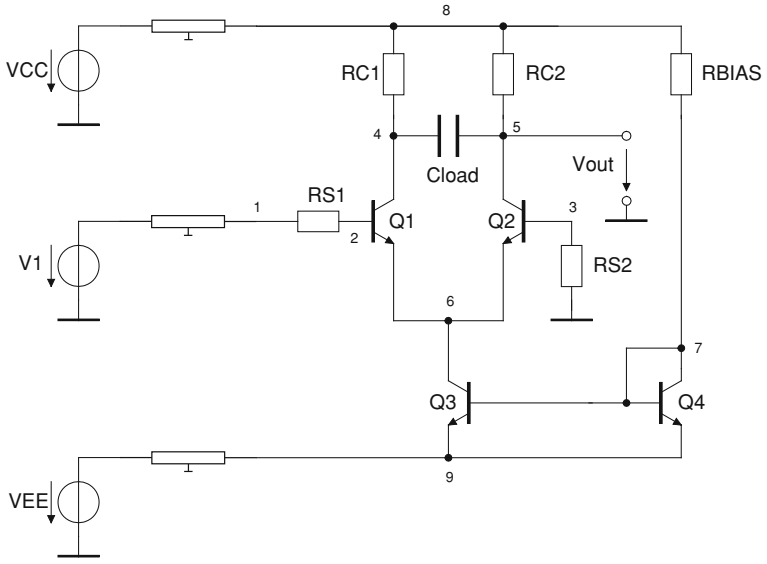

Fig. 15.5 Differential-amplifier circuit

years. This forces the usage of model descriptions based on *partial differential equations* (PDE) besides the netlist based models or those based on DAEs, especially for the semi-conductor components. Hence, one has to cope with *partial differential-algebraic equations* (PDAE), coupled systems of DAEs and PDEs.

Moreover, the circuit usually is hierarchical, as we have various subsystems coupled by a topology. Due to their respective accuracies, these subsystems have different mathematical descriptions. By using standard graph theoretical methods like MNA or STA (see [13]) to build up the describing equation system, this hierarchy is lost. So our goal is the exploitation of the circuit's hierarchical structure.

As an example, let us consider the differential-amplifier circuit depicted in Fig. 15.5. The voltage sources VCC and VEE denote the voltage supply for the amplifier circuit, whereas the voltage source V1 defines the input. The output is defined as the voltage-potential of node 5, denoted by Vout. The three sources are connected to the remaining circuit components via three transmission lines, for which we will use a discretized PDE model of the telegraph or transmission line equations with 20 line segments each (see e.g. [7] or [8], Chaps. 6 and 5).

15.3.1 Symbolic Reduction of the Entire Circuit

If we use MNA in node voltage formulation to set up the describing equation system for the transient circuit behavior, we obtain 167 equations with a total

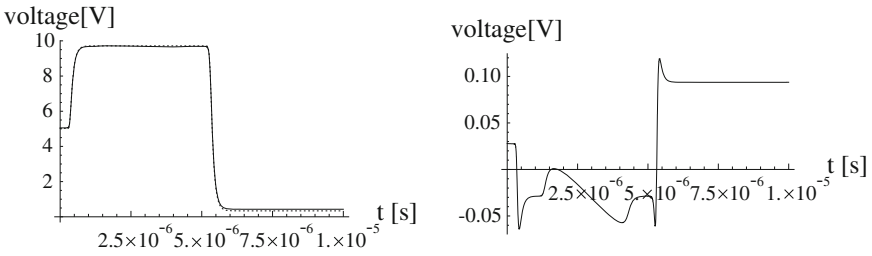

Fig. 15.6 *Left:* Solutions of the original system (*solid*) and the reduced system (*dotted*) allowing 2% error. *Right:* The corresponding error plot

number of 645 terms. For the input V1, we chose a sine-wave voltage excitation with a magnitude of 2 V and a frequency of 10^5 Hz. The supply voltages VCC and VEE are 12 V and −12 V, respectively. By using the symbolic reduction techniques presented in Sect. 15.2 and permitting an error of 2%[2] for the output Vout to reduce the entire system, we obtain a system consisting of 124 equations with 425 terms in total. For the reduction, a few hours are needed,[3] in which more than 95% of that time is spent for the computation of the transient ranking[4] (see e.g. [4, 14, 15]). Figure 15.6 shows the solution and the error of this reduced system in comparison to the solution of the original system.

According to these figures, our reduced system with only about 1% error is a very accurate approximation.

If we allow an error of 10% for the reduction of the original system, we only obtain 44 equations and a total of 284 terms. The time needed is almost the same because of the ranking computation mentioned above. However, the reduced equation complexity has been achieved at the expense of accuracy (cf. Fig. 15.7).

15.3.2 Exploitation of the Hierarchical Structure

What will happen, if we take an 'intuitive' hierarchy into account? Therefore consider certain structural patterns in the circuit's netlist: the differential pair of transistors (together with some resistors) in the upper box on the right side of Fig. 15.8, a current mirror in the lower right, three transmission lines in the middle, and the sources on the left.

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[2] x% error here means $\frac{x}{100}$ of the maximum magnitude of the reference solution, considered on the entire time interval: $\frac{x}{100} \cdot \sup_{t\in[t_0,t_1]} ||v_F(t)||_\infty$.

[3] The computations were executed on a Dual Quad Xeon E5420 with 2.5 MHz and 16 GB RAM.

[4] A ranking is a trade-off between accuracy and efficiency in computation time that estimates the influence of a term in the equation system on the system's solution.

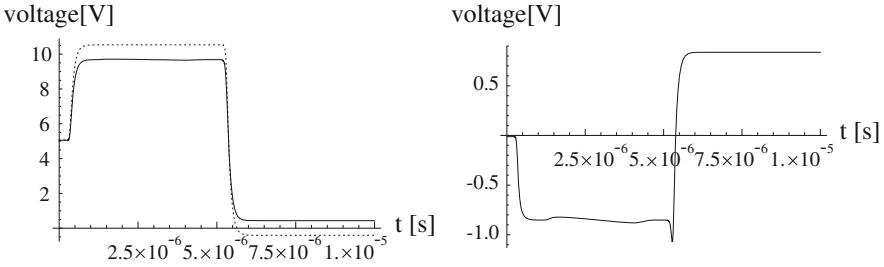

Fig. 15.7 *Left:* Solutions of the original system (*solid*) and the reduced system (*dotted*) allowing 10% error. *Right:* The corresponding error plot

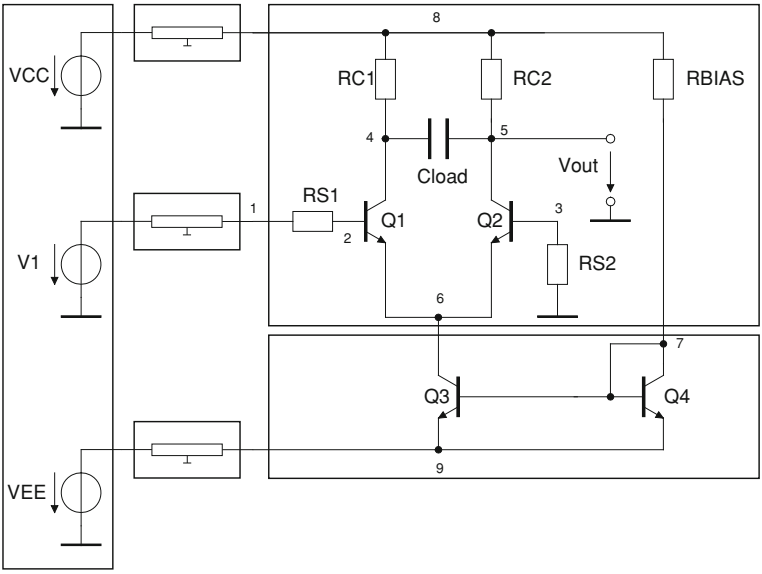

Fig. 15.8 Differential-amplifier circuit with its 'intuitive' hierarchy

As said before, by using e.g. MNA to set up the describing equation system for the entire circuit, the hierarchy information is lost, since the system contains equations with mixed parts from different subsystems. But if we consider the five subsystems one by one, we can transmit the hierarchy information into the describing set of equations and reduce them separately.

For the reduction of the three transmission lines, we translate the describing linear equation system into its state space form and apply Arnoldi's algorithm (see e.g. [5] or [1], Chaps. 10 and 11), a numerical approximation method based on projections on an appropriate Krylov space. For both the transmission lines that are connected to the voltage supplies VCC and VEE we iterate only one step,[5] for the

[5] One step provides sufficient accuracy here, since the sources are DC voltage sources.

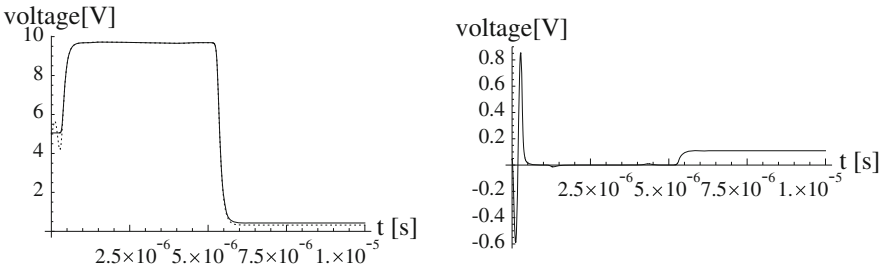

Fig. 15.9 *Left:* Solutions of the hierarchically reduced system (*dotted*) and the original system (*solid*) by applying the 3-step Arnoldi iteration to the input voltage transmission line. *Right:* The corresponding error plot

one connected to the input voltage V1 we perform three steps in the Arnoldi iteration.[6] Due to two additional equations and variables for internal port modeling, we thus can reduce the transmission line subsystems from 50 down to 8 resp. 4 equations.

The current mirror and the differential pair subsystems are reduced symbolically by using the presented techniques from Sect. 15.2. An exact description of how this is done is given in Sect. 15.4. In case of the current mirror subsystem, the symbolic simplification yields 9 instead of 16 equations with a total number of 20 instead of 59 terms. For the subsystem with the differential pair, we obtain a reduced system with 13 instead of 22 equations and 50 instead of 91 terms in total. For both of these reductions a 2% error bound[7] is permitted, but we observe almost no further reductions, if we allow 10% error instead. Note that all of the reductions mentioned above are computed within seconds. How these reduction steps—particularly in the symbolic case—can be carried out will be explained in the next section.

If we now plug together all the reduced subsystems to obtain a reduced form of the entire differential-amplifier circuit, the results are very accurate as one can see in Fig. 15.9. Instead of 167 equations and a total number of 645 terms, we only have 62 equations with 252 terms altogether. The error of the entire system compared to the original one is approximately 8%.

A higher dimensional projection space obtained by the Arnoldi iteration provides more accurate solutions, but of course also leads to a larger system. If, for example, we perform five iteration steps in the Arnoldi algorithm to reduce the transmission line that is connected to the input voltage V1 instead of only three, we can further improve our results and obtain a maximum error of the entire reduced

[6] We performed some experiments with a higher number of iteration steps, but the gain of additional accuracy in comparison to the size of the larger system was rather marginal for a number of iteration steps bigger than five.

[7] As we are reducing only the single subsystem, this error bound is not limiting the error of the entire circuit's output `Vout` to the given values (see Sect. 15.4 and Algorithm 1 for further details).

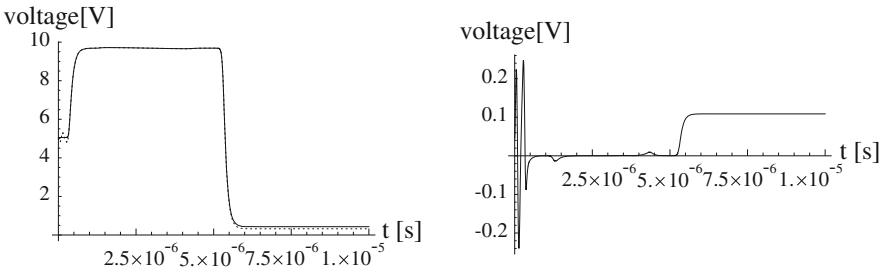

Fig. 15.10 *Left:* Solutions of the hierarchically reduced system (*dotted*) and the original system (*solid*) by applying the 5-step Arnoldi iteration to the input voltage transmission line. *Right:* The corresponding error plot

system of approximately 2% (Fig. 15.10). But then the reduced entire system consists of 66 equations and a total number of 396 terms.

15.3.3 Using the Reduced Model with Other Inputs

To check whether the reduced model obtained with our hierarchical approach works fine also for other inputs, we apply a pulse wave with a magnitude of 2 V, a sum of three pulses with magnitudes of 1, 2, and 3 V, respectively, and a sum of three sine functions

$$f(t) := 2 \cdot \sin(2\pi \cdot 10^5 \cdot t) + 2 \cdot \sin(2\pi \cdot 2 \cdot 10^5 \cdot t) + 1 \cdot \sin(2\pi \cdot 5 \cdot 10^5 \cdot t)$$

to V1. The graphs of these functions are shown in Fig. 15.11 on the time interval $I = [0\ \text{s}, 10^{-5}\ \text{s}]$.

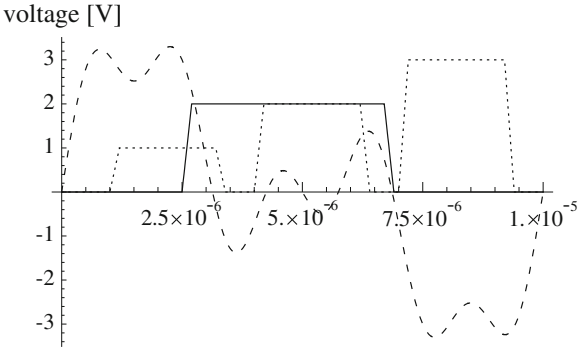

Fig. 15.11 Three other inputs `V1` to test the reduced model of the differential-amplifier circuit

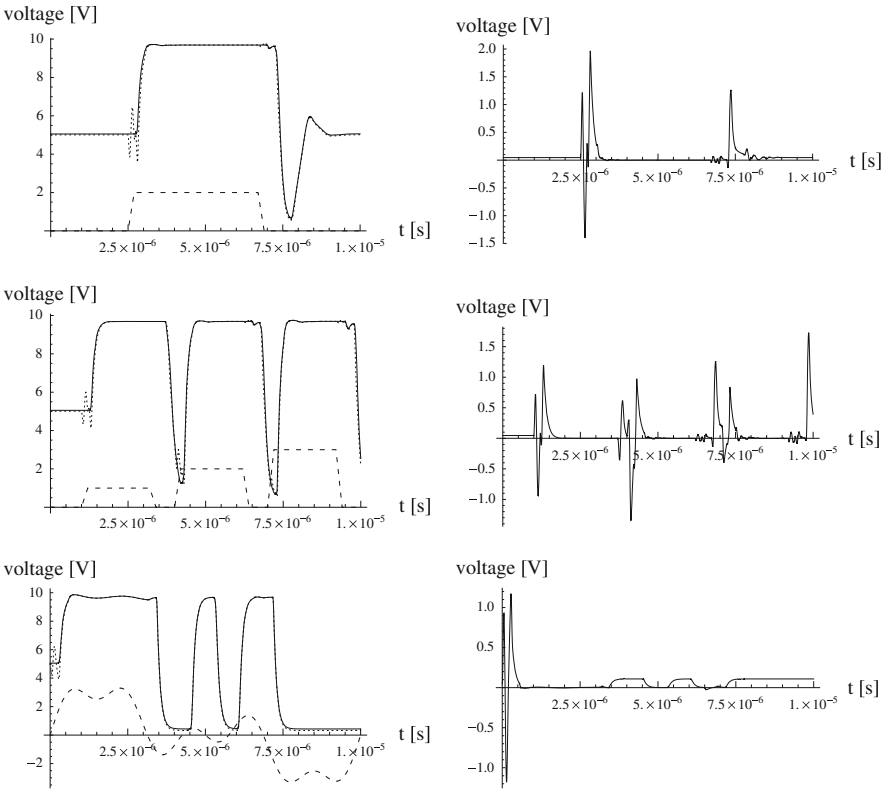

Fig. 15.12 *Left:* Simulation results of the original (*solid*) and the hierarchically reduced model (*dotted*), together with the corresponding input `V1` (*dashed*). *Right:* The corresponding error plots

With these inputs, both the original differential-amplifier and our hierarchically reduced model[8] are simulated. The graphs of the simulations as well as the corresponding error plots are shown in Fig. 15.12.

According to these figures, the obtained model works quite well in all the test cases and therefore can be used as a behavioral model of the original differential amplifier in a certain domain.

15.3.4 Comparison of both Approaches

The results of the two different reduction approaches for the differential-amplifier circuit are listed in Table 15.1.

[8] We chose the more accurate model with 66 equations, see Fig. 15.10.

Table 15.1 Results of the two different reduction approaches for the differential-amplifier circuit

	Orig. system	Reduction of entire circuit		Reduction exploiting hierarchy	
Equations	167	124	44	66	62
Terms	645	425	284	396	252
(Permitted) error		2%	10%	~2%	~8%
Arnoldi iterations				(5/1)	(3/1)
Computation time		Few hours	Few hours	Within seconds	Within seconds

Comparing both approaches, we conclude that the one that exploits the hierarchical structure is the better choice, since it delivers much better results in less computation time; we obtained reduced systems with almost the same accuracy in the 2% error case, but only about half the number of equations. Performing only three steps in the Arnoldi iteration to reduce the transmission line connected to the input voltage V1, we still received a reduced overall system that fit the original (reference) solution quite well. On the other hand, the reduction of the whole circuit permitting an error of 10% led to a system that fully exploits the error bound.

15.4 Workflow for the Exploitation of the Hierarchy

Now we come to the workflow for the reduction of the particularly symbolic subsystems of the entire circuit. It is schematically shown in Fig. 15.13.

From the hierarchical segmentation, we have a set of interacting subsystems. Since we always need a reference solution to symbolically reduce a system, we need a 'closed circuit'. If we simply cut out a subsystem from its connecting structure, we will have no defined input/output behavior at its ports, i.e. we have no information about its current-voltage relation. However, the following algorithm provides a possibility for reducing such a subsystem (see also Fig. 15.13).

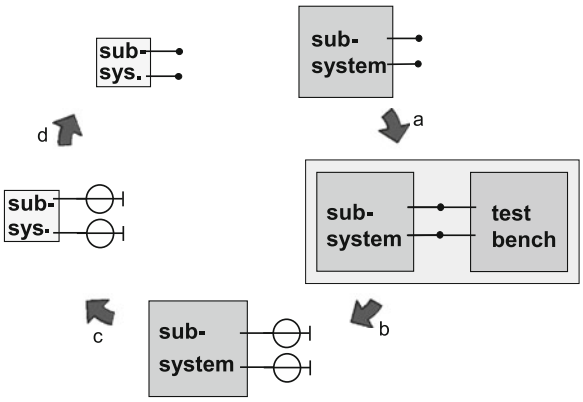

Fig. 15.13 Illustration of the workflow for the symbolic reduction of circuit subsystems

Algorithm 1 (Reduction of subsystems)

(a) connect the subsystem to a test bench[9] and record the voltages[10] at its ports
(b) remove the test bench and plug voltage sources to the subsystem's ports that deliver exactly the recorded voltages (as a data-based function) thus having the subsystems isolated
(c) now the closed circuit can be reduced[11] with appropriate (numerical or) symbolic methods presented in Sect. 15.2
(d) remove all the above sources after the reduction of the subsystem and finally obtain a reduced subsystem that serves as a behavioral model

This workflow has been applied to the subsystems of the differential-amplifier example and delivered the results described at the end of the previous section.

It should be mentioned here that this approach only controls the errors at the ports of the single subsystems. Thus, one cannot pose a statement about or guarantee a certain global error, i.e. the error on the output of the entire (reduced) circuit when replacing the original subsystems by the reduced ones. This could possibly be a point of future investigation (see also Sect. 15.6).

15.5 Comparison to Other Approaches

In [9], LTI coupled control systems are considered, which are coupled by input/output-relations. Moment matching approximation and balanced truncation, two numerical MOR methods, are used to reduce the order of the closed-loop systems. Moreover, structure-preserving model reduction approaches using balanced truncation or Krylov subspaces are presented and some error bounds are given. The internal inputs of the LTI subsystems are given by a linear combination of the other subsystem's internal outputs and the external input, the external output is a linear combination of all internal outputs of the subsystems.

In contrast, in this paper we are dealing with *nonlinear hierarchical* systems which are much less studied, but of great importance. We do not consider an approach that is based on inputs and outputs for the coupling of subsystems as adequate to model an electronic circuit, since the subsystems are *mutually* interacting with each other. Hence, we did not try to extend these approaches.

In [16], however, the author uses "variable sharing" and relations on system variables for modeling the behavior of the variables on the subsystems' external terminals to capture physical phenomena. This approach is applicable not only to

[9] A test bench is a simulation test environment. Here, one could take all the rest of the entire circuit as test bench.

[10] Of course, one could record the currents as well.

[11] By providing the *voltages* at all k ports, they work as the input to the subsystem. Then the *currents* flowing into the subsystem at the k ports are defined as the output and will be controlled by the specified error bound.

electronic circuits, but also to other systems. For example, in a hydraulic system, if two pipes are connected with each other, their pressure variables at the link are equalized while the sum of their flow variables is zero.[12] Thus the variables at the link are shared. Also in our opinion, this approach is appropriate to capture all relevant physical effects of the interacting subsystems, while viewing interconnections as output-to-input assignments introduces a signal transmission mechanism that is not part of the physics of an electronic circuit.

In our paper, we use a similar approach and, in addition, provide a sophisticated model reduction method for hierarchically structured nonlinear systems.

Of course there already exist some methods like POD for *nonlinear* model order reduction. However, we could not find any other approaches for nonlinear model order reduction techniques that explicitly exploit the hierarchy of the overall system. We found some other structure-preserving approaches [2, 6, 12], but these were applied only to *linear* systems. They are based on Krylov space approximations with a certain shape of the projecting matrices to preserve the structure of the original system in its reduced equivalent.

15.6 Summary and Future Work

In this paper, we considered two different approaches for the reduction of a differential-amplifier circuit. The first one reduced the entire circuit using methods as presented in Sect. 15.2 (cf. also [3, 14]). The second approach, introduced in this paper, exploits the circuit's hierarchy. Here we reduce the subsystems separately, then plug the reduced ones together, and thus obtain a reduced overall system.

The new hierarchy-exploiting approach turned out to be the better choice, since we obtained much better results with respect to computation time. Moreover, the accuracy was almost the same, but the number of equations could be halved.

The principal idea is to reduce the subsystems separately (either symbolically or numerically), each one allowing a certain approximation error ε_k. If we plug together the reduced subsystems, we obtain an approximation for the entire system with a certain error ε compared to the original overall system. If the total error ε or the degree of reduction appears not to be satisfactory, we restart the reduction of at least one appropriate subsystem with an altered error bound ε_k More details can be found in [10].

One goal of possible future investigation could be finding a functional relation between the errors ε_k and the error ε of the entire system. The challenge, probably realistic only for special systems, would be obtaining an estimate for the subsystem errors as function of the user-specified error ε.

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[12] The respective flows are directed towards the interior of each pipe.

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