Chapter 12
On Synthesis of Reduced Order Models

Roxana Ionutiu and Joost Rommes

Abstract A framework for model reduction and synthesis is presented, which enables the re-use of reduced order models in circuit simulation. Two synthesis techniques are considered for obtaining the circuit representation (netlist) of the reduced model: (1) by means of realizing the reduced transfer function and (2) by unstamping the reduced system matrices. For both methods, advantages and limitations are discussed. Especially when model reduction exploits structure preservation, we show that using the model as a current-driven element is possible, and allows for synthesis without controlled sources. The presented framework serves as a basis for reduction of large parasitic R/RC/RCL networks.

Keywords Circuit synthesis · Reduced models · Metlist representation · Passivity · Terminals · Impedance · Modified model analysis

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R. Ionutiu (✉)
Department of Mathematics and Computer Science, Eindhoven University of Technology, P.O. Box 513, 5600 MB Eindhoven, The Netherlands
e-mail: r.ionutiu@tue.nl

J. Rommes
NXP Semiconductors, HTC46-2.08, 5656 AE Eindhoven, The Netherlands
e-mail: joost.rommes@nxp.com

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12.1 Introduction

The main motivation for this chapter comes from the need for a general framework for the (re)use of reduced order models in circuit simulation. Although many model order reduction methods have been developed and evolved since the 1990s (see for instance [1] for an overview), it is usually less clear how to use these methods efficiently in industrial practice, e.g., in a circuit simulator. One reason can be that the reduced order model does not satisfy certain physical properties, for instance, it may not be stable or passive while the original system is. Failing to preserve these properties is typically inherent to the reduced order method used (or its implementation). Passivity (and stability implicitly) can nowadays be preserved via several methods [2, 10, 16, 19, 21, 26, 27], but none address the practical aspect of (re)using the reduced order models with circuit simulation software (e.g., SPICE [9]). This brings forward another reason of concern within the circuit simulation industry. The linear circuit to be reduced is represented by a *netlist*, which is a description of the circuit element values (R, L, C) and their connections to the circuit nodes (see also Fig. 12.1). However, reduced order models (as a result of model reduction applied on the dynamical system describing the original circuit) are usually represented in terms of *system matrices* or of the *input–output transfer function*. Typically, circuit simulators are not prepared for inputs in a mathematical representation, and would require additional software architecture to handle them. In contrast, a reduced model in *netlist* representation could be easily coupled to bigger systems and directly simulated.

Synthesis is the realization step needed to map the reduced order model from the mathematical representation (in terms of system matrices or transfer function) into a netlist consisting of electrical circuit components [13]. In [7] it was shown that passive systems (with positive real transfer functions) can be synthesized with positive R, L, C elements and transformers (see also [23]). Later developments [6] propose a method to circumvent the introduction of transformers, however the resulting realization is non-minimal (i.e., the number of electrical components generated during synthesis is too large). Allowing for possibly negative R, L, C values, other methods have been proposed via e.g. direct stamping [18, 19] or full realization [14, 20]. These mostly model the input/output connections of the reduced model with controlled sources.

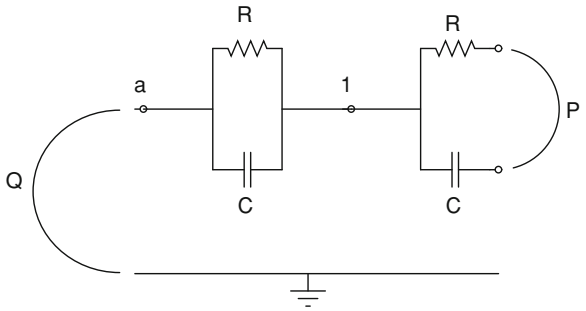

Fig. 12.1 Circuit with terminal a, internal node 1, port P, and port Q(a,0)

In this paper we consider two synthesis methods that do not involve controlled sources: (1) *Foster synthesis* [13], where the realization is done via the system's transfer function and (2) *RLCSYN synthesis by unstamping* [29], which exploits input–output structure preservation in the reduced system matrices (provided that the original system matrices are written in *modified nodal analysis (MNA)* representation). The focus of this paper is on structure preservation and RLCSYN, especially because synthesis by unstamping is simple to implement for both SISO and MIMO systems. Strengthening the result of [29], we give a simple procedure to reduce either current- or voltage-driven circuits directly in impedance form, enabling synthesis without controlled sources. The reduced order model is available as a netlist, making it suitable for simulation and reuse in other designs. Similar software [8] is commercially available.

The material in this chapter is organized as follows. The remainder of this section introduces terminology for the different nodes pertaining to a circuit topology (Sect. 12.1.1). A brief mathematical formulation of model order reduction is given in Sect. 12.1.2. The Foster synthesis is presented in Sect. 12.2. In Sect. 12.3 we focus on reduction and synthesis with structure (and input/output) preservation. Section 12.3.1 describes the procedure to convert admittance models to impedance form, so that synthesized models are easily (re)used in simulation. Based on [29], Sect. 12.3.2 is an outline of SPRIM/IOPOR reduction and RLCSYN synthesis. Numerical considerations on SPRIM/IOPOR are covered in Sect. 12.3.3. Experiments follow in Sect. 12.4, and Sect. 12.5 concludes.

12.1.1 Internal Nodes, Terminals, and Ports

The terms internal nodes, terminals (or external nodes), and ports often occur in electronic engineering related papers. An *internal node* is a node in a circuit that is not visible on the outside of a circuit, i.e., no currents can be injected in an internal node (cf. node 1 in Fig. 12.1). A *terminal (external node)* is a node that is visible on the outside, i.e., a node in which currents can be injected (cf. node a in Fig. 12.1). A port consists of two terminals that can be connected, for instance, by a source or another (sub)circuit (cf. port P in Fig. 12.1). Sometimes terminals are referred to as ports and vice versa: from the context it should then be clear which terminal(s) complete the ports; usually it is implicitly assumed that the ground node completes the ports. In Fig. 12.1, for instance, terminal a can be seen as a port (Q) by including the ground node.

12.1.2 Problem Formulation

In this paper the dynamical systems $\Sigma(\mathbf{A}, \mathbf{E}, \mathbf{B}, \mathbf{C}, \mathbf{D})$ are of the form $\mathbf{E}\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t)$, $\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t)$, where $\mathbf{A}, \mathbf{E} \in \mathbb{R}^{n \times n}$, $\mathbf{E}$ may be

singular but the pencil $(\mathbf{A}, \mathbf{E})$ is regular, $\mathbf{B} \in \mathbb{R}^{n\times m}$, $\mathbf{C} \in \mathbb{R}^{p\times n}$, $\mathbf{x}(t) \in \mathbb{R}^n$, and $\mathbf{u}(t) \in \mathbb{R}^m$, $\mathbf{y}(t) \in \mathbb{R}^p$, $\mathbf{D} \in \mathbb{R}^{p\times m}$. If $m, p > 1$, the system is called multiple-input multiple-output (MIMO), otherwise it is called single-input single-output (SISO). The frequency domain transfer function is defined as $\mathbf{H}(s) = \mathbf{C}(s\mathbf{E} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}$. For systems in MNA form arising in circuit simulation see Sect. 12.3

The model order reduction problem is to find, given an n-th order (descriptor) dynamical system, a k-th order system, $k<n$: $\widetilde{\mathbf{E}}\dot{\tilde{\mathbf{x}}}(t) = \widetilde{\mathbf{A}}\tilde{\mathbf{x}}(t) + \widetilde{\mathbf{B}}\mathbf{u}(t)$, $\tilde{\mathbf{y}}(t) = \widetilde{\mathbf{C}}\tilde{\mathbf{x}}(t) + \mathbf{D}\mathbf{u}(t)$, such that the output approximation error $\|\mathbf{y}(t) - \tilde{\mathbf{y}}(t)\|$ (in appropriate norm) is small. The corresponding dimensions are: $\widetilde{\mathbf{E}}, \widetilde{\mathbf{A}} \in \mathbb{R}^{k\times k}$, $\widetilde{\mathbf{B}} \in \mathbb{R}^{k\times m}$, $\widetilde{\mathbf{C}} \in \mathbb{R}^{p\times k}$, $\tilde{\mathbf{x}}(t) \in \mathbb{R}^k$, $\mathbf{u}(t) \in \mathbb{R}^m$, $\tilde{\mathbf{y}}(t) \in \mathbb{R}^p$, and $\mathbf{D} \in \mathbb{R}^{p\times m}$. The number of inputs and outputs is the same as for the original system, and the corresponding transfer function becomes: $\widetilde{\mathbf{H}}(s) = \widetilde{\mathbf{C}}(s\widetilde{\mathbf{E}} - \widetilde{\mathbf{A}})^{-1}\widetilde{\mathbf{B}} + \mathbf{D}$. For an overview of model order reduction methods, see [1, 5, 25]. Projection based model order reduction methods construct a reduced order model via the Petrov–Galerkin projection:

$$\widetilde{\Sigma}(\widetilde{\mathbf{E}}, \widetilde{\mathbf{A}}, \widetilde{\mathbf{B}}, \widetilde{\mathbf{C}}, \mathbf{D}) \equiv (\mathbf{W}^*\mathbf{E}\mathbf{V}, \mathbf{W}^*\mathbf{A}\mathbf{V}, \mathbf{W}^*\mathbf{B}, \mathbf{C}\mathbf{V}, \mathbf{D}), \tag{12.1}$$

where $\mathbf{V}, \mathbf{W} \in \mathbb{R}^{n\times m}$ are matrices whose $k \ll n$ columns form bases for relevant subspaces of the state-space. There are several projection methods, that differ in the way the matrices $\mathbf{V}$ and $\mathbf{W}$ are chosen. These also determine which properties are preserved after reduction. Some stability preserving methods are: *modal approximation* [24], *poor man's TBR* [22]. Among *moment matching* [11] methods, the following preserve passivity *PRIMA* [19], *SPRIM* [10], *spectral zero interpolation* [2, 16, 26]. From the balancing methods, *balanced truncation* [4] preserves stability, and *positive real balanced truncation* [21, 27] preserves passivity.

12.2 Foster Synthesis of Rational Transfer Functions

This section describes the Foster synthesis method, which was developed in the 1930s by Foster and Cauer [13] and involves realization based on the system's transfer function. The Foster approach can be used to realize any reduced order model that is computed by standard projection based model order reduction techniques. Realizations will be described in terms of SISO impedances (Z-parameters). For equivalent realizations in terms of admittances (Y-parameters), see for instance [13, 28]. Given the reduced, proper system (12.1) and assuming that all its finite poles are simple [i.e., the matrix pencil $(\widetilde{\mathbf{A}}, \widetilde{\mathbf{E}})$ is non-defective], consider the partial fraction expansion [17] of its transfer function:

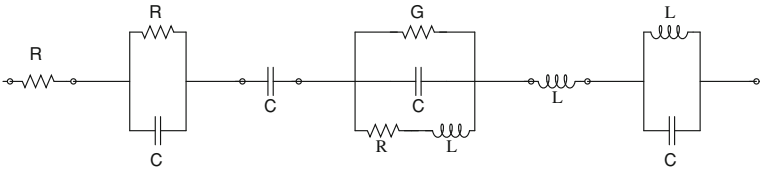

Fig. 12.2 Realization of a general impedance transfer function as a series *RLC* circuit

Table 12.1 Circuit element values for Fig. 12.2 for the Foster impedance realization of (12.3)

pole	residue	$R(\Omega)$	C(F)	L(H)	$G(\Omega^{-}1)$
$p_1 = \infty$	$r_1 \in \mathbb{R}$	r_1			
$p_2 \in \mathbb{R}$	$r_2 \in \mathbb{R}$	$-\frac{r_2}{p_2}$	$\frac{1}{r_2}$		
$p_3 = 0$	$r_3 \in \mathbb{R}$		$\frac{1}{r_3}$		
$p_4 = \sigma + i\omega \in \mathbb{C}$	$r_4 = \alpha + i\beta \in \mathbb{C}$	$\frac{a_0}{a_1}L$	$\frac{1}{a_1}$	$\frac{a_1^3}{a_1^2 b_0 - a_0(a_1 b_1 - a_0)}$	$\frac{a_1 b_1 - a_0}{a_1^2}$
$p_5 \equiv \bar{p}_4$	$r_5 \equiv \bar{r}_4$				
	$a_0 = -2(\alpha\sigma + \beta\omega)$,	$a_1 = 2\alpha$,	$b_0 = \sigma^2 + \omega^2$,	$b_1 = -2\sigma$	
$p_6 = \infty$	$r_6 \in \mathbb{R}$			r_6	
$p_7 \in i\mathbb{R}$	$r_7 \in \mathbb{R}$		$\frac{1}{r_7}$	$\frac{2r_7}{p_7\bar{p}_7}$	
$p_8 \equiv \bar{p}_7$	$r_8 \equiv \bar{r}_7$				

$$\widetilde{\mathbf{H}}(s) = \sum_{i=1}^{k} \frac{\tilde{r}_i}{s - \tilde{p}_i} + \mathbf{D}, \tag{12.2}$$

The residues are $\tilde{r}_i = \frac{(\widetilde{\mathbf{C}}\tilde{\mathbf{x}}_i)(\tilde{\mathbf{y}}_i^* \widetilde{\mathbf{B}})}{\tilde{\mathbf{y}}_i^* \widetilde{\mathbf{E}} \tilde{\mathbf{x}}_i}$, the poles are $\tilde{p}_i$ and, if non-zero, $\mathbf{D}$ gives additional contribution from poles at ∞. An eigentriplet $(\tilde{p}_i, \tilde{\mathbf{x}}_i, \tilde{\mathbf{y}}_i)$ is composed of an eigenvalue $\tilde{p}_i$ of $(\widetilde{\mathbf{A}}, \widetilde{\mathbf{E}})$ and the corresponding right and left eigenvectors $\tilde{\mathbf{x}}_i, \tilde{\mathbf{y}}_i \in \mathbb{C}^k$. The proper expansion (12.2) belongs to the more general class of transfer functions (not necessarily proper) which can be expressed using basic summands of the form:

$$Z(s) = r_1 + \frac{r_2}{s - p_2} + \frac{r_3}{s} + \left(\frac{r_4}{s - p_4} + \frac{\bar{r}_4}{s - \bar{p}_4}\right) + sr_6 + \left(\frac{r_7}{s - p_7} + \frac{r_7}{s - \bar{p}_7}\right). \tag{12.3}$$

For completeness, in (12.3) we can assume that any kind of poles may appear, i.e., either purely real, purely imaginary, in complex conjugate pairs, at ∞ or at 0 (see also Table 12.1). The Foster realization converts each term in (12.3) into the corresponding circuit block with R, L, C components, and connects these blocks in series in the final netlist. This is shown in Fig. 12.2. Note that any reordering of the circuit blocks in the realization of (12.3) in Fig. 12.2 still is a realization of

(12.3). The values for the circuit components in Fig. 12.2 are determined according to Table 12.1.

The realization in netlist form can be implemented in any language such as SPICE [9], so that it can be reused and combined with other circuits as well. The advantages of Foster synthesis are: (1) its straightforward implementation for single-input-single-output (SISO) transfer functions, via either the impedance or the admittance transfer function, (2) after reducing purely *RC* or *RL* circuits via modal approximation [24], the reduced netlists obtained from Foster synthesis are guaranteed to have positive *RC* or *RL* values respectively (see [15] for a proof). Note however that Foster synthesis does not guarantee positive circuit elements in general (e.g., when used to synthesize reduced models originating from *RLC* circuits, or reduced models of *RC* and *RL* circuits that were obtained with methods different than modal approximation). The main disadvantage is that for multi-input-multi-output transfer functions, finding the Foster realization (see for instance [28]) is cumbersome and may also give dense reduced netlists (i.e., all nodes are interconnected). This is because the Foster synthesis of a k-dimensional reduced system with p terminals, will generally yield $O(p^2k)$ circuit elements.

12.3 Structure Preservation and Synthesis by Unstamping

This section describes the second synthesis approach, which is based on *unstamping* the reduced matrix data into an *RLC* netlist and is denoted by RLCSYN [29]. It is suitable for obtaining netlist representations for models reduced via methods that preserve the MNA structure and the input–output connectivity at the circuit terminals. Such a method is the *input–output structure preserving* method SPRIM/IOPOR [29]. The strength of the result in [29] is that the input/output connectivity is synthesized after reduction without controlled sources, provided that the system is in *impedance form* (i.e., inputs are currents injected into the circuit terminals, and outputs are voltages measured at the terminals). For ease of understanding, the input–output structure preserving reduction from [29] can be interpreted as model reduction with *preservation of external nodes* [e.g., after reducing the circuit in Fig. 12.1, the nodes forming ports Q and P are external (terminals) and will also appear in the synthesized reduced model]. This way the reduced netlist can be easily coupled to other circuitry in place of the original netlist, and (re)using the reduced model in simulation becomes straightforward. The main drawback is that, when the reduced system matrices are dense and the number of terminals is large [$O(10^3)$], the RLCSYN unstamping procedure yields dense netlists. For a k dimensional reduced network with p terminals, the RLCSYN synthesized netlist will generally have $O(p^2k^2)$ circuit elements.

First, we motivate reduction and synthesis in impedance form, and show how it also applies for systems that are originally in admittance form. Then we explain model reduction via SPRIM/IOPOR, followed by RLCSYN synthesis. Finally, a note on numerical aspects concerning the SPRIM/IOPOR projection is given.

12.3.1 A Simple Admittance to Impedance Conversion

In [29] it was shown how SPRIM/IOPOR preserves the structure of the input/output connectivity when the original model is in impedance form, allowing for synthesis via RLCSYN without controlled sources. The emerging question is: how to ensure synthesis without controlled sources, if the original model is in admittance form (i.e., it is voltage driven)? We show that reduction and synthesis via the input impedance transfer function can be performed, also when the original circuit is initially voltage driven.

Consider the modified nodal analysis (MNA) description of an input *admittance*[1] type *RLC* circuit, driven by n_s voltage sources:

$$\underbrace{\begin{pmatrix} \mathscr{C} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathscr{L} \end{pmatrix}}_{\mathbf{E}_Y} \underbrace{\frac{d}{dt}\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_S(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\dot{\mathbf{x}}_Y} + \underbrace{\begin{pmatrix} \mathscr{G} & \mathscr{E}_v & \mathscr{E}_l \\ -\mathscr{E}_v{}^* & \mathbf{0} & \mathbf{0} \\ -\mathscr{E}_l{}^* & \mathbf{0} & \mathbf{0} \end{pmatrix}}_{-\mathbf{A}_Y} \underbrace{\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_S(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\mathbf{x}_Y} = \underbrace{\begin{pmatrix} \mathbf{0} \\ \mathscr{B} \\ \mathbf{0} \end{pmatrix}}_{\mathbf{B}_Y} \mathbf{u}(t), \tag{12.4}$$

where $\mathbf{u}(t) \in \mathbb{R}^{n_s}$ are input voltages and $\mathbf{y}(t) = \mathbf{C}_Y \mathbf{x}(t) \in \mathbb{R}^{n_s}$ are output currents, $\mathbf{C}_Y = \mathbf{B}_Y^*$. The states are $\mathbf{x}_Y(t)^T = [\mathbf{v}(t), \mathbf{i}_S(t), \mathbf{i}_L(t)]^T$, with $\mathbf{v}(t) \in \mathbb{R}^{n_v}$ the node voltages, $\mathbf{i}_S(t) \in \mathbb{R}^{n_s}$ the currents through the voltage sources, and $\mathbf{i}_L(t) \in \mathbb{R}^{n_l}$ the currents through the inductors, $n_v + n_s + n_l = n$. The $n_v = n_1 + n_2$ node voltages are formed by the n_1 external nodes/terminals[2] and the n_2 internal nodes (assuming that the voltage sources may be ungrounded, n_1 satisfies: $n_s < n_1 \leq 2n_s + 1$). The dimensions of the underlying matrices are: $\mathscr{C} \in \mathbb{C}^{n_v \times n_v}$, $\mathscr{G} \in \mathbb{C}^{n_v \times n_v}$, $\mathscr{E}_v \in \mathbb{C}^{n_v \times n_s}$, $\mathscr{L} \in \mathbb{C}^{n_l \times n_l}$, $\mathscr{E}_l \in \mathbb{C}^{n_v \times n_l}$, $\mathscr{B} \in \mathbb{C}^{n_1 \times n_s}$. Assuming without loss of generality that (12.4) is permuted such that the *first* n_1 nodes are the external nodes, the input voltages are determined by a linear combination of $\mathbf{v}_{1:n_1}(t)$ only. Thus the following holds:

$$\mathscr{E}_v = \begin{pmatrix} \mathscr{B}_v \\ \mathbf{0}_{n_2 \times n_s} \end{pmatrix} \in \mathbb{C}^{n_v \times n_s}, \quad \mathscr{B}_v \in \mathbb{C}^{n_1 \times n_s}, \quad \mathscr{B} = -\mathscr{B}_v. \tag{12.5}$$

We derive the first order impedance-type system associated with (12.4). Note that by definition, $\mathbf{i}_S(t)$ flows *out of* the circuit terminals into the voltage source (i.e., from the + to the − terminal of the voltage source, see also [19, Fig. 3], [15]).

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[1] The subscript Y refers to quantities associated with a system in admittance form.

[2] The MNA form (12.4) corresponds to the ungrounded circuit (i.e., the reference node is counted within the n_1 external nodes), resulting in a defective matrix pencil $(\mathbf{A}_Y, \mathbf{E}_Y)$. For subsequent computations such as the construction of a Krylov subspace, the pencil $(\mathbf{A}_Y, \mathbf{E}_Y)$ must be regular. Thus in (12.4), one node must be chosen as a ground (reference) node by removing the row/column corresponding to that node; this ensures that the regularity conditions (i) and (ii) from [23, page 5, Assumption 4] are satisfied. The positive definiteness of $\mathscr{C}, \mathscr{L}, \mathscr{G}$ is also a necessary condition to ensure the circuit's passivity.

We can define new input currents as the currents flowing *into* the circuit terminals: $\mathbf{i}_{in}(t) = -\mathbf{i}_S(t)$. Since $\mathbf{v}_{1:n_1}(t)$ are the terminal voltages, they describe the new output equations, and it is straightforward to rewrite (12.4) in the impedance form:

$$\begin{cases} \underbrace{\begin{pmatrix} \mathscr{C} & \mathbf{0} \\ \mathbf{0} & \mathscr{L} \end{pmatrix}}_{\mathbf{E}} \underbrace{\frac{d}{dt}\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\dot{\mathbf{x}}} + \underbrace{\begin{pmatrix} \mathscr{G} & \mathscr{E}_l \\ -\mathscr{E}_l{}^* & \mathbf{0} \end{pmatrix}}_{-\mathbf{A}} \underbrace{\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\mathbf{x}} = \underbrace{\begin{pmatrix} \mathscr{E}_v \\ \mathbf{0} \end{pmatrix}}_{\mathbf{B}} \mathbf{i}_{in}(t) \\ \underbrace{\begin{pmatrix} \mathscr{E}_v^* & \mathbf{0} \end{pmatrix}}_{\mathbf{C}} \underbrace{\begin{pmatrix} \mathbf{v}(t) \\ \mathbf{i}_L(t) \end{pmatrix}}_{\mathbf{x}} = \mathbf{y}(t) = \mathscr{B}_v \mathbf{v}_{1:n_1}(t), \quad \mathscr{E}_v^* = \begin{pmatrix} \mathscr{B}_v^* \mathbf{0}_{n_s \times n_2} \end{pmatrix} \end{cases} \tag{12.6}$$

where $\mathbf{B}$ describes the new *input incidence matrix* corresponding the input currents, $\mathbf{i}_{in}$. The new *output incidence matrix* is $\mathbf{C}$, corresponding to the voltage drops over the circuit terminals. We emphasize that (12.6) has fewer unknowns than (12.4), since the currents $\mathbf{i}_S$ have been eliminated. The transfer function associated to (12.6) is an input impedance: $\mathbf{H}(s) = \frac{\mathbf{y}(s)}{\mathbf{i}_{in}(s)}$. In Sect. 12.3.2 we explain how to obtain an impedance type reduced order model in the input/output structure preserved form:

$$\begin{cases} \underbrace{\begin{pmatrix} \widetilde{\mathscr{C}} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathscr{L}} \end{pmatrix}}_{\widetilde{\mathbf{E}}} \underbrace{\frac{d}{dt}\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\dot{\widetilde{\mathbf{x}}}} + \underbrace{\begin{pmatrix} \widetilde{\mathscr{G}} & \widetilde{\mathscr{E}}_l \\ -\widetilde{\mathscr{E}}_l^* & \mathbf{0} \end{pmatrix}}_{-\widetilde{\mathbf{A}}} \underbrace{\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\widetilde{\mathbf{x}}} = \underbrace{\begin{pmatrix} \widetilde{\mathscr{E}}_v \\ \mathbf{0} \end{pmatrix}}_{\widetilde{\mathbf{B}}} \mathbf{i}_{in}(t) \\ \underbrace{\begin{pmatrix} \widetilde{\mathscr{E}}_v^* & \mathbf{0} \end{pmatrix}}_{\widetilde{\mathbf{C}}} \underbrace{\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\widetilde{\mathbf{x}}} = \mathbf{y}(t) = \mathscr{B}_{v1:n_1}(t), \quad \widetilde{\mathscr{E}}_v^* = \begin{pmatrix} \mathscr{B}_v^* \mathbf{0}_{n_s \times k_2} \end{pmatrix} \end{cases} \tag{12.7}$$

where $\widetilde{\mathscr{C}}$, $\widetilde{\mathscr{L}}$, $\widetilde{\mathscr{G}}$, $\widetilde{\mathscr{E}}_v$ are the reduced MNA matrices, and the reduced input impedance transfer function is: $\widetilde{\mathbf{H}}(s) = \frac{\widetilde{\mathbf{y}}(s)}{\mathbf{i}_{in}(s)}$. Due to the input/output preservation, the circuit terminals are easily preserved in the reduced model (12.7).

It turns out that after reduction and synthesis, the reduced model (12.7) can still be used as a voltage driven admittance block in simulation. This is shown next. We can rewrite the second equation in (12.7) as: $\begin{pmatrix} -\widetilde{\mathscr{E}}_v^* & \mathbf{0} & \mathbf{0} \end{pmatrix} \begin{pmatrix} \widetilde{\mathbf{v}}(t)^T & \widetilde{\mathbf{i}}_S(t)^T & \widetilde{\mathbf{i}}_L(t)^T \end{pmatrix}^T = \mathscr{B}\mathbf{u}(t)$. This result together with $\mathbf{i}_{in}(t) = -\mathbf{i}_S(t)$, reveals that (12.7) can be rewritten as:

$$\underbrace{\begin{pmatrix} \widetilde{\mathscr{C}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \widetilde{\mathscr{L}} \end{pmatrix}}_{\widetilde{\mathbf{E}}_Y} \underbrace{\frac{d}{dt}\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \mathbf{i}_S(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\dot{\widetilde{\mathbf{x}}}_Y} + \underbrace{\begin{pmatrix} \widetilde{\mathscr{G}} & \widetilde{\mathscr{E}}_v & \widetilde{\mathscr{E}}_l \\ -\widetilde{\mathscr{E}}_v^* & \mathbf{0} & \mathbf{0} \\ -\widetilde{\mathscr{E}}_l^* & \mathbf{0} & \mathbf{0} \end{pmatrix}}_{-\widetilde{\mathbf{A}}_Y} \underbrace{\begin{pmatrix} \widetilde{\mathbf{v}}(t) \\ \mathbf{i}_S(t) \\ \widetilde{\mathbf{i}}_L(t) \end{pmatrix}}_{\widetilde{\mathbf{x}}_Y} = \underbrace{\begin{pmatrix} \mathbf{0} \\ \mathscr{B} \\ \mathbf{0} \end{pmatrix}}_{\widetilde{\mathbf{B}}_Y} \mathbf{u}(t), \tag{12.8}$$

which has the same structure as the original admittance model (12.4). Conceptually one could have reduced system (12.4) directly via the input admittance. In that case, synthesis by unstamping via RLCSYN [29] would have required controlled sources [14]. As shown above, this is avoided by: applying the simple admittance-to-impedance conversion (12.4)–(12.6), reducing (12.6)–(12.7), and finally reinserting voltage sources after synthesis (if the input–output structure preserved admittance reduced admittance (12.8) is needed).

12.3.2 I/O Structure Preserving Reduction and RLCSYN Synthesis

The reduced input impedance model (12.7) is obtained via the input–output structure preserving SPRIM/IOPOR projection [29] as follows. Let $\mathbf{V} = \left(\mathbf{V}_1^T, \mathbf{V}_2^T, \mathbf{V}_3^T\right)^T \in \mathbb{C}^{((n_1+n_2+n_i)\times k)}$ be the projection matrix obtained with PRIMA [19], where $\mathbf{V}_1 \in \mathbb{C}^{(n_1\times k)}$, $\mathbf{V}_2 \in \mathbb{C}^{(n_2\times k)}$, $\mathbf{V}_3 \in \mathbb{C}^{(n_i\times k)}$, $k \geq n_1$, $i = 1\ldots3$. After appropriate orthonormalization (e.g., via Modified Gram–Schmidt [24, Chapter. 1]), we obtain: $\widetilde{\mathbf{V}}_i = \text{orth}(\mathbf{V}_i) \in \mathbb{C}^{n_i\times k_i}$, $k_i \leq k$. The SPRIM [10] block structure preserving projection is: $\widetilde{\mathbf{V}} = \text{blkdiag}\left(\widetilde{\mathbf{V}}_1, \widetilde{\mathbf{V}}_2, \widetilde{\mathbf{V}}_3\right) \in \mathbb{C}^{\mathrm{n}\times(\mathrm{k}_1+\mathrm{k}_2+\mathrm{k}_3)}$, which does not yet preserve the structure of the input and output matrices. The input–output structure preserving SPRIM/IOPOR [29] projection is $\widetilde{\mathbf{W}} = \begin{pmatrix} \mathbf{W} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathbf{V}}_3 \end{pmatrix} \in \mathbb{C}^{n\times(n_1+k_2+k_3)}$ where:

$$\mathbf{W} = \begin{pmatrix} \mathbf{I}_{n_1\times n_1} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathbf{V}}_2 \end{pmatrix} \in \mathbb{C}^{(n_1+n_2)\times(n_1+k_2)}. \tag{12.9}$$

Recalling (12.5), we obtain the reduced system matrices in (12.7): $\widetilde{\mathscr{C}} = \mathbf{W}^*\mathscr{C}\mathbf{W}$, $\widetilde{\mathscr{G}} = \mathbf{W}^*\mathscr{G}\mathbf{W}$, $\widetilde{\mathscr{L}} = \widetilde{\mathbf{V}}_3^*\mathscr{L}\widetilde{\mathbf{V}}_3$, $\widetilde{\mathscr{E}}_l = \mathbf{W}^*\mathscr{E}_l\widetilde{\mathbf{V}}_3$, $\widetilde{\mathscr{E}}_v = \mathbf{W}^*\mathscr{E}_v = \left(\mathscr{B}_v^* \quad \mathbf{0}_{n_s\times k_2}\right)^*$, which compared to (12.5) clearly preserve input–output structure. Therefore a netlist representation for the reduced impedance-type model can be obtained, that is driven by injected currents just as the original circuit. This is done via the RLCSYN [29] unstamping procedure. To this end, we use the Laplace transform and convert (12.7) to the second order form:

$$\begin{cases} [s\widetilde{\mathscr{C}} + \widetilde{\mathscr{G}} + \frac{1}{s}\widetilde{\Gamma}]\widetilde{\mathbf{v}}(s) = \widetilde{\mathscr{E}}_v\mathbf{i}_{in}(s) \\ \widetilde{\mathbf{y}}(s) = \widetilde{\mathscr{E}}_v^*\widetilde{\mathbf{v}}(s), \end{cases} \tag{12.10}$$

where $\widetilde{\mathbf{i}}_L(s) = \frac{1}{s}\widetilde{\mathscr{L}}^{-1}\left(\widetilde{\mathscr{E}}_l^*\right)\widetilde{\mathbf{v}}(s)$ and $\widetilde{\Gamma} = \widetilde{\mathscr{E}}_l\widetilde{\mathscr{L}}^{-1}\widetilde{\mathscr{E}}_l^*$.

The presentation of RLCSYN follows [29, Sect. 4], [15] and is only summarized here. In circuit simulation, the process of forming the $\mathscr{C}, \mathscr{G}, \mathscr{L}$ system matrices from the individual branch element values is called "stamping".

The reverse operation of "unstamping" involves decomposing entry-wise the values of the reduced system matrices in (12.10) into the corresponding R, L, and C values. The resulting Rs, Ls and Cs are connected in the reduced netlist according to the MNA topology. The reduced input/output matrices of (12.10) directly reveal the input connections in the reduced model via injected currents, without any controlling elements. The prerequisites for an unstamping realization procedure therefore are:

1. The original system is in MNA impedance form (12.6). If the system is of admittance type (12.4), apply the admittance-to-impedance conversion from Sect. 12.3.1.
2. In (12.6), no Ls are directly connected to the input terminals so that, after reduction, diagonalization and regularization preserve the input/output structure.
3. System (12.6) is reduced with SPRIM/IOPOR [28] to (12.7) and converted to second order form (12.10). The alternative is to obtain the second order form of the original system first, and reduce it directly with SAPOR/IOPOR [3, 29].
4. The reduced system (12.10) must be diagonalized and regularized according to [29]. Diagonalization ensures that all inductors in the synthesized model are connected to ground (i.e., there are no inductor loops). Regularization eliminates spurious over-large inductors. These steps however are not needed for purely RC circuits.

12.3.3 On SPRIM/IOPOR and Rank Loss of $\widetilde{\mathbf{A}}$

In some cases it was observed (and shown by results in Sect. 12.4.2) that models reduced with SPRIM or SPRIM/IOPOR exhibit poles and zeros at 0. This section explains when this happens and supports theoretically the interpretation of the results in Sect. 12.4.2

Proposition 1 *Let* $\mathbf{W}$*and* $\widetilde{\mathbf{V}}_3$ *be the SPRIM/IOPOR projection matrices* (12.9)*, with full column rank. If* $\widetilde{\mathscr{E}}_l = \mathbf{W}^*\mathscr{E}_l\widetilde{\mathbf{V}}_3$ *in* (12.3.2) *has deficient column rank, then the SPRIM/IOPOR reduced model* (12.7) *has at least a pole-zero pair at* 0.

Proof Recalling that $\widetilde{\mathbf{V}}_2$ has full column rank, it is clear from (12.9) that $\mathbf{W}$ also has full column rank. Nonetheless $\mathbf{W}^* \in \mathbb{C}^{(n_1+k_2)\times(n_1+n_2)}$ has more columns than rows (usually $k_2 \ll n_2$), thus $\mathbf{W}^*$ is column rank deficient. Hence $\widetilde{\mathscr{E}}_l = \mathbf{W}^*\mathscr{E}_l\widetilde{\mathbf{V}}_3$ will have deficient column rank (even if $\mathscr{E}_l$ and $\widetilde{\mathbf{V}}_3$ have full column rank). Then in (12.7) we have: $\text{rank}(\widetilde{\mathbf{A}}) < \#\text{cols}(\widetilde{\mathbf{A}})$. Thus $\widetilde{\mathbf{A}}$ has deficient column rank $\Rightarrow$ $\widetilde{\mathbf{A}}$ has at least an eigenvalue at $0 \Rightarrow 0$ is also an eigenvalue of the pencil $(\widetilde{\mathbf{A}}, \widetilde{\mathbf{E}})$ and this is a pole at 0. The zeros of the reduced system (12.7) are determined via the

Rosenbrock matrix [23, Chapter 5]: $\widetilde{\mathbf{A}}_z = \begin{bmatrix} \widetilde{\mathbf{A}} & \widetilde{\mathbf{B}} \\ -\widetilde{\mathbf{C}} & \mathbf{0} \end{bmatrix} = \begin{bmatrix} -\widetilde{\mathscr{G}} & -\widetilde{\mathscr{E}}_l & \widetilde{\mathscr{E}}_v \\ \widetilde{\mathscr{E}}_l^* & \mathbf{0} & \mathbf{0} \\ -\widetilde{\mathscr{E}}_v^* & \mathbf{0} & \mathbf{0} \end{bmatrix}$, which immediately reveals that if $\widetilde{\mathscr{E}}_l$ is column rank deficient, then $\widetilde{\mathbf{A}}_z$ also loses rank and will have a 0 eigenvalue. Therefore the SPRIM/IOPOR reduced system (12.7) will also have a zero at 0. □

Analytically, pole-zero pairs at 0 are harmless since they theoretically cancel. Numerically this may not be the case, altering the approximation for low frequencies (as seen for instance in the result in Sect. 12.4.2).

12.4 Numerical Examples

Two circuits are chosen to demonstrate the applicability of the model reduction and synthesis procedures treated in this paper. For the single-input-single-output (SISO) example, one can easily provide synthesized models via both Foster and RLCSYN. For the multi-input-multi-output (MIMO) example, a synthesized model can be obtained straightforwardly with RLCSYN, thus RLCSYN synthesis is preferred over Foster synthesis.

12.4.1 SISO RLC *Network*

We reduce the SISO *RLC* transmission line in Fig. 12.3. Note that the circuit is driven by the voltage **u**, thus it is of admittance type (12.4). The admittance simulation of the model reduced with the *dominant spectral zero method (Dominant SZM)* [16], synthesized with the Foster approach, is shown in Fig. 12.5. The behavior of the original model is well approximated for the entire frequency range, and can also reproduce oscillations at dominant frequency points.

The benefit of the admittance-to-impedance transformation described in Sect. 12.3.1 is seen in Fig. 12.6. By reducing the system in impedance form with SPRIM/IOPOR and synthesizing (12.7) (using the second order form (12.10)) with RLCSYN [29], we are able to recover the reduced admittance (12.8) as well. The approximation is good for the entire frequency range.

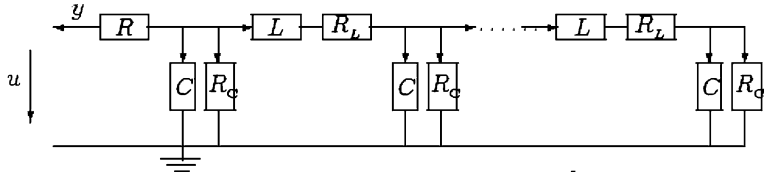

Fig. 12.3 Transmission line from Sect.12.4.1

12.4.2 *MIMO* RLC *Network*

We reduce the MIMO *RLC* netlist resulting from the parasitic extraction [12] of the coil structure in Fig. 12.4. The model has 4 pins (external nodes). Pin 4 is connected to other circuit nodes only via *C*'s, which causes the original model (12.6) to have a pole at 0. The example shows that: (1) the SPRIM/IOPOR model preserves the terminals and is synthesizable with RLCSYN without controlled sources, and (2) structure preserving projections may affect numerical cancellations of pole-zero pairs at 0.

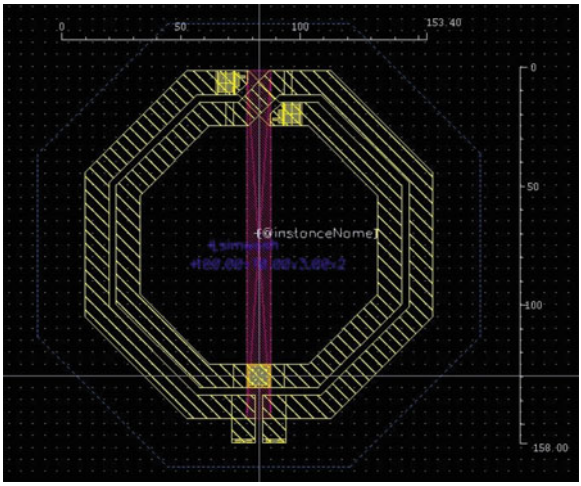

Fig. 12.4 Coil structure from Sect.12.4.2

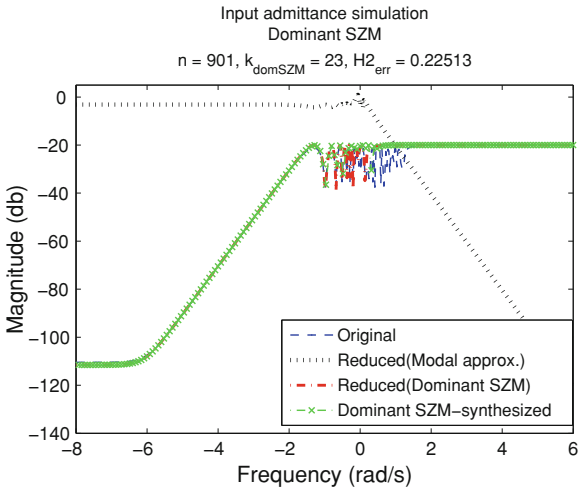

Fig. 12.5 Input admittance transfer function: original, reduced with Dominant SZM in admittance form and synthesized with Foster admittance

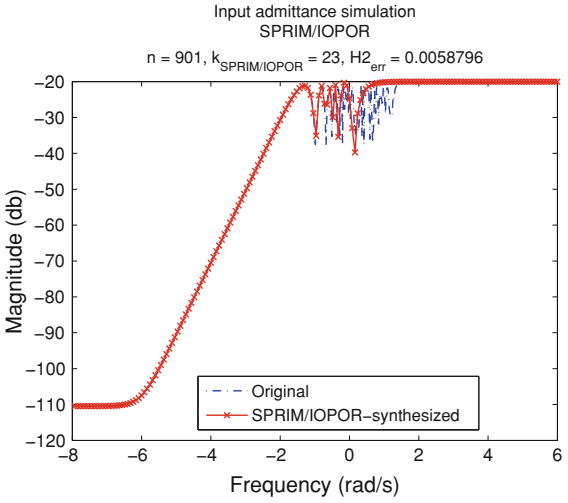

Fig. 12.6 Input admittance transfer function: original and synthesized SPRIM/IOPOR model (via impedance), after reconnecting the voltage source at the input terminal

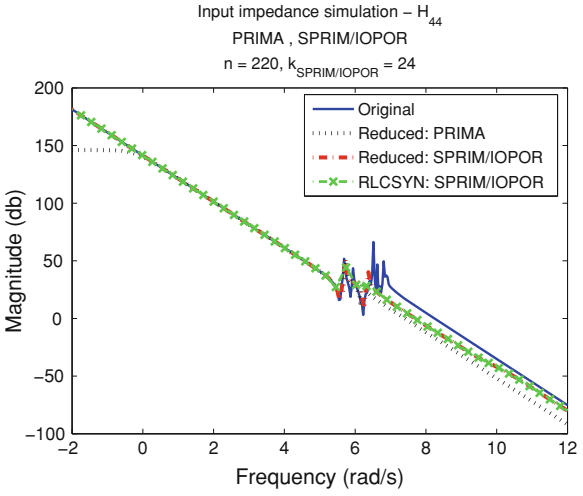

Fig. 12.7 Input impedance transfer function with "v_4" kept: $\mathbf{H}_{44}$ for PRIMA, SPRIM/IOPOR and RLCSYN realization

Fig. 12.7 shows the simulation of the transfer function from input 4 to output 4, which clearly reflects the presence of the pole at 0 due to the large response magnitude for low frequencies. By inspecting the response from input 3 to output 3 however, we notice in Fig. 12.8 that the SPRIM/IOPOR model is less accurate around DC than PRIMA. The SPRIM/IOPOR (12.9) projection approximates the original pole at 0 by a small pole (not at 0), but still places zeros at 0 due to the dependencies created in the Rosenbrock matrix $\widetilde{\mathbf{A}}_z$ (see Sect. 12.3.3). Such pole-zero pairs can no longer cancel numerically, affecting the approximation quality for low frequencies.

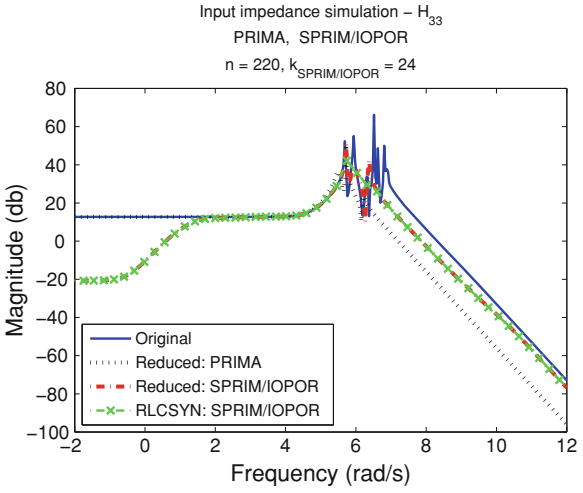

Fig. 12.8 Input impedance transfer function with "v_4" kept: $\mathbf{H}_{33}$ for PRIMA, SPRIM/IOPOR and RLCSYN realization

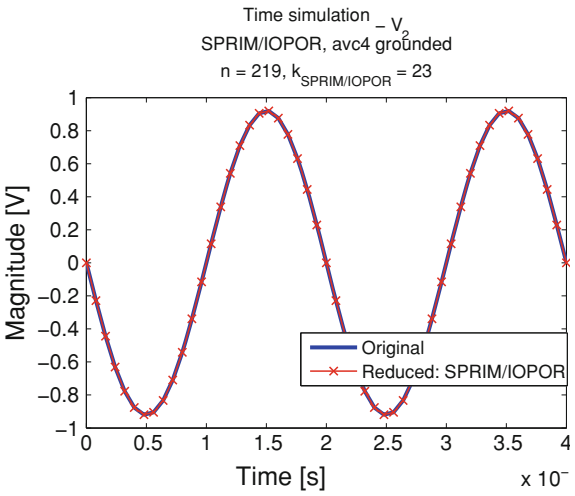

Fig. 12.9 Transient simulation with "v_4" grounded: voltage measured at node 2 for SPRIM/IOPOR (from RLCSYN realization)

The alternative is to ground pin 4 prior to reduction. This will remove the pole at 0 from the original model, resolve the corresponding numerical cancellation effects, and improve approximation around DC. As seen from Fig. 12.10, SPRIM/IOPOR applied on the remaining 3-terminal system gives a better approximation than PRIMA for the entire frequency range. The transient simulation in Fig. 12.9 confirms that the SPRIM/IOPOR model is both accurate and stable. With pin 4 grounded however, we loose the ability to (re)connect the synthesized model in simulation via all the terminals .

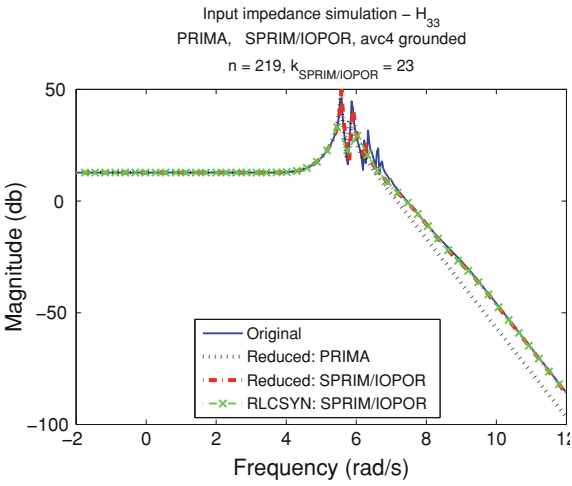

Fig. 12.10 Input impedance transfer function with "v_4" grounded: $\mathbf{H}_{33}$ for PRIMA, SPRIM/IOPOR and RLCSYN realization

Table 12.2 Summary and comparison of synthesis methods

To summarize	Projection and Foster realization of $\hat{\mathbf{H}}(s)$	I/O pres. SPRIM and RLCSYN unstamping
Properties	Passivity guaranteed by positive realness of $\hat{\mathbf{H}}(s)$ from appropriate $\mathbf{V}$, $\mathbf{W}$	Passivity ensured via congruence transformation $\tilde{\mathbf{W}}$, $\tilde{\mathbf{W}}^T\tilde{\mathbf{W}} = \mathbf{I}$ on Σ in MNA form
Advantages	Σ need not be in MNA form	Preserved I/O and MNA structure
	RC, *RL* reduced with modal approximation $\Rightarrow$ positive elements	Unstamping easy for MIMO via impedance $\hat{\Sigma}$
Main hurdles	MIMO realization for >2 terminals only for **admittance** $\mathbf{H}(s)$ and $\hat{\mathbf{H}}(s)$	$\widetilde{\mathscr{G}}$ may loose rank
	Dense MIMO netlists	Reduced $\widetilde{\mathscr{G}}$,$\widetilde{\mathscr{C}}$, are dense
	For p ports, k poles $O(p^2k)$ circuit elements	For p ports, k moments $O(p^2k^2)$ circuit elements
	Positive *R*, *L*, *C* not guaranteed	Positive *R*, *L*, *C* not guaranteed

12.5 Conclusions and Outlook

A framework for realizing reduced mathematical models into *RLC* netlists was developed. Model reduction by projection for *RLC* circuits was described and associated with two synthesis approaches: Foster realization (for SISO transfer functions) and RLCSYN [29] synthesis by unstamping (for MIMO systems). The approaches were tested on several examples, and a comparison is shown in Table 12.2. Future research will investigate reduction and synthesis methods for *RCLK* circuits with many terminals.

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