Chapter 7

Charge Pumps for LCD Drivers

by Gaetano Palumbo and Domenico Pappalardo

It was shown in Chapters 4 and 6 that LCD drivers, especially those for small-size panels, make extensive use of charge pumps. High-voltage boosting circuits are indeed required to generate the row and column voltages if the external supply is kept low to contain power consumption and area of the digital section [YKC2003], [SK2008]. Owing to the consequent relevance of an optimized CP design and also because a comprehensive treatment of the subject is missing in electronic textbooks, we decided to include this chapter as a conclusion of the book.

A Charge Pump (CP) is an electronic circuit that converts the supply voltage V_{DD} to a DC output voltage V_{Out} that is several times higher than V_{DD} (i.e., it is a DC-DC converter whose input voltage is lower than the output one) [D1976], [WGM1989]. Unlike the other traditional DC-DC converters, which employ inductors, CPs are made up of capacitors and switches (or diodes) only, thereby allowing integration on silicon. CPs were originally used in smart power ICs [H1990, WVK1992, GP1994, GP1996] and nonvolatile memories [JNH1992, UKA1992, AKU1994, CGO1999, ZLD2001, IOS2001, PPG2006] and, given the continuous scaling down of IC power supplies, they have also been employed in a vast variety of integrated systems [CT1991, DD1998, BN1998, MS1998, NGN2001, MC2001].

In practical applications, CPs may be either loaded by a simple capacitor (or equivalently the gate of a MOS transistor) or by more complex networks. In the last case the CP load can be simply modeled by means of an equivalent capacitance and an equivalent current generator whose value is given by the load current, which for LCD drivers is proportional to the frame frequency and the driven capacitance. A current generator can also be used to model a pure resistive load. The load type determines a change in the CP behavior, and consequently on the design strategy to be followed. Although for LCD drivers only the case with the current load has to be considered, in this chapter both the situations are considered for the sake of completeness.

D.J.R. Cristaldi et al., *Liquid Crystal Display Drivers*, DOI 10.1007/978-90-481-2255-4_7,

7.1 Analysis of the Charge Pump with a Pure Capacitive Load

7.1.1 One-Stage Charge Pump

To show the behavior of an ideal CP, let us consider the one-stage topology (Fig. 7.1) which comprises a single pumping capacitor C, two switches, S_1 and S_2 (driven by two complementary phases), a clock signal whose amplitude is equal to the power supply V_{DD} (Fig. 7.2) and a pure capacitive load C_L (also referred to as the bulk capacitor).

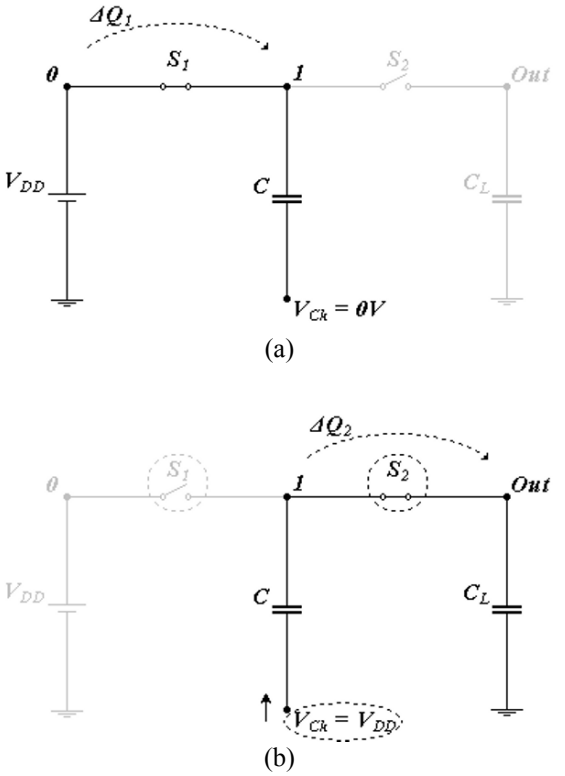

Fig. 7.1 Ideal one-stage CP: (**a**) first half period; (**b**) second half period

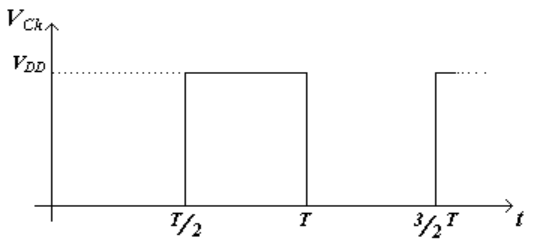

Fig. 7.2 Clock signal, V_{Ck}, of the CP in Fig. 7.1

During the first half period (0 to $T/2$), S_1 and S_2 are respectively closed and open and C, being connected to the power supply, is charged to V_{DD} (Fig. 7.1a). In the second half period ($T/2$, T) the switches change their state, the clock signal now equals V_{DD}, and part of the charge stored in C is transferred to C_L. Hence, at each cycle the output voltage will increase up to the final asymptotic value, $2V_{DD}$. In a generic period j, considering that C is charged to V_{DD} before redistribution and that the charge into C_L is the one stored in the previous period being equal to C_L $V_{Out}(j-1)$, we get the recursive equation

$$V_{Out}(j) = \frac{C \cdot 2V_{DD} + C_L \cdot V_{Out}(j-1)}{C + C_L} \tag{7.1}$$

The above equation is plotted in Fig. 7.3. It is apparent that several cycles are needed to approach $2V_{DD}$ and that the step increment of the output voltage in each successive clock period becomes smaller. Indeed, the output voltage will steeply increase in the first part of the transient and will slowly tend to its final value, where no charge redistribution will ideally happen.

In conclusion, according to its name, a CP takes charges from the power supply, via the capacitor C, and pumps these charges into the output capacitor C_L, thus increasing the output voltage up to an ideal value that is twice the power supply.

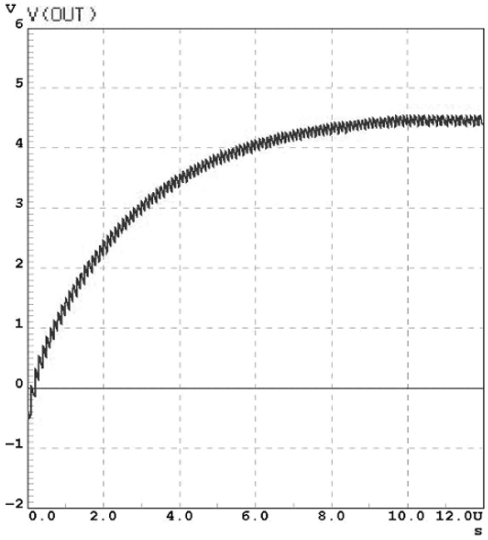

Fig. 7.3 Output voltage transient of the one-stage CP

7.1.2 *N*-stage Charge Pump

The one-stage CP topology can be generalized by including additional cascaded stages as shown in Fig. 7.4, where a generic N-stage CP is depicted. Each stage is made up of a pumping capacitor C and a switch S_i; the CP needs a two-phase clock and to properly connect the output load to the final stage switch S_{Out} is also required.

The behavior of the *N*-stage CP is similar to that of a one-stage CP. During the first half clock period, V_{Ck} is low and only the odd switches are closed (see Fig. 7.5a). The first pumping capacitor is thus charged to V_{DD} and all the other pumping capacitors in the odd stages receive the charge from the capacitor of the previous stage (this happens also for the load capacitor if the number of stages is even).

During the subsequent half clock period the signal V_{Ck} is equal to V_{DD} and only the even switches are closed (see Fig. 7.5b). Now all the capacitors in the odd stages give the charge to the capacitor in the subsequent stage (the load capacitor is maintained separated from the CP if the number of stages is even, since the switch S_{Out} is open).

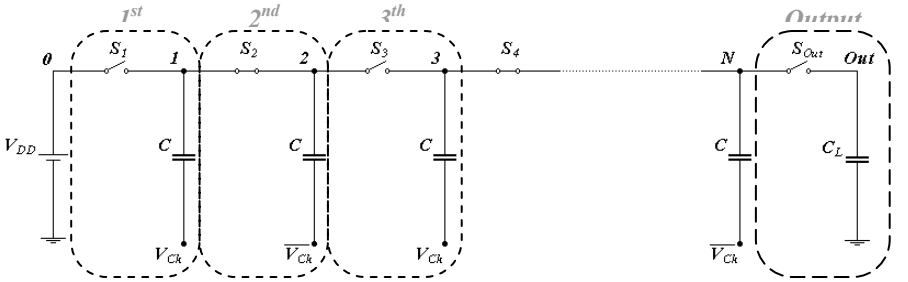

Fig. 7.4 *N*-stage charge pump

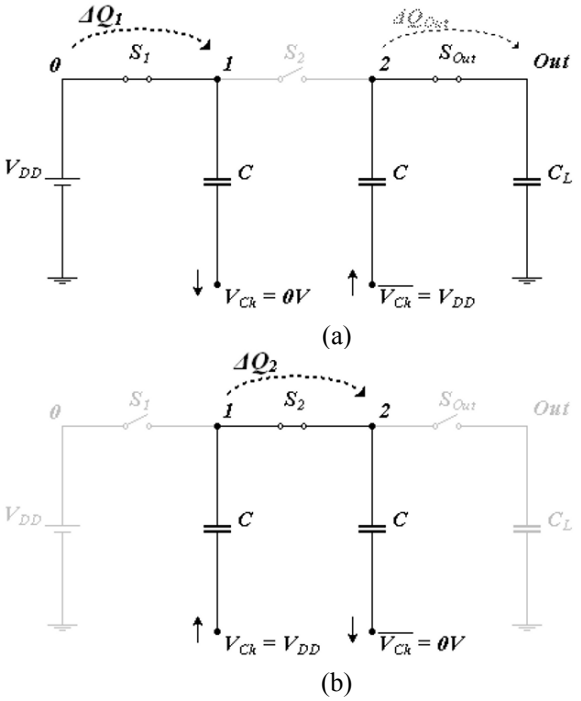

Fig. 7.5 *N*-stage CP: (**a**) first half period; (**b**) second half period

In summary, in a complete clock period, each CP capacitor receives an amount of charge from the capacitor at its left side and gives a part of this charge to the capacitor at its right side. Thus, in each period there is a charge transfer from the power supply to the output load.

7.1.3 Charge Pump Parameters

The most important design parameters of a CP are the number of stages, the silicon area occupation, the rise time and the charge consumption.

The **number of stages,** N, is strictly related to the required output voltage, V_{Out}. Indeed, the output voltage of a CP with a pure capacitive load in the steady state (i.e., when the charge transfer from the power supply to the output is ideally zero) is

$$V_{Out}\Big|_{Steady\ State} = (N+1)\cdot V_{DD} \tag{7.2}$$

To physically implement a CP, the required **total silicon area**, A_{Tot}, may be non negligible. Since this area is mainly due to the capacitors, we can approximate A_{Tot} with only the area required to implement the capacitors

$$A_{Tot} = k\cdot N\cdot C = k\cdot C_{Tot} \tag{7.3}$$

In the above equation, the parameter k depends on the processes used to realize the capacitors and C_{Tot} is the sum of the pumping capacitors (i.e., $N{\cdot}C$).

The **rise time**, t_r, is defined as the time required to achieve a defined output value $V_{Out}(t_r)$. From the dynamic models developed in [TT1997, PBB2000, PP2006], the CP rise time can be approximated with the relationship

$$t_r = T\cdot\left(N\frac{C_L}{C}+0.3N+0.6\right)\cdot\ln\left[\frac{(N+1)V_{DD}-V_{Out}(0)}{(N+1)V_{DD}-V_{Out}(t_r)}\right] \tag{7.4}$$

where T is the clock period. Moreover, for N much higher than 1, and normalizing the output voltage to the power supply

$$v_x = \frac{V_{Out}(t_r)}{V_{DD}} \tag{7.5}$$

$$v_{x0} = \frac{V_{Out}(0)}{V_{DD}} \tag{7.6}$$

we get

$$t_r = T \cdot N^2 \cdot \frac{C_L + C_{Eq}}{C_{Tot}} \cdot \ln\left(\frac{N+1-v_{x0}}{N+1-v_x}\right) \tag{7.7}$$

where capacitance C_{Eq} is equal to $C_{Tot}/3$.

As expected, to reach the output steady state voltage, $(N+1)V_{DD}$, (7.7) anticipates an infinite rise time. Moreover, it is apparent that t_r is affected by the load capacitance and the total CP capacitance, C_{Tot}.

Since from (7.7) we can write

$$V_{Out}(t_r) = (N+1)V_{DD} - \left[(N+1)V_{DD} - V_{Out}(0)\right] \cdot e^{-\frac{t_r}{\frac{N}{Cf}(C_L + C_{Eq})}} \tag{7.8}$$

the dynamic behavior of CP with a pure capacitive load is equivalent to that of a simple RC circuit [PBB2000]. More specifically, the CP model is the RC circuit in Fig. 7.6 where

$$R_{Eq} = \frac{N}{C \cdot f} \tag{7.9}$$

and $V_{Out}(+\infty)$ is the output voltage in the steady state, given by (7.2).

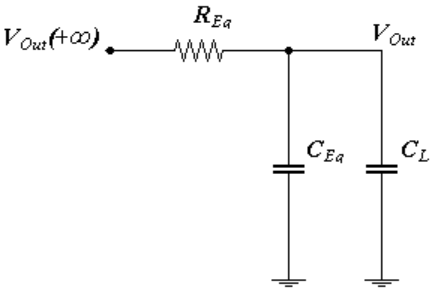

Fig. 7.6 CP equivalent model

To evaluate the **charge consumption** of a CP, we must compute the charge delivered by the power supply to the CP during its rise time. The charge consumption can be divided into three main contributes: the charge given to the load, Q_L, the charge required during the transient by the pumping capacitances, Q_{Pump}, and the contribution wasted in the parasitic elements shown in Fig. 7.7, Q_{Par}.

Note that, referring to Fig. 7.7, the parasitic capacitance at the bottom plate, C_P, of the pumping capacitors is generally more than one order of magnitude higher than that of the other plate. Thus, the charge consumption can be written as

$$Q_T = Q_L + Q_{Pump} + Q_{Par} \tag{7.10}$$

Taking into account the equivalent RC circuit in Fig. 7.6, we get

$$Q_L(t_r)+Q_{Pump}(t_r)=(N+1)\cdot(C_{Eq}+C_L)\cdot\left[V_{Out}(t_r)-V_{Out}(0)\right] \qquad (7.11)$$

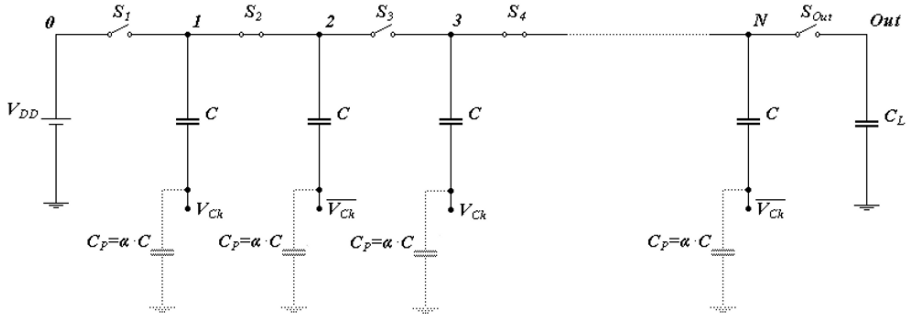

Fig. 7.7 *N*-stage CP with parasitic effects

During each clock period, the charge loss due to parasitic effects (required to charge and discharge the parasitic capacitances on the bottom plate of a pumping capacitor) can be modeled by NC_PV_{DD}, and the contribute during the rise time results to be

$$Q_{Par}=NC_PV_{DD}\frac{t_r}{T}=\alpha C_{Tot}V_{DD}\frac{t_r}{T} \qquad (7.12)$$

where the bottom plate parasitic capacitance, C_P, is assumed proportional to the pumping capacitance C through a factor α.

Substituting each contribute into (7.10), we get the expression of the total charge sunk by the power supply up to the rise time

$$Q_T(t_r)=\left[(N+1)(v_x-v_{x0})+\alpha N^2\ln\frac{N+1-v_{x0}}{N+1-v_x}\right]\left(C_{Eq}+C_L\right)\cdot V_{DD} \qquad (7.13)$$

7.2 Optimized Design of the Charge Pump with a Pure Capacitive Load

The design parameters involved in the design of a CP are summarized in Table 7.1 and can be obtained from relationships (7.3), (7.7) and (7.13). The first parameter to be set is the number of stages. However, even if (7.2) relates N and the steady state output voltage in a simple way, it cannot be really used since this value is ideally reached after and infinite time.

From a practical viewpoint, it is useful to analyze the plot in Fig. 7.8, where Q_{Tot} and C_{Tot}, normalized to their minimum values, are plotted versus N. By inspection, it is apparent that two different minima exist. Hence, before starting the design procedure, we have to clearly identify the main design target, in order to use the design approach which allows the chosen performance to be optimized. Two different design strategies can be developed: one minimizes the area (and rise time

[DP1996]), the other minimizes the charge consumption (i.e. the power consumption) during the transient behavior.

Table 7.1 CP design parameters

Parameter	Comment
V_{DD}	Technology dependent
Q_{Tot}	**Not known a priori**
$V_{Out}(t_r)$	Design constraint
t_r	Design constraint
$F=1/T$	Technology dependent
$A_{Tot} \propto C_{Tot}$	**Not known a priori**
N	**Not known a priori**
$\alpha = C_P/C$	Technology dependent

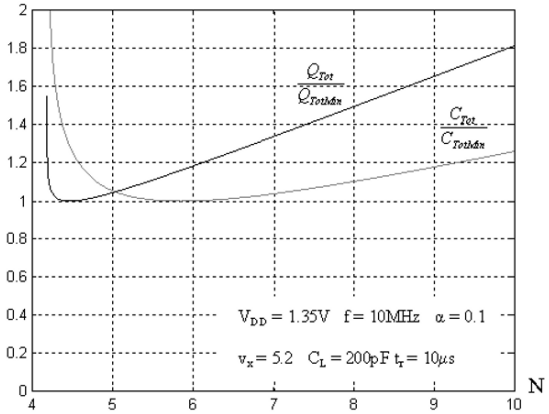

Fig. 7.8 Q_{Tot} and C_{Tot} normalized to their minimum values versus N

7.2.1 Minimizing Area Occupation and Rise Time

To establish the optimum number of stages that minimizes the silicon area we must first evaluate C_{Tot} through (7.7), and set to zero its derivative with respect to N. Similarly, the optimum N that minimizes the rise time is found by directly setting to zero the derivative of (7.7). In both cases we get

$$2\ln\frac{(N+1)-v_{x0}}{(N+1)-v_x}+N\left[\frac{1}{(N+1)-v_{x0}}-\frac{1}{(N+1)-v_x}\right]=0 \tag{7.14}$$

The above expression can be simplified using the empirical approximation (very accurate for x ranging from 0.3 to 1 [PP2006])

$$\ln(x)\approx\frac{2x^2-x-1}{3x} \tag{7.15}$$

And, after some algebraic simplifications (7.14) becomes

$$\frac{(v_x - v_{x0})\left[4v_x + 2v_{x0} - 3(N+2)\right]}{\left[(N+1) - v_x\right]\left[(N+1) - v_{x0}\right]} = 0 \tag{7.16}$$

from which, the optimum N minimizing both the total capacitance and rise time is

$$N_{Aop} = \frac{4}{3}v_x + \frac{2}{3}v_{x0} - 2 \tag{7.17a}$$

and since v_{x0} is often equal to 1, we get

$$N_{Aop} = \frac{4}{3}(v_x - 1) \tag{7.17b}$$

Once defined N_{Aop}, we can use the rise time constraint, given by (7.7), to evaluate the required total pumping capacitance and, hence, the value of C.

7.2.2 Minimizing Charge Consumption

To find the optimum number of stages that minimizes charge consumption, we take the derivative of (7.13) and set it to zero

$$(v_x - v_{x0}) + 2\alpha N \ln\frac{(N+1) - v_{x0}}{(N+1) - v_x} - \alpha N^2 \frac{v_x - v_{x0}}{\left[(N+1) - v_x\right]\left[(N+1) - v_{x0}\right]} = 0 \tag{7.18}$$

To solve (7.18) we again approximate the logarithmic term. We now use the linear approximation which minimizes the error in the range 0–1 [PP2006]

$$\ln(x) \approx 2(x-1) \tag{7.19}$$

Thus (7.18) becomes

$$1 + \frac{4\alpha N}{(N+1) - v_{x0}} - \frac{\alpha N^2}{\left[(N+1) - v_x\right]\left[(N+1) - v_{x0}\right]} = 0 \tag{7.20}$$

or equivalently

$$(1+3\alpha)N^2 - \left[v_x + v_{x0} + 4\alpha(v_x - 1) - 2\right]N + (v_x - 1)(v_{x0} - 1) = 0 \tag{7.21}$$

Since v_{x0} is often equal to 1, the optimum number of stages minimizing charge consumption is expressed by

$$N_{Qop} = \frac{1+4\alpha}{1+3\alpha}(v_x - 1) \tag{7.22}$$

Again, once calculated N_{Qop}, we find the pumping capacitor, C, for the required rise time by using relationship (7.7).

7.2.3 Comparison Between the Optimized Design Strategies

To perform a comparison of the design strategies discussed before, we evaluate the area overhead caused by the minimum power consumption design and the charge consumption overhead caused by the minimum silicon area design [PP2006].

As already stated, the silicon area can be directly derived from the CP total capacitance, hence evaluating (7.7) for each design strategy, we get

$$t_{r,Aop} = T\frac{C_L + C_{Eq}}{C_{T,Aop}}\left[\frac{4}{3}(v_x - 1)\right]^2 \ln 4 \tag{7.23}$$

$$t_{r,Qop} = T\frac{C_L + C_{Eq}}{C_{T,Qop}}\left[\frac{1+4\alpha}{1+3\alpha}(v_x - 1)\right]^2 \ln\left(\frac{1}{\alpha} + 4\right) \tag{7.24}$$

where $C_{T,Aop}$ and $C_{T,Qop}$ are the pumping total capacitances in the cases of area and charge consumption minimization, respectively. Assuming a given rise time to be achieved by both design strategies, we can evaluate, by equating (7.23) and (7.24), the increased total CP capacitance for the optimized power consumption design with respect to the minimum area design. It results to be

$$\frac{C_{T\,Qop} - C_{T\,Aop}}{C_{T\,Aop}} = \left(\frac{3}{4}\frac{1+4\alpha}{1+3\alpha}\right)^2 \frac{\ln\left(\frac{1}{\alpha} + 4\right)}{\ln 4} - 1 \tag{7.25}$$

Relationship (7.25) is a decreasing function of α as can be seen by its plot in Fig. 7.9. It is apparent the area increase of 25% to 5% for α ranging from 0.1 to 0.5.

To compare the charge consumption of the two design strategies, we substitute N from (7.17) and (7.22) into relationship (7.13) (assuming as usual v_{x0} equal to 1), we get

$$Q_{T\,Aop} = \left[\frac{4}{3}(v_x - 1)^2 + \alpha\left(\frac{4}{3}\right)^2 (v_x - 1)^2 \ln 4\right](C_L + C_{Eq})V_{DD} \tag{7.26}$$

for the area minimization design, and

$$Q_{T\,Qop} = \left[\frac{1+4\alpha}{1+3\alpha}\left(v_x - 1\right)^2 + \alpha\left(\frac{1+4\alpha}{1+3\alpha}\right)^2 \left(v_x - 1\right)^2 \ln\left(\frac{1}{\alpha}+4\right)\right]\left(C_L + C_{Eq}\right)\cdot V_{DD} \tag{7.27}$$

for the charge consumption minimization design. Hence, the increase of the charge consumption incurred by the minimum area design is given by

$$\frac{Q_{T\,Aop} - Q_{T\,Qop}}{Q_{T\,Qop}} = \frac{\frac{4}{3}\left(1+\alpha\frac{4}{3}\ln 4\right)}{\frac{1+4\alpha}{1+3\alpha}\left[1+\alpha\frac{1+4\alpha}{1+3\alpha}\ln\left(\frac{1}{\alpha}+4\right)\right]} - 1 \tag{7.28}$$

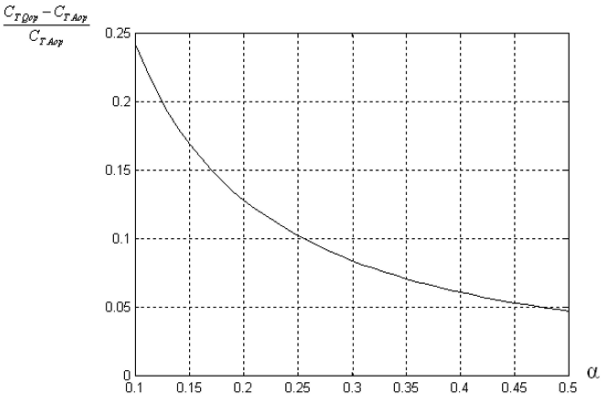

Fig. 7.9 Increase on total CP capacitance (proportional to silicon area) of minimum power consumption design with respect to the minimum area design

By inspection of Fig. 7.10, where relationship (7.28) is plotted, we can see that (7.28) is a decreasing function of α and is always lower than 15% for typical α values.

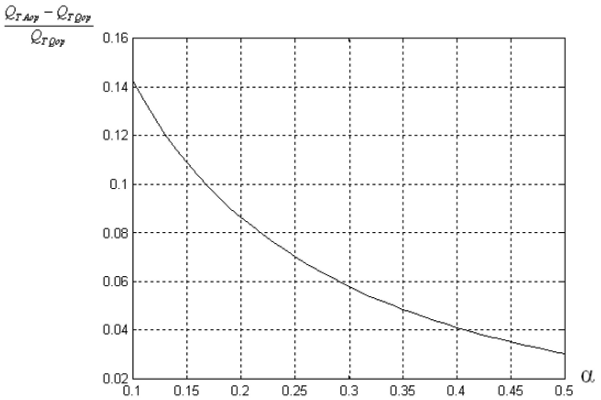

Fig. 7.10 Increase on charge consumption (i.e. power consumption) of minimum area design with respect to minimum consumption design

7.3 Analysis of the Charge Pump with a Current Load

A CP with a current load is shown in Fig. 7.11. In this case, once reached the steady state, the CP has to provide in each time period, T, an amount of charge equal to

$$\Delta Q = I_L \cdot T \tag{7.29}$$

which is constant, assuming constant the current load, I_L. This is also the amount of charge exchanged in each half period (in the steady state) between two adjacent capacitors. More specifically, ΔQ is transferred from the capacitor on the left to the capacitor (or the load) on the right connected in each half period (see Fig. 7.12).

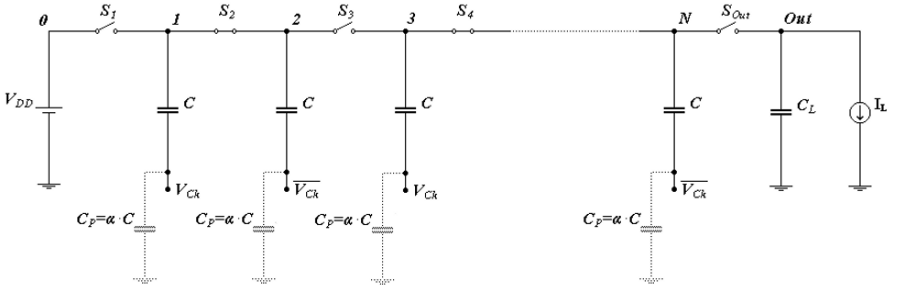

Fig. 7.11 N-stage CP with a current load

The amount of charge ΔQ affects the steady state output voltage, whose average value in each period is

$$V_{Out}\Big|_{Steady\ State} = (N+1) \cdot V_{DD} - N \cdot \frac{I_L \cdot T}{C} \tag{7.30}$$

Consider for example a two-stage CP with a current load, as shown in Fig. 7.12. During the first half period (in the steady state), the first capacitor is connected to the power supply, and is recharged by ΔQ, the same amount provided by the CP to the output. In the next half period, when the first and the second pumping capacitors are connected together, since switch S_2 is closed, they exchange the same amount of charge, ΔQ, and the highest node voltage results to be

$$V_1\Big|_{V_{Ck}=V_{DD}} = V_2\Big|_{\overline{V_{Ck}}=0V} = V_1\Big|_{V_{Ck}=0V} + V_{Ck} - \Delta V = 2 \cdot V_{DD} - \Delta V \tag{7.31}$$

where

$$\Delta V = \frac{\Delta Q}{C} \tag{7.32}$$

Finally, in the subsequent first half period, when the switches S_1 and S_{Out} are closed, the output voltage is

$$V_{Out} = V_2\Big|_{\overline{V_{Ck}}=V_{DD}} = V_2\Big|_{\overline{V_{Ck}}=0V} + V_{Ck} - \Delta V = 3 \cdot V_{DD} - 2\Delta V \tag{7.33}$$

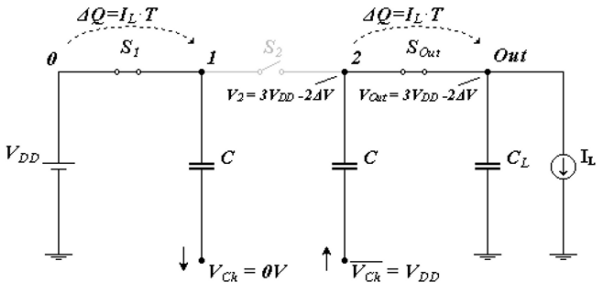

Fig. 7.12 A two-stage CP with a current load

In conclusion, generalizing the analysis for an *N*-stage CP, we write the output voltage

$$V_{Out}\Big|_{Steady\ State} = (N+1) \cdot V_{DD} - N \cdot \Delta V \tag{7.34}$$

and substituting (7.32) and (7.29) we get relationship (7.30).

Carrying out a more detailed analysis by considering the continuous charge transfer from the CP to the output load, we observe that when the output load is not connected to the CP (i.e., when switch S_{Out} is open), the current load discharges the load capacitance by an amount equal to $\Delta Q/2$. An output voltage ripple, V_r, arises, whose amplitude is

$$V_r = \frac{\Delta Q}{C_L} = \frac{I_L \cdot T}{C_L} \tag{7.35}$$

It decreases with C_L and with the clock frequency.

The area of CP with a load current is of course still given by (7.3), but using (7.30) it can also be rewritten as

$$A_{Tot} = k \cdot \frac{N^2}{(N+1) \cdot V_{DD} - V_{Out}} \frac{I_L}{f} \tag{7.36}$$

The current consumption, I_{VDD}, can be divided into two main terms [PPG2002]

$$I_{VDD} = I_{Id} + I_{Par} \tag{7.37}$$

The former, I_{Id}, is related to the ideal CP behavior and the latter, I_{Par}, accounts for the parasitic effects. I_{Id} can be evaluated by considering that the charge amount delivered to the load, ΔQ, and provided by the power supply, is transferred in each period from one capacitor to another, thus it results to be

$$I_{Id} = (N+1) \cdot \frac{\Delta Q}{T} = (N+1) \cdot I_L \tag{7.38}$$

The same result can be achieved by using the transformation factor of the CP. We amplify the power supply of an N+1 factor, and in an ideal case without wasting energy (i.e., transferring all the power taken from the power supply into the output load), the current sunk by the CP is N+1 times higher than the load current.

Neglecting the contribute of the cross conduction currents, which arises when two adjacent switches provide a conductive path during commutation,[1] current I_{Par} is mainly due to the charging and discharging in each time period, T, of the total parasitic capacitance, C_P,

$$I_{Par} = N \frac{C_P V_{DD}}{T} = \alpha C_{Tot} f V_{DD} \tag{7.39}$$

[1]Cross conduction depends on the CP topology and increases with the switching frequency. It sets a limit to the maximum frequency adoptable.

Thus, from (7.38), (7.39) and using (7.30) to express the total pumping capacitance, the current consumption in the steady state is given by

$$I_{VDD} = \left[(N+1) + \alpha \cdot \frac{N^2}{(N+1) \cdot V_{DD} - V_{Out}} \cdot V_{DD} \right] \cdot I_L \tag{7.40}$$

It is worth noting that the current consumption, and hence the power consumption, depends neither on the clock frequency, nor on total CP capacitance, but it is linearly related to the current load, I_L.

7.4 Optimized Design of the Charge Pump with a Current Load

The design parameters involved in the design of a CP with a current load are summarized in Table 7.2. Among the unknown entries (evidenced in bold characters) two can be evaluated by using (7.36) and (7.40).

We can start the CP design by finding parameter N, and as for the design of a CP with a pure capacitive load, we can follow two possible strategies minimizing either the area or power consumption.

As shown in Fig. 7.13 (which exemplifies the case in whch V_{DD}=1.35 V, V_{Out}=5 V, f=10 MHz, α=0.1, and I_L=300 μA) area and current consumption are minimized for different values of N.

Table 7.2 CP design parameters

Parameter	Comment
V_{DD}	Technology dependent
I_{VDD}	**Not known a priori**
V_{Out}	Design constraint
I_{Out}	Design constraint
f=1/T	Technology dependent
$A_{Tot} \propto C_{Tot}$	**Not known a priori**
N	**Not known a priori**
α= C_P/C	Technology dependent

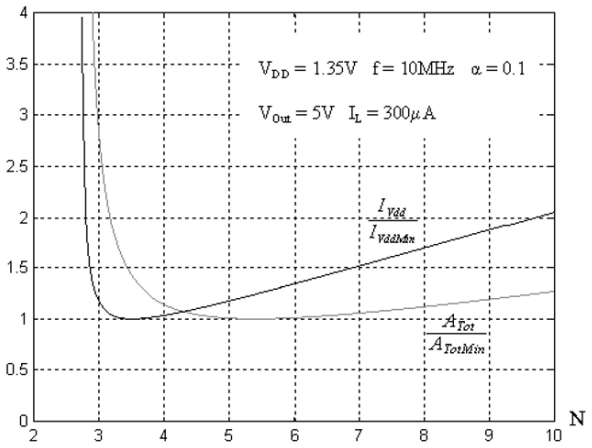

Fig. 7.13 Current consumption and area normalized to their minimum values versus *N*

7.4.1 Minimizing Area Occupation

To find the optimum *N* minimizing the silicon area, we must set to zero the derivative of (7.36) with respect to *N*. On the other hand, if we want to maximize the current provided to the load, we have to set to zero the derivative of current I_L evaluated from (7.30). In both cases, we get

$$\left\{2N \cdot \left[(N+1) \cdot V_{DD} - V_{Out}\right] - N^2 \cdot V_{DD}\right\} \cdot \frac{I_L}{f} = 0 \tag{7.41}$$

which, solved for *N*, gives [TA1999]

$$N_{Aop} = 2 \cdot \left(\frac{V_{Out}}{V_{DD}} - 1\right) \tag{7.42}$$

After solving (7.30) for *C*,

$$C = N \cdot \frac{I_L \cdot T}{(N+1) \cdot V_{DD} - V_{Out}} \tag{7.43}$$

and substituting N_{Aopt} in (7.43), we find the stage capacitance *C*.

7.4.2 Minimizing Current (Power) Consumption

The optimum *N* that minimizes current consumption is obtained by setting to zero the derivative of (7.40) with respect to *N*.

$$1+\alpha\frac{N\cdot\left[\left(N+2\right)\cdot V_{DD}-2\cdot V_{Out}\right]}{\left[\left(N+1\right)\cdot V_{DD}-V_{Out}\right]^2}\cdot V_{DD}=0 \tag{7.44}$$

Hence, solving for N, we get [26]

$$N_{Iop}=\left(1+\sqrt{\frac{\alpha}{1+\alpha}}\right)\cdot\left(\frac{V_{Out}}{V_{DD}}-1\right) \tag{7.45}$$

Finally, substituting the optimum value of (7.45) in (7.42) we get the required value of C for the optimized design.

7.4.3 Comparison Between the Optimized Design Strategies

In order to compare the two considered design strategies, let us start evaluating the increase in area of the minimum power consumption design, compared to the minimum area design [PPG2002].

From (7.43) and using the values N_{Aop} and N_{Iop}, we obtain the CP total capacitance for minimization of area and power consumption, respectively

$$C_{T,Aop}=4\left(\frac{V_{Out}}{V_{DD}}-1\right)\frac{I_L\cdot T}{V_{DD}} \tag{7.46}$$

$$C_{T,Iop}=\frac{\left(1+\sqrt{\frac{\alpha}{1+\alpha}}\right)^2}{\sqrt{\frac{\alpha}{1+\alpha}}}\left(\frac{V_{Out}}{V_{DD}}-1\right)\frac{I_L\cdot T}{V_{DD}} \tag{7.47}$$

From which the increase of area results to be

$$\frac{C_{T\,Iop}-C_{T\,Aop}}{C_{T\,Aop}}=\frac{\left(1+\sqrt{\frac{\alpha}{1+\alpha}}\right)^2}{4\sqrt{\frac{\alpha}{1+\alpha}}}-1 \tag{7.48}$$

Relationship (7.48), plotted in Fig. 7.14, is a decreasing function of α, and it is about equal to 0.4 and 0.2 (i.e. an increase of 40% and 20% in area) for α equal to 0.1 and 0.2, respectively. For α much lower than 0.1 (not plotted), the minimum power consumption strategy requires a huge amount of silicon area.

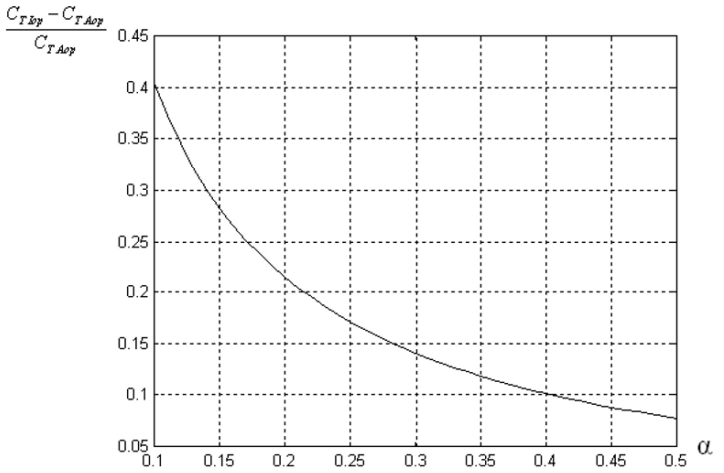

Fig. 7.14 Increment of capacitance (i.e., area) in the case of power consumption optimization with respect the case of area minimization

Let us now evaluate the increase in current consumption incurred by the minimum area design. Substituting (7.42) or (7.45) into (7.40), we find the expression of I_{VDD} for the minimum area and minimum current design strategies

$$I_{VDD,Aop} = \left[2(1+2\alpha)\left(\frac{V_{Out}}{V_{DD}} - 1 \right) + 1 \right] \cdot I_L \tag{7.49}$$

$$I_{VDD,Iop} = \left\{ \left[(1+2\alpha) + 2\sqrt{\alpha+\alpha^2} \right] \left(\frac{V_{Out}}{V_{DD}} - 1 \right) + 1 \right\} \cdot I_L \tag{7.50}$$

The current increase is given by

$$\frac{I_{VDD\ Aop} - I_{VDD\ Iop}}{I_{VDD\ Iop}} = \frac{\left[2(1+2\alpha)\left(\frac{V_{Out}}{V_{DD}} - 1 \right) + 1 \right]}{\left[(1+2\alpha) + 2\sqrt{\alpha+\alpha^2} \right] \left(\frac{V_{Out}}{V_{DD}} - 1 \right) + 1} - 1 \tag{7.51}$$

By inspection of Fig. 7.15, in which (7.51) is plotted, we see that the increment in I_{VDD} is a decreasing function of α and an increasing function of the ratio V_{Out}/V_{DD}. In particular, for an ideal one-stage CP, the current consumption increase is, for the optimum area design, not higher than 20%. On the other hand, for V_{Out}/V_{DD} higher than 4, the current consumption increase is higher than 20% provided that α is lower than 0.15. Similar results that take into consideration CP power efficiency instead of current consumption are found in [PPG2002].

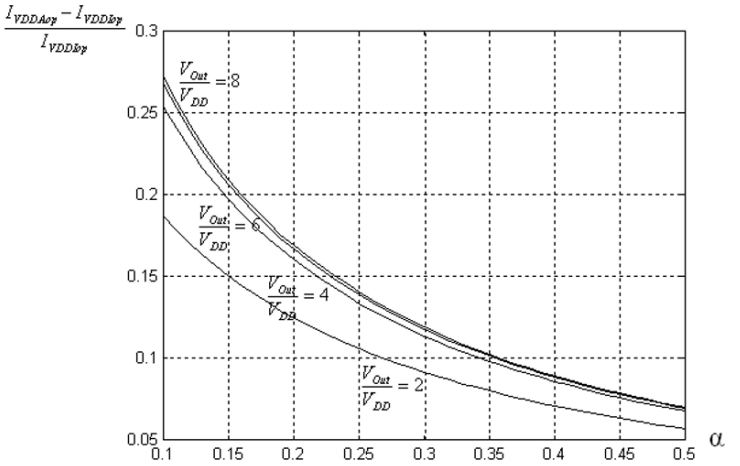

Fig. 7.15 Increment of current consumption (i.e., power consumption) in the case of area minimization with respect the case of minimum current consumption

7.5 Voltages in a CP with a Current Load

7.5.1 Evaluation of Voltages in the Inner Nodes

Since the voltages in the CP nodes are higher than the power supply, to evaluate the voltage stress on each CP component, it is useful to compute the voltage on each CP node and across each switch. At this purpose, let us consider the voltage at the generic node *j*, and analyze its value at the beginning and the end of each half period. Without loss of generality, we can assume that in the first half period the capacitor of the stage *j* (with the clock signal low) is connected together the previous stage through the closed switch S_j,. Hence, during this half period, it shares its charge with the capacitor in the stage (*j*-1).

The voltage at the beginning of this half period is

$$V_{i,start-left-sharing} = j\left(V_{DD} - \Delta V\right) \tag{7.52}$$

and at the end of the half period it is

$$V_{i,end-left-sharing} = j\left(V_{DD} - \Delta V\right) + \Delta V \tag{7.53}$$

During the subsequent half period, when switch S_j is open and switch S_{j+1} is closed, the clock signal driving the stage *j* is high (i.e., there is charge sharing with the capacitor in the stage *j*+1), and the voltage at the beginning of the half period is

$$V_{i,start-right-sharing} = j\left(V_{DD} - \Delta V\right) + \Delta V + V_{DD} \tag{7.54}$$

and at the end of the half period it is

$$V_{i,end-right-sharing} = j\left(V_{DD} - \Delta V\right) + V_{DD} \tag{7.55}$$

7.5.2 Behavior of the Voltages Across the Switches

Let us consider the switch S_j, which interconnects capacitors at nodes j-1 and j, and evaluate the voltage across it, $V_{j,j\text{-}1}=V_j-V_{j\text{-}1}$. This voltage behavior is plotted in Fig. 7.16.

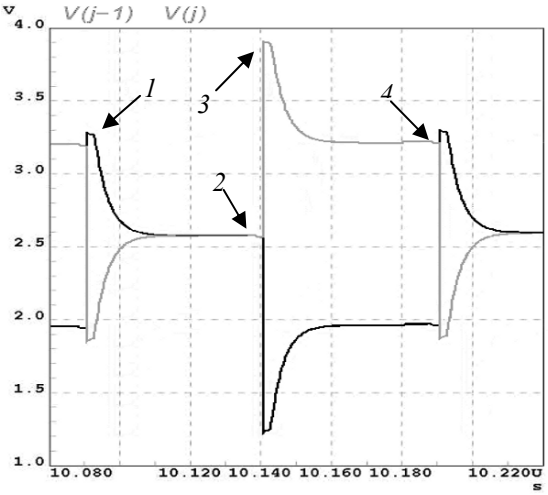

Fig. 7.16 Voltage across switch S_j

At the first half period end S_j is closed and consequently the voltage across the switch is zero (point 2 in Fig. 7.16). At the beginning of the subsequent half period (S_j open) the clock signal changes, and the voltages at nodes j and j-1 fall and rise, respectively, by the clock amplitude. Hence, the voltage across the switch results to be $V_{j,j\text{-}1}=2V_{DD}$ (point 3 in Fig. 7.16). At the end of this half period, the capacitor at node j (j−1) gives (receives) charge ΔQ. Thus, as seen from point 4 in Fig. 7.16, the voltage at node j (j−1) reduces (increases) of ΔV, and $V_{j,j\text{-}1}=2V_{DD}-2\Delta V$. Finally, when S_j is closed again and the charge transfer between capacitors at nodes j-1 and j begins, the clock signal changes, and the voltage across the switch is $V_{j,j\text{-}1}=-2\Delta V$ (point 1 in Fig. 7.16).

These voltage values are equal for all the CP switches, and are summarized in Table 7.3.

It is worth noting that the voltage across the switches depends on the clock amplitude (assumed, as usual, equal to the power supply) and on the voltage step, ΔV, which is given by

$$\Delta V = \frac{(N+1)V_{DD} - V_{Out}}{N} \tag{7.56}$$

After substituting the appropriate N defined for each optimized design strategy in (7.56), we find the ΔV expressions summarized in Table 7.4, that combined with the results in Table 7.3, allow to accurately define the voltage across the switches.

Table 7.3 Switch voltages versus time

Time	Switch voltages $V_{j,j-1}$
Beginning S_j closed	$-2\Delta V$
End S_j closed	0 V
Beginning S_j open	$2V_{DD}$
End S_j open	$2V_{DD}-2\Delta V$

Table 7.4 Expression of ΔV in Table 7.3

CP load	Optimized design	ΔV
Capacitive	*Minimum Area*	$V_{DD}/4$
	Minimum Charge Consumption	$\frac{1+4\alpha}{2+7\alpha}\cdot V_{DD} \cong \frac{V_{DD}}{2}$
Capacitive and Current	*Minimum Area*	$V_{DD}/2$
	Minimum Current Consumption	$\left[\sqrt{\alpha(1+\alpha)}-\alpha\right]\cdot V_{DD}$

7.6 Charge Pump Topologies

In the previous sections we have considered CP with ideal switches. However, real CPs differ substantially for the way in which switches are implemented.

7.6.1 The Dickson Charge Pump

The IC realization of a CP was demonstrated for the first time by Dickson in 1976 [D1976]. Like previous CPs adopted in discrete implementation, such as the Crockcroft and Walton topology proposed in 1932 [CW1932], the **Dickson CP** makes use of diodes instead of switches, as illustrated in Fig. 7.17. A CP topologically similar to the Dickson but implemented with MOS diodes, as shown in Fig. 7.18, was also implemented on silicon [WGM1989].

The main advantage provided by diodes is the absence of the switch control signals. The main drawback is the reduction of the CP output voltage. Indeed, when a diode is forward biased (i.e., when the corresponding switch must be closed), it causes a voltage loss equal to the diode threshold voltage, V_γ, which reduces the output voltage of a factor $(N+1)V_\gamma$.

This reduction is particularly critical under low power supplies, and determines also a loss in the CP power efficiency. For this reason, the Dickson CP is not a practical topology for present applications.

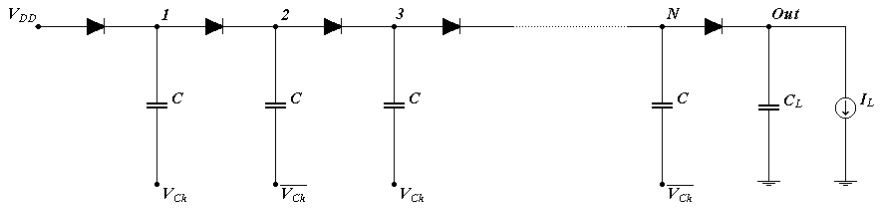

Fig. 7.17 Dickson CP

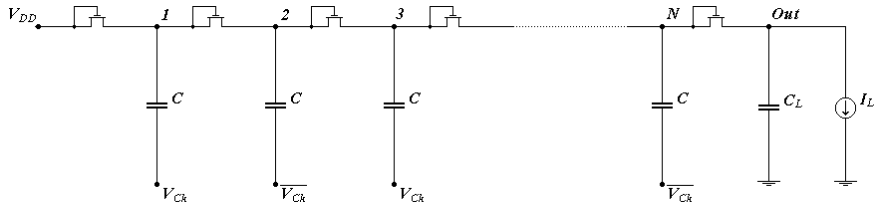

Fig. 7.18 CP with MOS diodes

7.6.2 The Bootstrap Charge Pump

An attractive and widely adopted implementation of the CP switches was presented in [UKA1992], [AKU1994] and is called **bootstrap CP**. The associated CP topology is shown in Fig. 7.19, and the clock signals are plotted in Fig. 7.20.

Even if the implementation of a switch is conceptually simple, for example through a simple MOS transistor (or a transmission gate), in a CP the voltage at the switch terminals are higher than the power supply. As a consequence, the MOS transistors used to implement the CP switches, have to be switched ON by applying suitable gate voltages higher than their source terminal voltages. Specifically, considering the CP in Fig. 7.19, the required high gate voltages are obtained for each stage thanks to a bootstrap circuit, which is realized by adding (for each stage) another capacitor and MOS transistor.

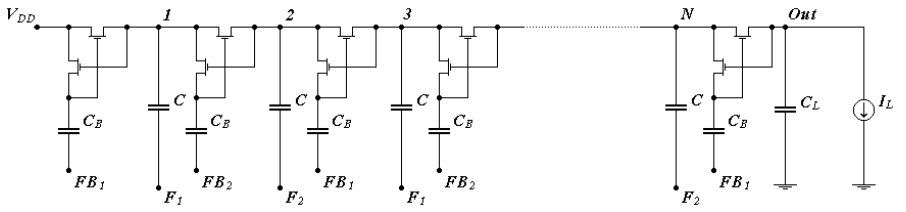

Fig. 7.19 Bootstrap CP

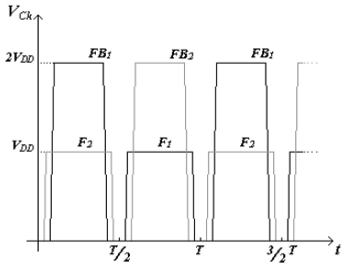

Fig. 7.20 Bootstrap CP clock (F_i) and control (F_{Bi}) signals

To understand the working principle of a bootstrap CP, let us analyze the generic stage (plus a capacitor) depicted in Fig. 7.21.

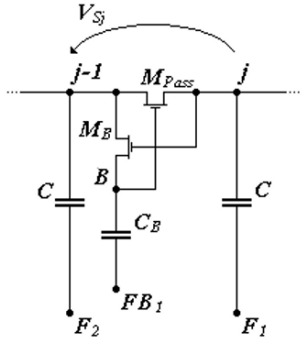

Fig. 7.21 Generic stage (plus a capacitor) of a bootstrap CP

During the half period in which there is no charge transfer (i.e., M_{PASS} is open), signal F_{B1} is low and the added transistor M_B is closed, since the voltage at its gate is higher than a threshold voltage ($V_{GS,MB}$ =2V_{DD}) than the other two nodes. The capacitor C_B is then charged up to a voltage equal to $V_{j\text{-}1}$=(j−1)V_{DD}−(j−2)ΔV, see (7.51).

During the subsequent half period, the clock signals F_1 and F_2 change their value, and after another small time slot (see Fig. 7.20), F_{B1} goes high to 2V_{DD}. Now the transistor M_B is open meanwhile the pass transistor M_{PASS} is closed. Indeed, the gate voltage of M_{PASS} is equal to (j+1)V_{DD}−(j−2)ΔV, which is higher than the voltage at of its source (i.e., the node j) by V_{DD}+2ΔV. Besides, during this half period the gate-source of M_{PASS} is sufficiently high to keep this transistor closed (the gate-source voltage is always not lower than V_{DD}+ΔV).

It is apparent that the ingenious behavior of this topology is obtained at the price of a more complex clocking and control section (requiring four phases and 2V_{DD} amplitude).

7.6.3 Double Charge Pumps

The **double CP** has been conceived to reduce the output ripple by using the same total CP capacitance, C_T. As depicted in Fig. 7.22, each half part, which has a total capacitance $C_T/2$, feeds the load in a different half period [KKJ1996]. Hence, the charge ΔQ pumped at the output is divided into two equal parts, each for half period. The output voltage (7.30) is the same as the simple CP, but the ripple is now

$$V_r = \frac{1}{2}\frac{\Delta Q}{C_L} = \frac{I_L \cdot T}{2 \cdot C_L} \tag{7.57}$$

Of course, by properly implementing the switches we realize a **double Dickson CP** or a **double bootstrap CP**. The latter is shown in Fig. 7.23.

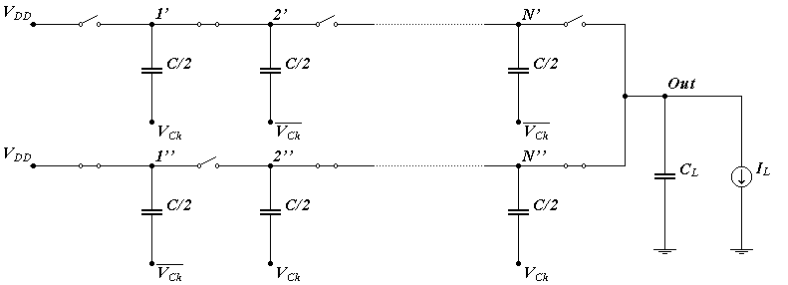

Fig. 7.22 Simplified schematic of a double CP

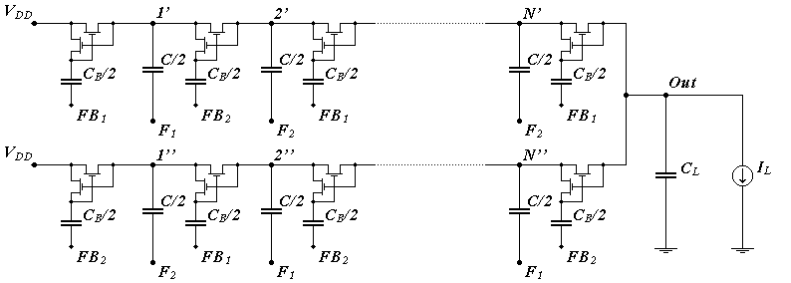

Fig. 7.23 Double bootstrap CP

A very interesting double CP that only recently is gaining popularity, was originally proposed in [GP1994, GP1996], and is shown in Fig. 7.24. This topology, often referred to as **latched CP**, because it includes a latch in each stage, is suited for very high clock frequencies. Indeed, unlike the bootstrap CP, the latched CP needs only a two-phase clock. This topology is suitable for full integration in PMLCD drivers with only C_L as external discrete capacitor.

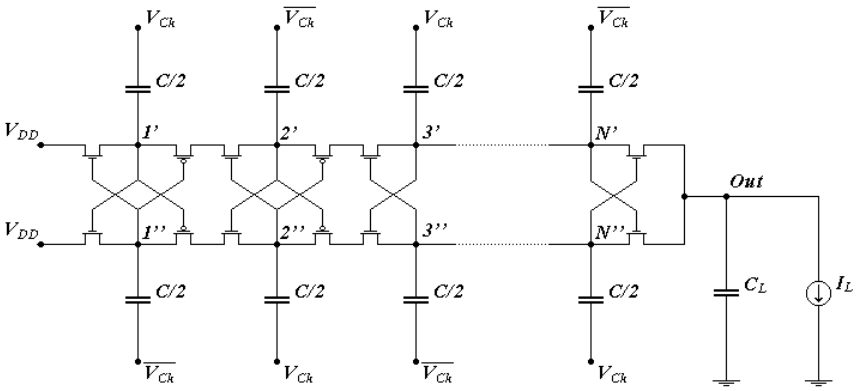

Fig. 7.24 Latched CP

7.6.4 Series-Parallel Charge Pumps

Another topology that reminds those originally adopted for discrete implementations [CW1932], is the **series-parallel CP**. It has been seldom used in an IC implementation [MS1998], since it was believed as inefficient for this use. However, only recently an in-depth analysis to evaluate its suitability for ICs has been carried out [SJO2001, CGT2007].

A two stage series-parallel CP is shown in Fig. 7.25. The peculiarity of this CP is the parallel charging of all the capacitors to the power supply, V_{DD}, during the first half period (i.e., when switches P_i and P_i' are closed and switches S_i are open), and the series connection of all capacitors in the other half period (i.e., when switches P_i and P_i' are open and switches S_i are closed).

The main drawback of this topology is caused by the parasitic capacitances which affect the behavior and performance more than the other topologies. Moreover, another critical aspect concerns the switches implementation.

AMLCDs require higher voltages and higher energy than PMLCDs, therefore the pumping capacitors (other than the C_L) are usually all external. Since this topology has the lowest number of capacitors it is suitable for AMLCD drivers in order to minimize the number of pins.

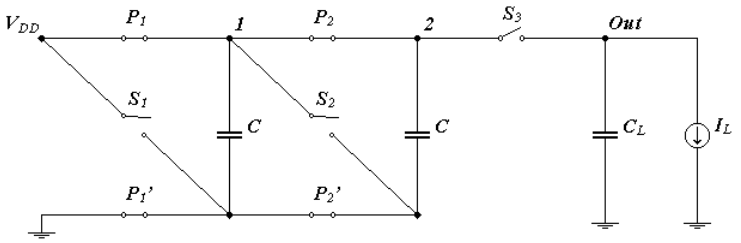

Fig. 7.25 Series-parallel CP

7.6.5 Charge Pumps with Adaptive Number of Stages

In many IC applications more than one CP with different number of stages is required. Thus, when the CPs are used in non overlapping time periods, it can be useful to implement only one CP which dynamically adapts its number of stages. Examples of CPs with adaptive stages are shown in [TTT2002, PPG2006].

More specifically, a solution that switches from a two-stage to a four-stage topology is proposed in [TTT2002]. In [PPG2006], the number of stages is dynamically chosen by rearranging the whole set of capacitors so that the required output voltage could be reached by maximizing the CP's efficiency. Hence, for a defined number of stages, the whole CP capacitance (i.e., silicon area used by the CP) always remains equal.

A version of the topology proposed in [PPG2006], which adapts its number of stages from 1 to 3, is shown in Fig. 7.26. Without loss generality, the topology makes use diodes as switches, but changes can be simply implemented if switches instead of diodes are used.

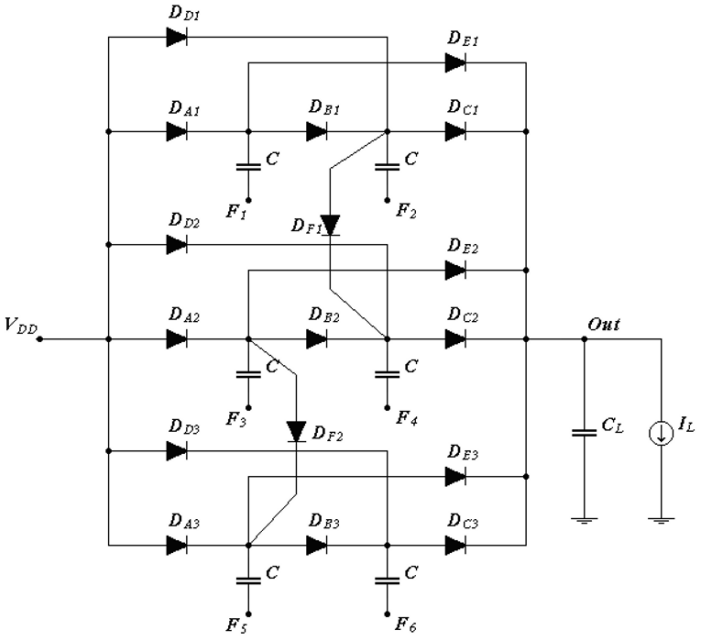

Fig. 7.26 CP with adaptive stages

It is worth noting that to provide adaptability, each capacitor is connected through a diode both to the power supply (D_{Ai} and D_{Di}) and to the output node (D_{Ci} and D_{Ei}). Moreover, there are diodes that connect couple of capacitors (D_{Bi} and D_{Fi}).

To understand the behavior of the CP, let us consider each single case starting from the single-stage one. In this configuration, all the capacitors have to be connected in parallel to form a single capacitor. In other words, this means that all the capacitors have to be driven by the same phase signal and all the diodes connecting couple of capacitors (D_{Bi} and D_{Fi}) are always reverse biased.

In the case in which a two-stage topology is needed, the CP in Fig. 7.26 works like three parallel two-stage topologies. Hence, it can be simply inferred that the set of phases F_1, F_3 and F_5 must be complementary to the other set F_2, F_4 and F_6. Under this condition, the diodes D_{Fi} are always reverse biased. Moreover, since at steady state $V_{2i}>V_{DD}$ and $V_{2i+1}<V_{Out}$, the diodes D_{Di} and D_{Ei} are also reverse biased.

Finally, a three-stage CP can be obtained by configuring the CP like two parallel three-stage CPs. This is obtained by driving the input phases F_1, F_3, F_4 and F_6 together, and the input phases F_2 and F_5 by the complementary phase. Thus, the two three-stage CPs have the two main paths constituted by internal nodes 1, 2 and 4 with the set of phases F_1, F_2 and F_4, and internal nodes 3, 5 and 6 with the set of phases F_3, F_5 and F_6. It can be simply verified that at the steady state the diodes D_{Di}, D_{Ei}, D_{C1}, D_{B2} and D_{A3} are reverse biased.

The phase arrangement for the three cases is summarized in Table 7.5.

Table 7.5 Clock phases for the CP in Fig. 7.26

	One-stage CP	**Two-stage CP**	**Three-stage CP**
FX	$F_1, F_2, F_3, F_4, F_5, F_6$	F_1, F_3, F_5	F_1, F_3, F_4, F_6
FN	-	F_2, F_4, F_6	F_2, F_5

7.7 Concluding Remarks

Following the suggestions of the authors of the book, derived from their own working practice, we report some additional guidelines particularly oriented to the design of charge pumps for LCD drivers.

For those cases in which the charge pump capacitors cannot be fully integrated, the main design target is to minimize the number of external pins required, and hence the number of stages N. Therefore, we cannot follow any of the optimized strategies previously presented. Instead, once fixed the minimum N, we find the capacitors value from (7.30) by using an adequate switching frequency as low as possible to minimize the losses due to cross conduction but avoiding acoustic noise.

On the other hand, when the integration of the charge pump capacitors is possible, as in small size LCD drivers, we could minimize the silicon area as shown in Section 7.4.1. However, in order to reduce also the current consumption (fundamental objective in portable applications), a trade-off between energy consumption and area must be met. This leads to a number of stages value comprised between that deriving from (7.42) (minimum silicon area) and that obtained by minimizing the current consumption. It is worth noting that to evaluate the current consumption, the cross conduction contribute must be included into (7.40) because in general the switching frequency adopted in fully integrated charge pumps is as high as possible. Since cross conduction currents increase with the switching frequency, a good compromise from a practical point of view is to set that particular clock frequency for which the losses due to cross conduction are equal to those due to parasitic capacitances.

Finally, it must be observed that the chapter deals with the charge pump core only. In practical applications this core is embedded within a negative feedback loop (as shown for instance in Fig. 4.12), which allows the regulation of the output

voltage by acting on the switching frequency, thus changing it according to the supply voltage and load values.

References

[AKU1994] S. Atsumi, M. Kuriyama, A. Umezawa, H. Banba, K. Naruke, S. Yamada, Y. Ohshima, M. Oshikiri, Y. Hiura, T. Yamane, and K. Yoshikawa, "A 16-Mb Flash EEPROM with a New Self-Data-Refresh Scheme for a Sector Erase Operation," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 4, pp. 461–468, 1994.

[BN1998] G. den Besten and B. Nauta, "Embedded 5 V-to-3.3 V Voltage Regulator for Supplying Digital IC's in 3.3 V CMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 7, pp. 956–962, 1998.

[CGO1999] P. Cappelletti, C. Golla, P. Olivo, and E. Zanoni, *Flash Memories*, Kluwer Academic Publishers, 1999.

[CGT2007] A. Cabrini, L. Gobbi, and G. Torelli, "Voltage Gain Analysis of Integrated Fibonacci-Like Charge Pumps for Low Power Applications," *IEEE Transactions on Circuits and Systems - Part II*, Vol. 54, No. 11, pp. 929–933, 2007.

[CT1991] R. Castello and L. Tomasini, "1.5-V High-Performance SC Filters in BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 26, No.7, pp. 930–936, 1991.

[CW1932] J. Crockcroft and E. Walton, "Production of High Velocity Positive Ions," *Proceedings of the Royal Society, A,* Vol. 136, pp. 619–630, 1932.

[D1976] J. Dickson, "On-Chip High-Voltage Generation MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE Journal of Solid-State Circuits*, Vol. 11, No. 3, pp. 374–378, 1976.

[DD1998] T. Duisters and E. Dijkmans, "A -90-dB THD Rail-to-Rail Input Opamp Using a New Local Charge Pump in CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 7, pp. 947–955, 1998.

[DP1996] G. Di Cataldo and G. Palumbo, "Optimized Design of an N-th Order Dickson Voltage Multiplier," *IEEE Transactions on Circuits and Systems - Part I*, Vol. 43, No. 5, pp. 414–418, 1996.

[GP1994] R. Gariboldi and F. Pulvirenti, "A Monolithic Quad Line Driver for Industrial Application," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 9, pp. 957–962, 1994.

[GP1996] R. Gariboldi and F. Pulvirenti, "A 70 mΩ Intelligent High Side Switch with Full Diagnostics," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 7, pp. 915–923, 1996.

[H1990] S. Hobrecht, "An Intelligent BiCMOS/DMOS Quad 1-A High-Side Switch," *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 6, pp. 1395–1402, 1990.

[IOS2001] T. Ishii, K. Oshima, H. Sato, T. Yoshitake, A. Sato, S. Kubono, K. Manita, T. Nakayama, and A. Hosogane, "A 126.6-mm^2 AND-Type 512-Mb Flash Memory with 1.8-V Power Supply," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 11, pp. 1707–1711, 2001.

[JNH1992] T. Jinbo, H. Nakata, K. Hashimoto, T. Watanabe, K. Ninomiya, T. Urai, M. Koike, T. Sato, N. Kodama, K. Oyama, and T. Okazawa, "A 5-V-Only 16-

Mb Flash Memory with Sector Erase Mode," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 11, pp. 1547–1553, 1992.

[KKJ1996] G T. Kawahara, T. Kobayashi, Y. Jyouno, S.-I. Saeki, N. Miyamoto, T. Adachi, M. Kato, A. Sato, J. Yugami, H. Kume, and K. Kimura, "Bit-Line Clamped Sensing Multiplex and Accurate High Voltage Generator for Quarter-Micron Flash Memories," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 11, pp. 1590–1599, 1996.

[MC2001] K.-S. Min and J.-Y. Chung, "A Fast Pump-Down V_{BB} Generator for Sub-1.5-V DRAMs," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 7, pp. 1154–1157, 2001.

[MS1998] H. Morimura and N. Shibata, "A Step-Down Boosted-Wordline Scheme for 1-V Battery-Operated Fast SRAM's," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 8, pp. 1220–1227, 1998.

[NGN2001] A. Novo, A. Gerosa, and A. Neviani, "A Sub-Micron CMOS Programmable CP for Implantable Pacemaker," *Analog Integrated Circuits and Signal Processing*, Vol. 27, No. 3, pp. 209–215, 2001.

[PBB2000] G. Palumbo, N. Barniol, and M. Bethaoui, "Improved Behavioral and Design Model of an N-th Order Charge Pump," *IEEE Transactions on Circuits and Systems - Part I*, Vol. 47, No. 2, pp. 264–268, 2000.

[PP2006] G. Palumbo and D. Pappalardo, "Charge Pump Circuits with only Capacitive Loads: Optimized Design," *IEEE Transaction on Circuits and Systems - Part II*, Vol. 53, No. 2, pp. 128–132, February 2006.

[PPG2002] G. Palumbo, D. Pappalardo, M. Gaibotti, "Charge Pump Circuits: Power Consumption Optimization," *IEEE Transactions on Circuits and Systems - Part I*, Vol. 49, No. 11, pp. 1535–1542, 2002.

[PPG2006] G. Palumbo, D. Pappalardo, and M. Gaibotti, "Charge Pump with Adaptive Stages for Non-Volatile Memories," *IEEE Proceedings of Circuits, Devices and Systems*, Vol. 153, No. 2, pp. 136–142, 2006.

[SJO2001] J. Starzyk, Y. Jan, and F. Oiu, "A DC-DC Charge Pump Design Based on Voltage Doublers," *IEEE Transactions on Circuits and Systems - Part I*, Vol. 48, No. 3, pp. 350–359, 2001.

[SK2008] F. Su and W.-H. Ki, "Component-Efficient Multiphase Switched-Capacitor DC-DC Converter with Configurable Conversion Ratios for LCD Driver Applications," *IEEE Transaction On Circuits and Systems - Part II*, Vol. 55, No. 8, pp. 753–757, 2008.

[TA1999] T. Tanzawa and S. Atsumi, "Optimization of Word-Line Booster Circuits for Low-Voltage Flash Memories," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 8, pp. 1091–1098, 1999.

[TT1997] T. Tanzawa and T. Tanaka, "A Dynamic Analysis of the Dickson Charge Pump Circuit," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 8, pp. 1231–1240, 1997.

[TTT2002] T. Tanzawa, T. Tanaka, K. Takeuchi, and H. Nakamura, "Circuit Techniques for a 1.8-V-Only NAND Flash Memory," *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 1, pp. 84–89, 2002.

[UKA1992] A. Umezawa, M. Kuriyama, S. Atsumi, H. Banba, K. Imamiya, K. Naruke, S. Yamada, E. Obi, M. Oshikiri, T. Suzuki, M. Wada, and S. Tanaka, "A 5-V-Only Operation 0.6-μm Flash EEPROM with Row Decoder Scheme in Triple-Well Structure," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 11, pp. 1540–1545, 1992.

[WGM1989] J. Witters, G. Groeseneken, and H. Maes, "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 5, pp. 1372–1380, 1989.

[WVK1992] S.L. Wong, S. Venkitasubrahmanian, M.J. Kim, and J.C. Young, "Design of a 60-V 10-A Intelligent Power Switch Using Standard Cells," *IEEE Journal of Solid-State Circuits*, Vol. SC-27, No. 3, pp. 429–432, 1992.

[YKC2003] T.-R. Ying, W.-H. Ki, and M. Chan, "Area-efficient CMOS Charge Pumps for LCD drivers," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 10, pp. 1721–1725, 2003.

[ZLD2001] M. Zhang, N. Llaser, and F. Devos, "Multi-Value Voltage-to-Voltage Converter Using a Multi-Stage Symmetrical Charge Pump for On-Chip EEPROM Programming," *Analog Integrated Circuits and Signal Processing*, Vol. 27, No. 1–2, pp. 85–95, 2001.