Chapter 5

Active Matrix LCDs and Their Addressing Techniques

We have seen that in PMLCDs the display contrast depends on the drive margin, but this parameter is in turn a function of the number of rows so that the more rows are added, the less contrast is obtained. **Active matrix LCDs** (**AMLCDs**, also called **TFT LCDs**) remove these multiplexing limitations by exploiting a switching element and a storage capacitor at every pixel of the display. These switches are usually implemented through transistors made up of deposited thin films, and are therefore called thin-film transistors,[1] TFTs. A TFT at each pixel allows the column voltages to be applied only to the row that is being addressed, while the storage capacitor maintains the pixel information for the whole frame also when the addressing signal is removed. Therefore, a high contrast is possible and a fast LC mixture can be used, since the pixel no longer has to respond to the average voltage over a whole frame period, as in PMLCDs. For the same reason the phenomenon of crosstalk is also minimized.

AMLCDs are hence suitable for full-motion video, requiring time responses below 20 ms. As main drawbacks, the TFT process increases production costs (at this purpose, a limit in the number of masks of the TFT process is from 4 to 6), reduces the yield and decreases the aperture ratio of the pixel: thus, to maintain an acceptable display luminance a brighter backlight is needed (by increasing power consumption).

In this chapter, after briefly describing the principal TFT devices and the structure of an AMLCD panel, addressing techniques for AMLCDs will be discussed. Related driver ICs and their implementation issues will be treated in Chapter 6.

[1]The majority of AMLCDs use TFTs as switching devices. An alternative commercially exploited solution is constituted by the Metal-Insulator-Metal (MIM) diode. The MIM low fabrication temperature is compatible with plastic substrates.

D.J.R. Cristaldi et al., *Liquid Crystal Display Drivers*, DOI 10.1007/978-90-481-2255-4_5,

5.1 Thin Film Transistors

In this section we will discuss the main characteristics of TFTs. Compared to conventional Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) implemented in a crystalline Si substrate, TFTs have similar model equations but, due to the reduced carrier mobility, μ, they exhibit poorer performance both in terms of conductance and switching speed. Being implemented on an insulating substrate, TFTs lack the substrate electrode (called Body or Bulk in conventional MOSFET devices), and have thus only three terminals named **Drain** (D), **Gate** (G), and **Source** (S). The presence of the insulating substrate provides ideal isolation of each device and negligible parasitic capacitances [LLB1992].

Figure 5.1 shows the cross section and top view of a basic[2] TFT (with the layers materials typically adopted) along with the circuit symbol. The gate-source voltage, v_{GS}, determines the TFT ON/OFF condition as it causes the formation of the conducting **channel** between the source and the drain (i.e., charges are induced in the semiconductor layer).

One type of TFT, the *n*-channel TFT, operates similarly to the *n*-channel MOSFET. In particular, we define the threshold voltage (whose typical value is about 1–4 V) as

$$V_{TH} = -qn_0 d_{CH} / C_{ox} \tag{5.1}$$

where q is the charge of the electron, n_0 is the charge density in the channel, d_{CH} is the channel thickness and C_{ox} is the capacitance of the gate dielectric per unit area ($C_{ox} = \varepsilon_0 \varepsilon_r / t_g$, where t_g is the thickness of the gate dielectric, see Fig. 5.1). The channel is formed if $v_{GS} > V_{TH}$, in this case the TFT is turned on and a current, i_D, can flow through the source and drain terminals, provided that a drain-source voltage, v_{DS}, is applied. Conversely, $i_D = 0$ if $v_{GS} \le V_{TH}$.

Assume now $v_{GS} > V_{TH}$. Denoting as W and L the channel width and length, respectively (as shown in Fig. 5.1), we can write the expression of the drain current as a function of the gate-source and drain-source voltages both in the triode and saturation operating conditions [S2006, MK2003].

The **triode region** (also termed the **linear** region) is characterized by $v_{DS} \le v_{GS} - V_{TH}$ and the drain current expression is

$$i_D = \mu C_{ox} \frac{W}{L} \left[\left(v_{GS} - V_{TH} \right) v_{DS} - \frac{v_{DS}^2}{2} \right] \tag{5.2}$$

In this region, one of the most important parameters is the ON resistance offered by the TFT between the source and drain (when used as a switch), whose expression is

[2]The device depicted in Fig. 5.1 is a "bottom-gate" (or inverted staggered) TFT implemented in either amorphous silicon or polysilicon. Other alternatives are possible; see for instance [B2005, K2004].

$$R_{ON} = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} = \frac{1}{\mu C_{ox} \frac{W}{L} \left(v_{GS} - V_{TH} \right)} \tag{5.3}$$

The above relation shows that the TFT conductivity is increased by increasing the **aspect ratio**, W/L, and/or the **overdrive voltage** $v_{GS}-V_{TH}$.

In the **saturation region** we have $v_{DS} > v_{GS} - V_{TH}$ and the drain current is dependent to a first approximation only on v_{GS} (we will see that this assumption is not accurate in polysilicon TFTs, due to the so called *kink* effect)

$$i_D = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(v_{GS} - V_{TH} \right)^2 \tag{5.4}$$

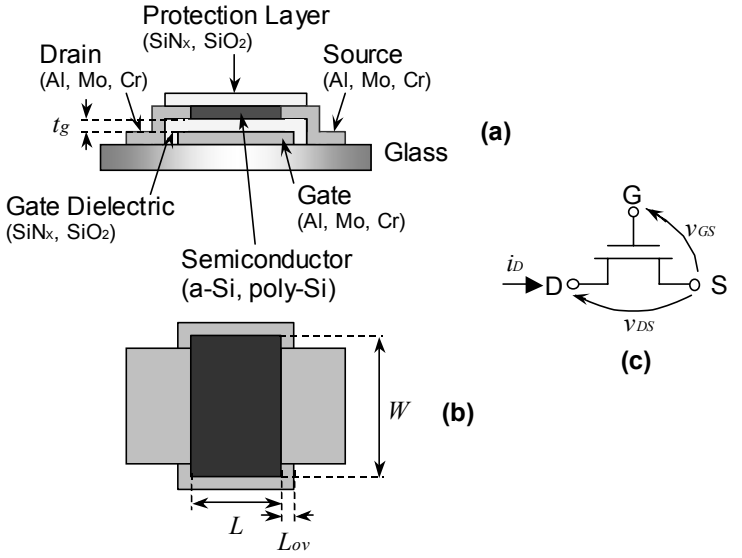


Fig. 5.1 Basic TFT: cross section (**a**), top view (**b**) and circuit symbol (**c**)

The output characteristics derived form (5.2) and (5.4) with v_{GS} as a parameter (and normalized to the factor $\mu C_{ox} W/L$), are plotted in Fig. 5.2. The transition region between the triode and saturation region (for $v_{DS} = v_{GS}-V_{TH}$) is represented by the dashed portion of a parabola whose equation is

$$i_D = \frac{\mu C_{ox}}{2} \frac{W}{L} v_{DS}^2 \tag{5.5}$$

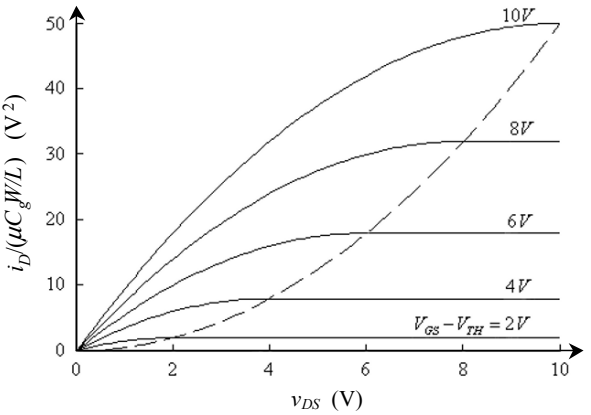


Fig. 5.2 Output characteristics (drain current versus drain-source voltage) of a generic TFT for $V_{GS} - V_{TH}$ = 2, 4, 6, 8, 10 V

Ideally, i_D is equal to zero when $v_{GS} < V_{TH}$, in realty a **leakage conduction** is always present. Therefore, an important aspect regarding TFT addressing is the proper minimization of this current. Indeed, when the pixel is not selected, a high leakage current discharging the storage capacitor leads to a loss of information, but a larger storage capacitor results in a lower aperture-ratio and in a slowdown of the charging time.

Other important parameters for the dynamic behavior of a TFT are the **parasitic capacitances** between couples of terminals, C_{GS}, C_{GD} and C_{DS}. In particular, the gate-drain capacitance (or equivalently the gate-source capacitance, because these capacitances are equal in a transistor operating in triode) has two main contributions: one is due to the channel capacitance, the other is caused by the overlap region between the gate and drain. Assuming v_{DS} small in triode region, about half of the channel capacitance contributes to C_{GD} and the other half to C_{GS}. If the length of the overlap is labeled as L_{OV} (see Fig. 5.1) the expressions of maximum and minimum (when the TFT is near the cutoff region) of C_{GD} are

$$C_{GD,\max} = W(L/2 + L_{OV})C_{ox} \tag{5.6a}$$

$$C_{GD,\min} = WL_{OV}C_{ox} \tag{5.6b}$$

We will show in Section 5.3 that C_{GD} is the origin of performance degradation as it causes unwanted charge redistribution effects.

The above equations are useful for pencil-and-paper calculations. Circuit designers need more accurate but efficient models (time-domain simulations of a complete panel may be an onerous task in terms of required CPU time) to be used in their simulators (SPICE-like models are the most popular) [HS1989, SSJ1997].

5.1.1 a-Si TFT

The most common semiconductor layer used for the integration of TFTs on glass substrates is realized with idrogenated **amorphous silicon** (a-Si:H, in the following a-Si for simplicity). It allows large-area fabrication in a low-temperature process (300°C–400°C) and is the dominant technology in computer and television LCDs. The main difference between a-Si TFT and a conventional Si MOSFET is the lower electron mobility (in the range of 0.2–1.5 cm²/Vs, while it is greater than 1800 cm²/Vs in crystalline Si), due to the presence of electron traps in amorphous silicon. Hence, a-Si TFTs are inadequate to be used in analog and high-speed digital processing directly on glass, but they are instead suitable for the implementation of ON/OFF pixel switches with refresh frequencies around 60 Hz. However, even for this simple scope, the low mobility would require extremely large aspect ratios, thereby reducing the **aperture-ratio** (i.e., only a portion of the pixel's area is transparent to light when the pixel is ON) and ultimately decreasing the display's brightness and contrast. To mitigate this problem, since the transconductance depends also on the gate-source overdrive, the gate of a TFT is driven by a high voltage, typically around 20 V.

Because a-Si materials exhibit poor stability and their structure can be modified by strong illumination and charge carrier injections (in particular its OFF current increases with incident light), the a-Si TFT must be shielded from light. Besides, this technology allows only *n*-channel TFTs to be realized. The conductivity of a-Si *p*-channel TFTs would not be sufficiently high, even as switches for LCDs.

Another disadvantage of a-Si TFTs is the **threshold voltage shift** (by several volts over a few hours with a DC voltage stress [GW2001, KNH2004]). It can be expressed by $\Delta V_{TH}(t) = A(V_{G,ST} - V_{TH,i})t^{\beta}$, where A and β are two temperature dependent parameters, $V_{G,ST}$ is the stress gate voltage and $V_{TH,i}$ is the threshold voltage before stress which has duration t [PBH1989]. It is caused by two mechanisms. At higher gate electric fields, electrons are injected into the gate dielectric [P1983, PD1993]; at lower electric fields, charges are trapped in the interface a-Si and gates [HMM1986]. The threshold voltage increase is larger for lower temperature processes [GW2001]. The shift is not a severe problem for switch operations, but the function of digital circuits is impaired when the static noise margin decreases considerably (becoming zero when V_{TH} increases to $V_{DD}/2$) [LVS2006]. The shift has different polarity for ON and OFF state, therefore a partial cancellation occurs. In any case, a practical driving scheme must take into account a threshold tolerance in the TFTs.

5.1.2 Poly-Si TFT

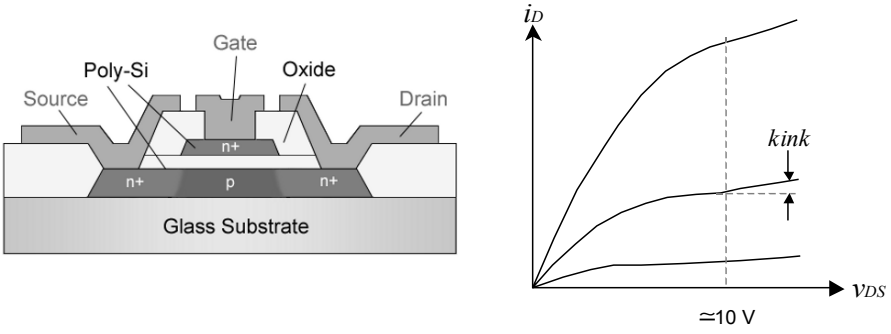
Polysilicon represents an alternative material appropriate to realize the TFT silicon layer, adopted in recent years for small-area displays. It is a silicon-based material, which contains numerous Si grains with sizes ranging from 0.1 to several microns. In semiconductor manufacturing, polysilicon is usually deposited as amorphous films by LPCVD (Low Pressure Chemical Vapor Deposition) and then crystallized by laser annealing above 900°C. This technology requires also expensive quartz substrates. The same approach cannot be exploited by the LCD industry since the strain temperature of glass is only about 650°C. **Low Temperature Polysilicon**

(**LTPS**) technologies, built on low-cost glass, were then developed based on either excimer laser annealing or by combined solid state phase crystallization [H1986, TDM1999, MS1999, JSH1996].

The preparation of LTPS film is more complicated than a-Si, and LTPS is more exposed to process variations over the substrate area. However, LTPS TFTs have a higher mobility than a-Si TFT (up to two orders of magnitude for electrons, 30 to 400 cm²/Vs, and up to 150 cm²/Vs for holes) and the implementation of both *n*-channel and *p*-channel transistors is possible, therefore they allow to increase the pixel aperture ratio (higher mobility means smaller TFT area for a given transconductance) and are suitable for the integration of CMOS-like circuits directly on the glass substrate (ultimately leading to a complete System on Glass, SOG). The latter is a remarkable advantage that allows the number of electrical connections on the LCD panel to be drastically reduced, thereby increasing reliability and compactness. The connections are made in the thin film technology using a mask which is in any case needed for processing the display.

A schematic cross section of a poly-Si TFT is shown in Fig. 5.3a. For high drain-source voltages, poly-Si TFTs exhibit the so called **kink** effect consisting in an anomalous increase of the drain current, as illustrated in Fig. 5.3b. This effect is mainly originated by the high voltage at the drain end of the channel that accelerates charges causing in turn an avalanche current (impact ionization). This current is able to flow to ground in monocristalline Si ICs, being the body electrically connected to a bias voltage. For TFTs the substrate is insulating glass, therefore this current increases the drain current. Of course, to contrast this problem, low supply voltages should be adopted. A Lateral Body Terminal (i.e., the extension of the channel area serving as collector of the charges) was also employed [Y1999].

Recently, Sharp in conjunction with Semiconductor Energy Laboratory Co. Ltd., has developed a process called **Continuous Grain Silicon** (CG Silicon), a further evolution of the LTPS technology, leading to the commercial introduction of high-resolution, high-definition system LCDs for mobile terminal devices in 2002. A complete CPU on a glass substrate is shown in Fig. 5.4 [N2003].



(a) (b)

Fig. 5.3 Poly-Si TFT, (**a**) cross section and (**b**) drain current versus drain-source voltage putting in evidence the kink effect

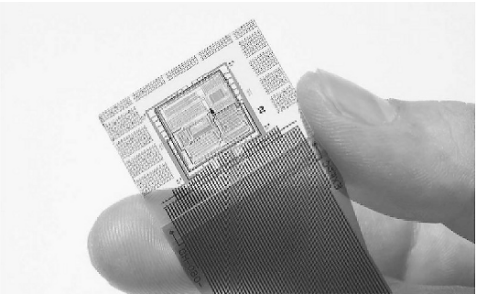


Fig. 5.4 CG Silicon CPU formed on a glass substrate (Semiconductor Energy Laboratory) [N2003]

5.1.3 Further Comparison of a-Si and Poly-Si TFT Performance

Figure 5.5 shows the a-Si and poly-Si TFT characteristics for V_{DS} = 5 V. The poly-Si TFT size is only 1/10 of its a-Si counterpart, to provide the same drain current corresponding to V_{GS} = 20V. The smaller size of transistors (in consequence of the greater mobility electron) can increase both resolution (pixels per inch) and aperture-ratio improving the image definition. For this reason and for the large process tolerances of poly-Si, displays with a high pixel density and pixel size of 15 µm×15 µm are best addressed by poly-Si TFTs. Application of this kind are small high-definition displays for view finders in camcorder, or projection displays [B2005].

Compared to a-Si TFTs, poly-Si TFTs exhibit higher OFF currents, caused by the electric field at the highly doped drain and the imperfect crystalline structure of the poly-Si material. Methods currently adopted against this limitation are the dual gate structure or adding another process step to realize a lightly doped drain (LDD) [L2001].

From the driving voltage point of view, a negative gate-source voltage around –5 to –8 V (not just 0 V) is adopted for a minimum leakage condition below 10 pA. On the other hand, to compensate for the low electron mobility the gate-source voltage is set at around 20 V for switch-on, to provide a drain current in the order of 100 µA.

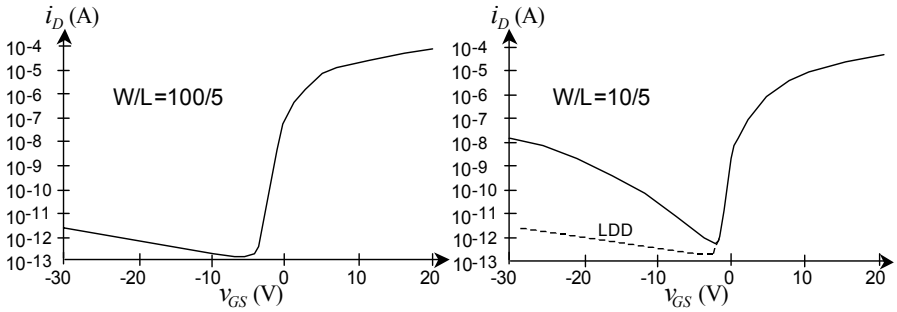


Fig. 5.5 Drain current versus gate-source voltage for an n-channel TFT: (**a**) a-Si TFT with W/L=100 µm/5 µm and (**b**) poly-Si with W/L=10 µm/5 µm. Voltage V_{DS} is 5 V in both cases. The *dashed curve* in (b) represents the OFF current obtained with lightly doped drain (LDD) technology

5.2 Structure of an AMLCD Panel

Like a passive-matrix color LCD, an AMLCD has a sandwich-like structure with liquid crystal filled between two glass plates kept to a controlled distance by spacers and exploits backlight, polarizers and color filters (the latter fitting the upper substrate). The cross section of an AMLCD is shown in Fig. 5.6.

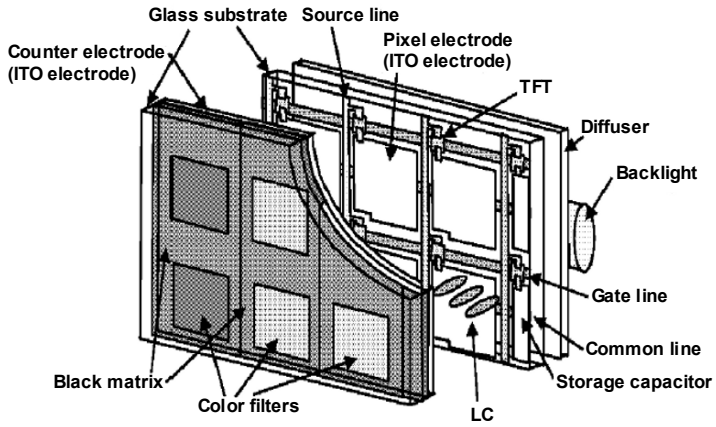


Fig. 5.6 Cross section of an AMLCD [U2006]

Each pixel of a color panel is subdivided into three RGB subpixels. TFTs are integrated on the back glass substrate, along with storage capacitors, ITO electrodes and interconnect wiring, as shown in Fig. 5.7a. In an AMLCD panel, the row and column electrodes are called gate and source electrodes (with reference to the associated TFT terminals). By scanning the gate lines sequentially, and by applying signal voltages to all source lines in parallel, we can address all pixels. As a result, the addressing of an AMLCD is very simple and performed line by line. Unlike passive-matrix addressing which required orthogonal row and column signals, the use of TFTs in AMLCDs makes each row independent from the others. Indeed, the thin-film storage capacitor (C_S), accessed through the associated TFT, memorizes the source (pixel data) voltage and maintains it even after the gate (selection) signal is removed. Note that C_S is added in parallel to the intrinsic LC capacitor, as the value of C_{LC} is too low for adequate charge retention. Between the color filters is placed a **black matrix**, made of an opaque metal, such as chromium (Cr), which shields the (a-Si) TFTs from room light and prevents light leakage between pixels to minimize photo-generated leakage currents in the TFTs. A double layer of Cr and CrOx is used to minimize reflection from the black matrix.

Figure 5.7b shows the electrical model of a subpixel with the storage capacitor C_S in parallel to C_{LC} connected as a load of the TFT. It is worth noting that C_S can be connected either to an adjacent gate line (**Cap-on-Gate**) or to a dedicated common storage bus (**Cap-on-Common**), see Fig. 5.7b, c. As main drawbacks, the former solution increases the capacitive load seen by the gate drivers while the latter

reduces the pixel aperture.[3] The former approach is thus unsuitable for panels with a diagonal size larger than about 20 in.

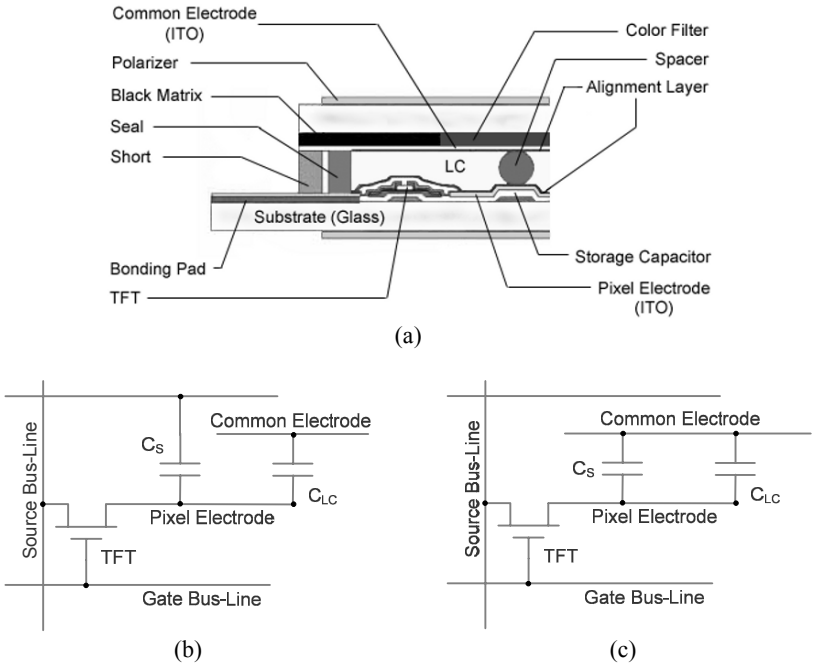


Fig. 5.7 Cross section of a subpixel in an AMLCD panel (**a**) equivalent circuits in Cap-on-Gate structure and (**b**) in Cap-on-Common structure (**c**)

In the unit cell, as shown in Fig. 5.8, TFT electrodes, storage-capacitor electrodes, signal bus-lines, and the black-matrix material constitute opaque areas. The combined areas of these elements, along with the area of the pixel aperture through which light can pass, determine the **aperture ratio** of the pixel: the aperture ratio is given by the area of the pixel aperture divided by the total pixel area (aperture area plus the area of the opaque elements). To increase this value as much as possible, the size of the opaque elements must be made as small as possible, while maintaining a design that maximizes the size of the pixel-electrode area. The Source Line (ITO) overlaps the bottom plate of the storage capacitor and the Gate Line at each pixel in the same column. These overlapping areas cause coupling capacitances.

A complete view of the TFT, C_S and C_{LC} is provided in Fig. 5.9a. The relative areas of C_S and C_{LC} are clearly evidenced. A top view showing the RGB color filters is depicted in Fig. 5.9b.

[3]To increase the pixel luminance for outdoor use, the opaque electrode of C_S can be covered with a reflective material, as suggested in [FNK2003].

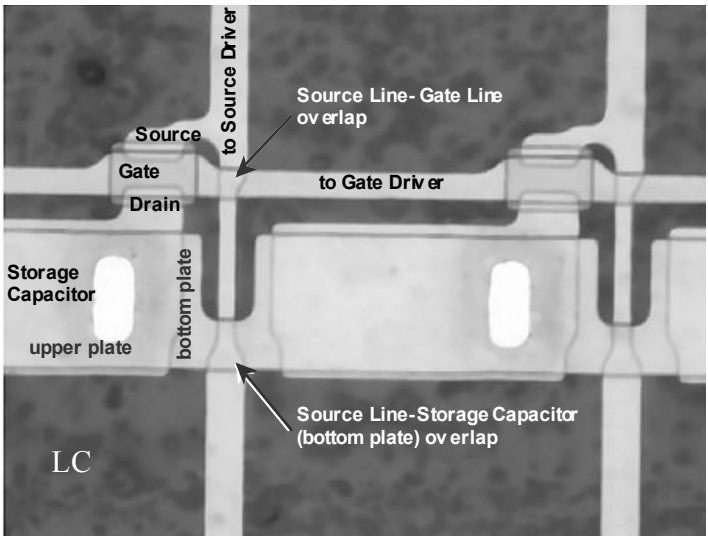
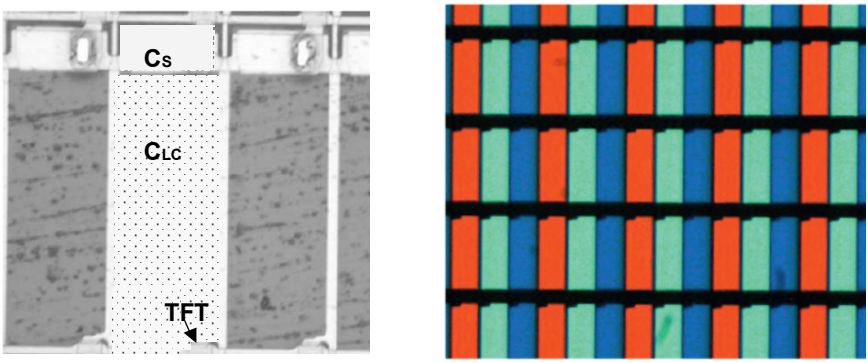


Fig. 5.8 Micrograph of an AMLCD panel showing the TFT, Storage Capacitor and interconnections



(a) (b)

Fig. 5.9 AMLCD panel micrographs: (**a**) detail of the pixel capacitances (*bottom view*); Fig.5.8 is a magnified version of this figure. (**b**) detail of the RGB color filters (*top view*)

5.3 General Considerations

In contrast to PMLCDs that need some form of elaboration technique (such as PWM and/or FRC) for gray level generation, AMLCDs are inherently designed to produce gray levels depending on the voltage magnitude applied to the pixel from the source line. With reference to Fig. 5.7, applying a suitable positive pulse voltage through a specific gate line has the effect of turning on all the TFTs whose gates are connected to that bus line. Capacitors C_{LC} and C_S are then charged at the voltage level applied through the (data) source line. This charged state (and consequently the pixel voltage

level) can be maintained as the gate voltage goes to a negative value, at which time the TFTs nominally turn off. The main function of C_S is then to maintain the voltage on the pixel electrode until the next source voltage is applied. An example of AMLCD addressing waveforms is illustrated in Fig. 5.10.

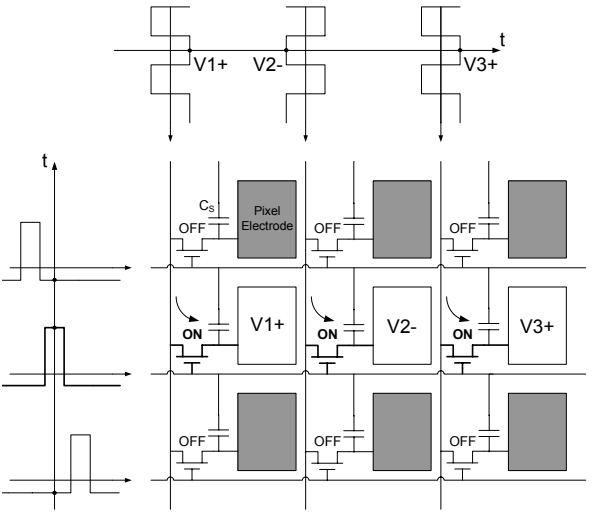


Fig. 5.10 Addressing example of an Active Matrix LCD

As already discussed, the scanning frequency should be at least 30 Hz to avoid flickering. A refresh frequency of 60 Hz is the result of a trade-off between elimination of flicker and low power dissipation. If $f_F = 1/T_F$ is the frame (scanning) frequency and N is the number of rows of display, the maximum access time to pixel (row time), T_R, will be:

$$T_R = \frac{T_F}{N} \tag{5.7}$$

When switched on, the resistance offered by the TFT, R_{ON}, should be adequate to charge the pixel capacitance at the maximum source line voltage within the row time. The ON time constant guaranteeing that, within $0.5T_R$, the voltage stored on C_S is only 1% below the desired value is given by (we consider that the source line voltage polarity is inverted in two consecutive addressing of the same pixel):

$$R_{ON}(C_S + C_{LC}) \le \frac{T_R}{2\ln(2\cdot 100)} = \frac{T_R}{10.6} \tag{5.8}$$

On the other hand, from (5.3), the expression of R_{ON} is

$$R_{ON} = \frac{1}{\mu C_g \frac{W}{L}\left(v_G - v_{DATA} - V_{TH}\right)} \tag{5.9}$$

where the TFT is assumed in the triode region. To ensure this, voltage v_G is made quite high, and v_{DS} is small, being zero at the steady state (i.e., no current flows in the TFT at the steady state). Hence, from (5.8) and (5.9) we find the minimum aspect ratio W/L of the TFT

$$\frac{W}{L} \geq \frac{1}{\mu C_g \left(v_G - v_{DATA} - V_{TH}\right) R_{ON}} = \frac{10.6(C_S + C_{LC})}{\mu C_g \left(v_G - v_{DATA} - V_{TH}\right) T_R} \tag{5.10}$$

When the TFT is OFF, several causes concur to discharge the pixel capacitance, modifying gray scale uniformity. The TFT leakage current is the most relevant one, but also resistive leakage through the LC material (R_{LC}) should be considered. Considering only the TFT leakage, I_{OFF}, this should be low enough to retain the charge on the pixel capacitance during the frame time. Assuming the parallel of C_S and C_{LC} be discharged by the constant current I_{OFF} during T_F, we get

$$I_{OFF} \leq \frac{C_S + C_{LC}}{T_F} \Delta V_{LK} \tag{5.11}$$

where ΔV_{LK} is limited by the maximum acceptable voltage loss (referred to one gray level).

Tables 5.1 and 5.2 show some technology and display parameters for a very large (56.3-in.) monolithic a-Si AMLCD [KSG2002].

Table 5.1 Technology parameters of a 56.3-in. a-Si AMLCD [KSG2002]

AMLCD Technology Parameter	Value	Unit	Symbol
Row (Gate) Bus Resistance (Width 30 μm)	18.8	Ω/mm	R_R
Row Bus Capacitance (Width 30 μm)	226	fF/mm	C_R
Column (Source) Bus Resistance (Width 10 μm)	45.0	Ω/mm	R_C
Column (Source) Bus Capacitance (Width 10 μm)	82.4	fF/mm	C_C
Row-to-Column Bus Overlap Capacitance	15.3	fF	C_{XC}
Column-to-Row Bus Overlap Capacitance	15.3	fF	C_{XR}
Sub-Pixel Liquid Crystal Capacitance	8.24	pF/mm^2	C_{LC}/A
Sub-Pixel Storage Capacitance	204	pF/mm^2	C_S/A
TFT Channel On-Resistance (Width/Length 100 μm/4.5 μm)	0.0634	MΩ-mm	R_{TFT}^{On}-W
TFT Channel Off-Resistance (Width/Length 100 μm/4.5 μm)	0.607	TΩ-mm	R_{TFT}^{OFF}-W
TFT Gate-to-Source Capacitance	689	fF/mm	C_{GS}/W
TFT Gate-to-Drain Capacitance	919	fF/mm	C_{GD}/W
Row Driver Resistance	1.00	kΩ	R_{RS}
Row Driver Capacitance	1.00	pF	C_{RS}
Column Driver Resistance	1.40	kΩ	R_{CS}
Column Driver Capacitance	1.40	pF	C_{CS}

Table 5.2 Display parameters of a 56.3-in. a-Si AMLCD [KSG2002]

AMLCD Display Parameters	Value	Unit
Number of Horizontal Pixel	1280	1
Number of Vertical Pixel	720	1
Number of Column Lines	3840	1
Number of Row Lines	720	1
Aspect Ratio	16 x 9	1
Horizontal Pixel Pitch	0.974	mm
Vertical Pixel Pitch	0.974	mm
Pixel Array Width	1,246	mm
Pixel Array Height	701	mm
Display Size	1,429 (56.3)	mm (in)
Worst Case Sub-Pixel Charging Time	26.8	μs

As a numerical example, consider an XGA display with 768 rows and 60-Hz frame frequency (N=768, T_F=16.6 ms and T_R=21 μs) in which 256 gray levels are generated by a voltage swing (v_{DATA}) of 8 V (typical for large size panels). Thus, 31.2 mV defines one gray level. Assume also that $C_{LC,min}$=150 fF, $C_{LC,max}$=300 fF, C_S= 400 fF, V_{ROW}=v_G=20 V, C_g=1.06·10^{-8} F/cm, μ=0.45 cm^2/V·s, V_{TH}=3.5 V. From (5.8) we get that $R_{ON} \leq$ 2.83 MΩ, yielding $W/L \geq$7.4 from (5.10). Assuming also as tolerable a ΔV_{LK} lower than 1/6 one gray level (about 5 mV), we get from (5.11) $I_{OFF} \leq$ 0.16 pA. The values of W/L and I_{OFF} we have found are compatible with usual TFT technologies.

5.3.1 Kickback

The gate-drain parasitic capacitor C_{GD} is also the cause of charge redistribution with the pixel capacitor C_S. This phenomenon is referred to as the **kickback effect** (it is the same effect known as the clock-feedthrough experienced by designers of digital and switched-capacitor circuits) and causes a decrement, ΔV_{KB}, in the LC voltage when the TFT is turned OFF at the end of a select period (the same effect holds also when the TFT is turned ON, but it is not cause of error since it occurs at the beginning of a select period). Considering Fig. 5.11, if ΔV_G is the voltage change at the TFT gate when the row is deselected and assuming V_{COM} constant, the voltage shift of V_{LC} is expressed by

$$\Delta V_{KB} = \frac{C_{GD}}{C_{GD} + C_S + C_{LC}} \Delta V_G \tag{5.12}$$

As a result of both kickback and leakage effects, the behavior of a typical V_{LC} waveform appears as qualitatively illustrated in Fig. 5.12. The kickback causes a modification of the data voltage and the generation of an unwanted DC component (if the common electrode is held at the middle of data signal voltage swing). It is thus the cause of gray-scale errors [KTK1982], shadings [KKN1990] and flickering [K1989].

From (5.12) we see that the error is nullified for C_{GD} ideally equal to zero. Besides, ΔV_{KB} decreases by increasing C_S+C_{LC}, but this decreases also the ON charging time constant. We recall that C_{GD} for a TFT in triode is not a constant as it depends on v_{GS}. A conservative choice in order to evaluate (5.12) is to take the maximum value (5.6). Also C_{LC} is not a constant, as already discussed in Section 2.2.3. Referring to Fig. 2.12, we can take the minimum value $C_{LC,\min}$.

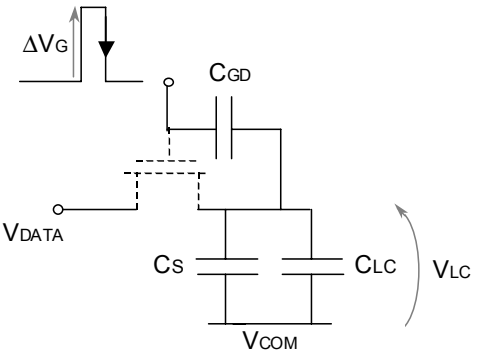


Fig. 5.11 Pixel electrical model for evaluating the kickback effect

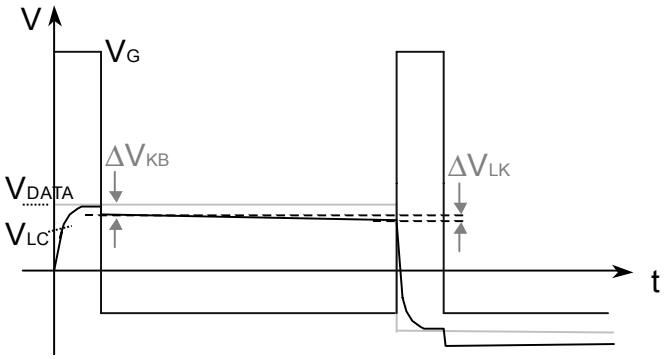


Fig. 5.12 Qualitative behavior of the pixel voltage due to kickback and leakage

As a numerical example, with the same data given before, assuming ΔV_G = 20–(–5) = 25 V, $C_{GD,\max}$=50 fF and again C_S+$C_{LC,\min}$ = 550 fF, we get the maximum ΔV_{KB} = 2.08 V, corresponding to about 67 gray levels. In addition, since the voltage shift is always negative, a DC component is added to V_{LC} that, as said in many occasions, must be avoided (limited to below 100 mV). This demonstrates that a compensation of the kickback is mandatory. To be more precise, we can write

$$C_{LC} = C_{LC,\min} + \Delta C_{LC} \tag{5.13}$$

where ΔC_{LC} depends on V_{LC}. Since also C_{GD} is dependent on the applied voltage, we can rewrite (5.12) as follows

$$\Delta V_{KB} = \Delta V_G \cdot \left[\underbrace{\frac{C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\min}}}_{\text{STATIC}} \right. \\ \left. \underbrace{- \frac{C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right) \cdot \left(C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}\right)}}_{\text{DYNAMIC}} \right] \quad (5.14)$$

We recognize a first static term, independent of the LC polarization, and a second dynamic term which depends on the LC capacitance variation (function of the gray level) and the TFT gate-drain capacitance variation. The sign of the dynamic term is opposite to that of the static term.

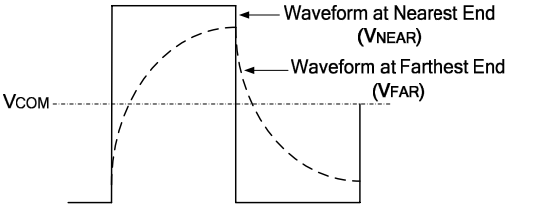
We will describe techniques for kickback compensation in Section 5.5.

5.3.2 RC Delay and Pre-emphasis Driving Method

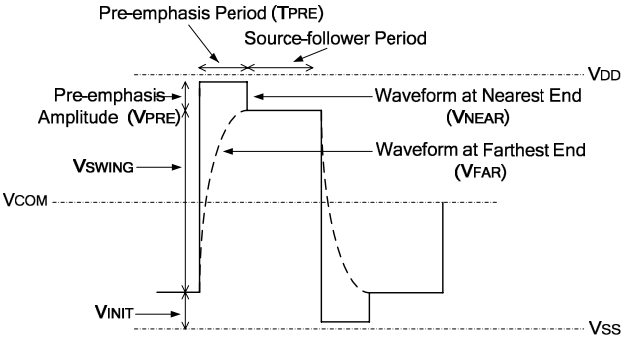
As the size and resolution of AMLCD panels increase, the large RC delay introduced by the rows and columns causes a smoothing of the ideal square waveforms and may cause an incomplete settling of the gate and column voltages. In other words, the rate of transferring the analog video signal voltage to the pixel in one row time becomes insufficient. The effect is illustrated in Fig. 5.13a. This limitation is particularly evident when driving large voltage increments onto pixel located at the farthest end of a column and of a row (with respect to the driving ends) and is particularly critical for moving pictures causing motion blur (leading to the appearance of a smear behind any moving image)[M2004]. Besides, the delay of the gate pulse waveforms produces also different kickback moving from the nearest driver end to the farthest end. To alleviate these problems, various approaches have been developed. One is technological, through the adoption of materials with low resistance for gate and source lines: for example, copper [TLT2006] or aluminium alloy [AIH1998, TCC1998]. The other approaches rely on modifying the driving method.

Source and gate drivers can be assembled at both ends of columns and rows for simultaneous driving in **Both-Side Drive** or **Dual Driving** (see Fig. 5.14). In this case the worst-case driving occurs at the center of the panel. Compared to the single-side drive, this method reduces the RC delay time up to a factor of 4, but doubles the number of gate and source drivers, thereby increasing fabrication costs. Source drivers are more critical in terms of area and power dissipation, therefore this approach is used only for the gate drivers.

A fast single-side drive technique exploits **Pre Emphasis** (or **Overdrive)**. Here the row time interval is divided into a "pre-emphasising sub-period" and a "source-follower sub-period", as illustrated in Fig. 5.13b. During the former interval, the source data waveforms use pre-emphasis amplitudes that, as we will see, vary according to the magnitude of the gray-level shift to be driven [KSK2003]. During the source-follower period, the image data voltage is presented to the source line. Figure 5.13b illustrates qualitatively the improvement offered by this technique compared to the conventional one [NIM2007].



(a)



(b)

Fig. 5.13 Waveforms for: (**a**) conventional single side and (**b**) Pre-Emphasis driving. The curves in solid (*dashed*) line represent the waveform near (far from) the driver end

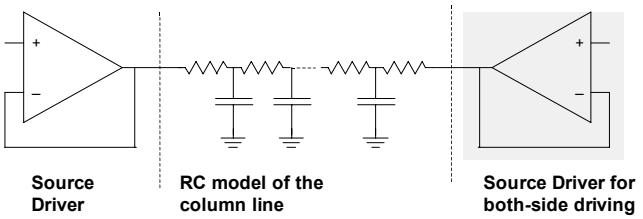


Fig. 5.14 Illustration of the Both-side Drive approach with RC-chain model of the source line and unity-gain amplifier(s) of the source driver

Let us evaluate analytically the required pre-emphasis voltage according to the data voltage swing and allowed pre-emphasis time T_{PRE}. During this time interval, the nearest end of the source line is driven at the voltage swing that is the sum of the target (nominal) voltage swing and the pre-emphasis voltage swing expressed by

$$V'_{SWING} = V_{SWING} + V_{PRE} \tag{5.15}$$

The farthest end source line voltage is expressed by

$$V_{FAR} = V_{INIT} + V'_{SWING}\left(1 - e^{-\frac{t}{R_{DATA}C_{DATA}}}\right) \tag{5.16}$$

where V_{INIT} is the initial pixel data voltage. The product R_{DATA} C_{DATA} can be evaluated through the Elmore's delay model [E1948] and, for an M-length RC-chain, it is

$$R_{DATA}C_{DATA} = \sum_{i=1}^{M}\left(C_i\sum_{j=1}^{i}R_j\right) \tag{5.17}$$

After imposing that at time T_{PRE} the far-end voltage of the source line must have settled to the target voltage level, V_{INIT}+V_{SWING}, we get [SK2007]

$$V_{PRE} = \frac{e^{-\frac{T_{PRE}}{R_{DATA}C_{DATA}}}}{1 - e^{-\frac{T_{PRE}}{R_{DATA}C_{DATA}}}}V_{SWING} \tag{5.18}$$

The above relation shows that the pre-emphasis voltage must be proportional to the required voltage swing. Observe that to maintain the advantages deriving form the method, pre-emphasis voltages need to change according to T_{PRE} and the display panel load conditions. Besides, to manage the overdrive voltages required by the approach, a higher-voltage IC fabrication process than that used for conventional source drivers must be adopted (i.e., V'_{SWING} may result higher than the ordinary supply).

Based on the fact that extremely white or black regions have insignificant effects on image quality, a modification of the approach that varies the duration of the pre-emphasis period, rather than its amplitude (this last can be maintained only in the mid-swing regions) was proposed in [YHY2007]. This method does not require higher-voltage IC processes.

5.4 Crosstalk Reduction and Polarity Inversion Techniques

5.4.1 Crosstalk in AMLCDs

As explained in Section 3.3.3 crosstalk is mainly due to capacitive coupling effects. These effects worsen with the scaling of lithographic dimensions and increasing number of gray levels. In addition, crosstalk in AMLCDs can be caused by the following mechanisms [LL1998]:

(1) incomplete pixel charging (due to high TFT ON resistance, unequal data driver loading, line delay);

(2) leakage current from the pixel through the TFT.

Remedies to these problems are based on material selection, fabrication processes, device design and layout. For our scopes, we will address only the capacitive coupling effects.

Consider the layout of a pixel and his crosstalk capacitance shown in Fig. 5.15.

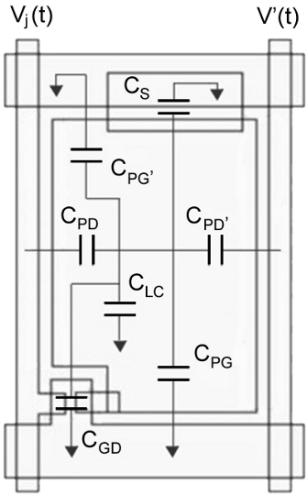


Fig. 5.15 Top view of a typical pixel layout showing the data-line-to-LC-electrode parasitic capacitance regions

The ratio of parasitic capacitances coupling the pixel-to-data line (α) and pixel-to-adjacent-data line (β) can be expressed as

$$\alpha = \frac{C_{PD}}{C_{LC} + C_S + C_{PG} + C_{PG'} + C_{GD} + C_{PD} + C_{PD'}} \tag{5.19a}$$

$$\beta = \frac{C_{PD'}}{C_{LC} + C_S + C_{PG} + C_{PG'} + C_{GD} + C_{PD} + C_{PD'}} \tag{5.19b}$$

where C_{PD} and $C_{PD'}$ are the data-line- and adjacent-data-line-to-pixel-electrode coupling capacitances, respectively, while C_{PG} and $C_{PG'}$ are the gate-line- and adjacent-gate-line-to-pixel-electrode coupling capacitances, respectively.

Note that all capacitances except C_S in (1) and (2) are functions of the liquid crystal dielectric constant. Both parameters α and β must be minimized to minimize the effects of crosstalk.[4] One method relies on increasing C_S. Another one requires a ground-plane shielding beneath the data line. Both methods need added pixel area, at the expense of a smaller aperture ratio and larger gate-line delay.[5] A third method is based on an appropriate data-driving scheme. It leaves unaltered the pixel layout and fabrication technology, thereby providing the least expensive and most straightforward approach to further pixel scaling. Note that this approach does not change α and β, but relies on incorporating some form of positive and negative data-line pulse-coupling cancellation. As a drawback, higher voltage drivers and/or higher driver power consumption may result.

We recall that any driving method must provide a nominally zero DC component of the pixel voltage. Actually a DC residual always exists and to avoid LC mixture damage, all present driving methods include some signal voltage polarity inversion in a time scale shorter than that needed for the mobile LC ions to move substantially.

According to the type of polarity inversion (in which the signs of both the row and column signals are periodically inverted) there are four possible driving methods. These are illustrated in Fig. 5.16 and are called **Frame Inversion, Column (Data-Line) Inversion, Row (Gate-Line) Inversion** and **Dot Inversion**.

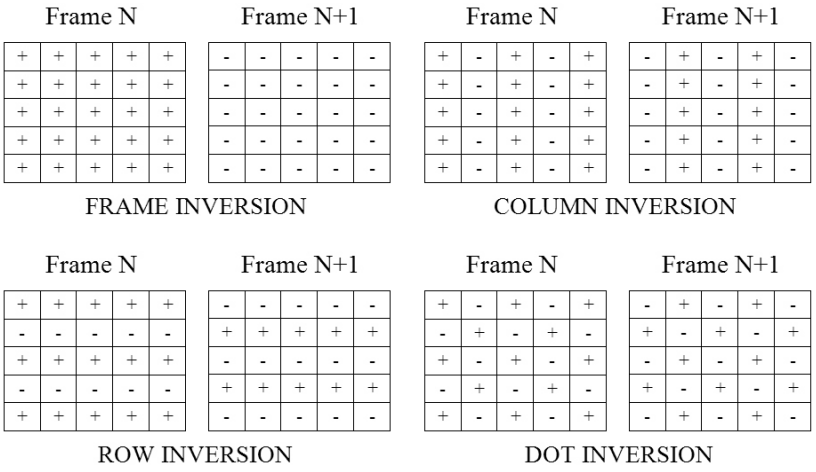


Fig. 5.16 Polarity inversion methods

[4] $\alpha = 0.08$ and $\beta = 0.03$ were extracted for a VGA display in [LL1998].

[5] The IPS-Pro pixel structure has large C_S capacitance without reducing the aperture ratio because the common electrode is made of transparent material under the pixel electrodes [EOO2006].

The principal trade-off among the four mentioned driving methods is the degree of crosstalk cancellation versus driver chip power dissipation, and sensitivity to flicker.

In the **Frame Inversion** method, each source signal has the same data polarity and the data polarity is inverted once per frame time. The value of the instantaneous voltage across the liquid crystal capacitor in the *i*th row position is given by:

$$V_{pi}(t) = V_i + \alpha \cdot [V_j(t) - V_i] + \beta \cdot [V_j'(t) - V_i'] \tag{5.20}$$

where V_i and V_i' are the data voltages initially written onto the pixel and the adjacent pixel through pixel selection, respectively, through their corresponding TFTs. $V_j(t)$ and $V_j'(t)$ are the data-line and adjacent-data-line voltages with their respective parasitic coupling factors to the pixel, α and β.

In the Frame Inversion method, the RMS voltage at the i_{th} row position in a *N*-row display can be derived from (5.20) as

$$\overline{V}_{pi}^2 = \frac{1}{N}\left\{ V_i^2 + \sum_{j>i}^{N}\left[V_i + \alpha\left(V_j - V_i\right) + \beta\left(V_j' - V_i'\right)\right]^2 + \sum_{j=1}^{i-1}\left[-V_i + \alpha\left(V_j - \left(-V_i\right)\right) + \beta\left(V_j' - \left(-V_i'\right)\right)\right]^2 \right\} \tag{5.21}$$

where the first term (V_i^2) represents the value of voltage pixel during the TFT switching-on (line *i-th* selected), the second term represents the value of voltage pixel during the switching-on of all subsequent rows, while the third is the voltage pixel during the switching-on of the previous rows (reversed polarity).

The simplified expression, obtained by neglecting the second-order crosstalk terms (proportional to α^2, β^2, and $\alpha\beta$) in (5.21), is

$$\overline{V}_{pi}^2 \cong \left(V_i - \alpha V_i + \beta V_i'\right)^2 + \frac{2}{N} V_i \left[\sum_{j\geq i}^{N}\left(\alpha V_j + \beta V_j'\right) - \sum_{j=1}^{i-1}\left(\alpha V_j + \beta V_j'\right)\right] \tag{5.22a}$$

then

$$\overline{V}_{pi}^2 \cong \left(V_i - \alpha V_i + \beta V_i'\right)^2 + \frac{2}{N}\alpha V_i \left[\sum_{j\geq i}^{N} V_j - \sum_{j=1}^{i-1} V_j\right] + \frac{2}{N}\beta V_i \left[\sum_{j\geq i}^{N} V_j' - \sum_{j=1}^{i-1} V_j'\right] \tag{5.22b}$$

Since each pixel is made up of three (RGB) sub-pixels, in general it is $V_j(t) \neq V_j'(t)$. This condition guarantees that the first-order term in (5.22b) (linear in α and β) is dependent on the data-line voltage for one frame. The Frame Inversion is sensitive to flickering due to the absence of spatial averaging.

In a similar way, a general expression can be written for the case of the **Column Inversion** method, for which each consecutive signal line has alternating positive and negative data polarity and the data polarity is inverted once per frame time. By neglecting the second-order crosstalk terms, we obtain:

$$\overline{V}_{pi}^2 \cong \left(V_i - \alpha V_i + \beta V_i^{'}\right)^2 + \frac{2}{N}\alpha V_i\left[\sum_{j\geq i}^{N} V_j - \sum_{j=1}^{i-1} V_j\right] - \frac{2}{N}\beta V_i\left[\sum_{j\geq i}^{N} V_j^{'} - \sum_{j=1}^{i-1} V_j^{'}\right] \tag{5.23}$$

Note that although $V_j(t) \neq V_j'(t)$, the Column Inversion method provides a better crosstalk compensation compared to the Frame Inversion owing to the polarity inversion between two adjacent columns that gives a *negative* contribution in the expression of RMS pixel voltage. This method is less sensitive to horizontal crosstalk caused by capacitive coupling between adjacent columns and can produce better crosstalk compensation to a larger number of pattern images compared to Frame Inversion. It is also less exposed to flicker due to the presence of spatial averaging.

For the **Row Inversion** driving method, where each signal line has the same data polarity and the data polarity is inverted once per scan line time, we obtain the expression in (5.24a) and by neglecting the second-order crosstalk terms we obtain the simplified expression in (5.24b).

$$\begin{aligned}\overline{V}_{pi}^2 = \frac{1}{N}\Bigg\{ & V_i^2 + \sum_{j(even)>i}^{N}\left[-V_i + \alpha\left(V_j - \left(-V_i\right)\right) + \beta\left(V_j^{'} - \left(-V_i^{'}\right)\right)\right]^2 \\ & + \sum_{j(even)=2}^{i-1}\left[V_i + \alpha\left(V_j - V_i\right) + \beta\left(V_j^{'} - V_i^{'}\right)\right]^2 \\ & + \sum_{j(odd)>i}^{N}\left[V_i + \alpha\left(V_j - V_i\right) + \beta\left(V_j^{'} - V_i^{'}\right)\right]^2 \\ & + \sum_{j(odd)=1}^{i-1}\left[-V_i + \alpha\left(V_j - \left(-V_i\right)\right) + \beta\left(V_j^{'} - \left(-V_i^{'}\right)\right)\right]^2 \Bigg\}\end{aligned} \tag{5.24a}$$

$$\overline{V}_{pi}^{2} \cong \left(V_i - \alpha V_i + \beta V_i^{'}\right)^2 + \frac{2}{N}\alpha V_i \left[\sum_{j(odd)\geq i}^{N} V_j - \sum_{j(odd)=1}^{i-1} V_j - \sum_{j(even)>i}^{N} V_j + \sum_{j(even)>1}^{i} V_j\right] + \frac{2}{N}\beta V_i \left[\sum_{j(odd)\geq i}^{N} V_j^{'} - \sum_{j(odd)=1}^{i-1} V_j^{'} - \sum_{j(even)>i}^{N} V_j^{'} + \sum_{j(even)>1}^{i} V_j^{'}\right] \quad (5.24b)$$

Compared to the Frame Inversion driving method described by (5.23), the Row Inversion one contains an additional polarity reversal, as it is evident from the separation of even and odd data-line values (V_j) and adjacent data-line (V_j') values. For this reason, the Row Inversion driving method, in general, provides better crosstalk compensation than the Frame Inversion driving method, but this is not guaranteed, because the magnitude of crosstalk is dependent upon the screen image pattern. For instance, if an alternating image pattern of black to white on the spatial periodicity of a scan line were present, the result is a worst-case adding of all coefficients of α and β for the case of the Row Inversion method. In general, image patterns tend to be uniform over a screen area of at least several gate-line spatial dimensions [LL1998]. In contrast to the Column Inversion method, this one provides a better compensation of the vertical crosstalk produced by capacitive coupling between the rows, but it is more sensitive to the horizontal crosstalk. As the Column Inversion, it is also less exposed to flicker. As above, a general expression can be written for the RMS pixel voltage in the case of the **Dot Inversion** method, where the column and the row inversion approaches are both applied to the data so that each consecutive signal line (column), as well as each consecutive gate line (row), has an alternating positive and negative data polarity, and the data polarity is inverted once per frame time. By neglecting the second-order crosstalk terms, the resulting expression is expressed in (5.25) and includes an additional polarity reversal compared to (5.24b).

$$\overline{V}_{pi}^{2} \cong \left(V_i - \alpha V_i + \beta V_i^{'}\right)^2 + \frac{2}{N}\alpha V_i \left[\sum_{j(odd)\geq i}^{N} V_j - \sum_{j(odd)=1}^{i-1} V_j - \sum_{j(even)>i}^{N} V_j + \sum_{j(even)>1}^{i} V_j\right] - \frac{2}{N}\beta V_i \left[\sum_{j(odd)\geq i}^{N} V_j^{'} - \sum_{j(odd)=1}^{i-1} V_j^{'} - \sum_{j(even)>i}^{N} V_j^{'} + \sum_{j(even)>1}^{i} V_j^{'}\right] \quad (5.25)$$

This method has virtually no flicker.

Equations (5.22b), (5.23), (5.24b), and (5.25) describing all four crosstalk-reduction driving methods show a gain-correction term $(V_i - \alpha V_i + \beta V_i')^2$ as the first term. For a simplified case, if $V_i = V_i'$, the gain correction is $(1 - \alpha + \beta)^2$, and the effect is only a parallel shift in the T/V curve which depends on the values of α and β. Any DC gain in the required RMS operation of the LC can easily be offset. In general, however, $V_i \neq V_i'$, which makes the gain term data dependent on the voltage or image pattern, and it cannot be easily offset.

Among the previous techniques, the Dot Inversion gives the best quality. Row and Column Inversion are suitable for the reduction of vertical and horizontal crosstalk effects, respectively. Since Column and Dot inversion needs source drivers with high voltage swings, a good trade-off between area/power consumption and image quality is given by the Row Inversion. Another approach that was not discussed and that is a further simplification of the Row Inversion is called **n-Line Inversion.** In this case polarity of the addressing waveforms is reversed at every *n* rows, where *n* is an integer less than the number *N* of matrix rows. Recently, **Vertical n-dot Inversion** has been adopted as a polarity reversal method to reduce power consumption while maintaining image quality [SKC2007]. The Vertical 2-dot Inversion is exemplified in Fig. 5.17.

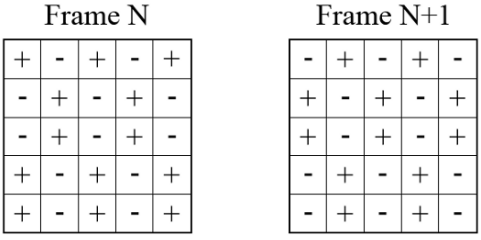


Fig. 5.17 Vertical 2-Dot Inversion driving method

In another technique, referred to as **Data Complement**, the row addressing time is partitioned into two intervals. During the first interval the data is applied to the source line, as usual. During the second interval all the row TFTs are turned OFF and the data complement (voltages with opposite sign) is applied to the source lines. If the two time intervals are equal, it can be easily shown that first-order crosstalk is eliminated [HAW1989]. The simplest case of equal subperiods halves however the net row time (it is now $T/2N$ instead of T/N) and hence requires an LC mixture with doubled switching speed. To avoid this drawback, the compensation interval can be a fraction $\delta T/N$ of the row time (with $\delta<0.5$), and the amplitude of the complement voltage must be increased by a $\sqrt{\delta/(1-\delta)}$ factor.

5.4.2 Power Analysis of Polarity-Inversion Techniques

In this section we will evaluate the power consumption of the above polarity inversion methods. We will consider a display with *N* rows and *M* columns and

assume that the load capacitance of each source driver is constant and that the common electrode voltage V_{COM} is 0 V.

(a) Frame Inversion. In this case the lowest power consumption is obtained when all the pixel voltages of the same column are equal during a given frame time (white pixels are considered, otherwise for all black pixels the power consumption is theoretically zero). Indeed, in this case the Source Drivers have the minimum number of commutations. The power dissipated by a single column is hence:

$$P_{COL} = \frac{1}{2} \cdot C_{TOT} \cdot \left[V_{SAT} - (-V_{SAT}) \right]^2 \cdot f_F = 2 \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \tag{5.25}$$

where C_{TOT} is the total capacitance seen by the Source Drivers, whose largest output voltages in the positive and negative frames are $+V_{SAT}$ and $-V_{SAT}$, respectively and f_F is the frame frequency.

The overall power consumption in this best-case condition is

$$P_{\min} = 2 \cdot M \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \tag{5.26}$$

The worst case occurs when we have an alternating succession of black and white rows. In this case each Source Driver must provide N commutations in each frame.

$$P_{\max} = \frac{1}{2} \cdot N \cdot M \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \tag{5.27}$$

$P_{\max}$ is $N/4$ times greater than $P_{\min}$ and then power consumption in Frame Inversion is limited by

$$P_{\min} \le P_{FI} \le \frac{M}{4} \cdot P_{\min} \tag{5.28}$$

(b) Column Inversion. The power consumption is exactly the same as in the previous case, because the pixels of the same column are subject to the same voltage. Hence, P_{CI} equals P_{FI}.

(c) Row and Dot Inversion. Dually to the previous approaches, here the maximum power consumption occurs when all the pixel voltages of the same column are equal during a given frame time. Indeed, in this case the Source Drivers have the maximum number of commutations.

$$P_{\max} = 2 \cdot N \cdot M \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \tag{5.29}$$

and is 4 times greater than P_{MAX} of Frame e Column Inversion approaches. Besides from (5.26) it is N times greater than P_{MIN} obtained with Frame and Column Inversion. Therefore, we get

$$P_{\min} \le P_{RI} = P_{DI} \le M \cdot P_{\min} \tag{5.30}$$

The power consumption is greater in those driving methods where row polarity is switched from frame to frame.

For simplicity, we have assumed V_{COM} equal to 0 V. Actually, V_{COM} can be different form 0 and even a variable voltage (V_{COM} switching) in order to meet the constraints set by the adopted CMOS technology, area occupation, and/or low voltage demand. The V_{COM} switching approach increases the power dissipation and causes additional charge injection effects through parasitic capacitances. We will see in Section 5.5.2 that V_{COM} switching requires the same polarity for pixel of the same row and therefore cannot be adopted in both Column and Dot Inversion techniques.

5.5 Kickback Compensation Methods

We have seen in (5.14) that the error due to the kickback includes two contributions: a static one, independent of the gray level, and a dynamic one

$$\Delta V_{KB} = \Delta V_{KB,ST} + \Delta V_{KB,DYN} \tag{5.31}$$

The dynamic contribution, being dependent on the actual data, must be compensated by the source driver. The static part may be compensated through different approaches: we can shift V_{COM} (as illustrated in Fig. 5.18), or through the subsequent gate voltage for Cap-on-Common architectures or other techniques that will be described in the following.

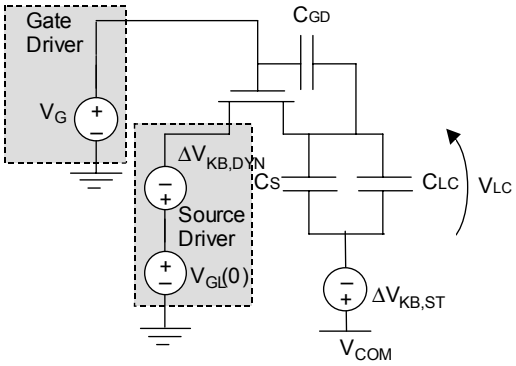


Fig. 5.18 Kickback compensation through the Source Driver (dynamic part) and V_{COM} (static part). The static part can be also compensated via the subsequent gate line, for cap-on-gate architectures

The gray-level voltage, V_{GL}, that through the source drivers must be applied to each pixel is hence

$$V_{GL} = V_{GL}(0) - \Delta V_{KB,DYN} \tag{5.32}$$

where $V_{GL}(0)$ represents the nominal gray-level voltage without kickback correction ("0" stands for zero kickback). Using (5.14), (5.32) can be rewritten as

$$V_{GL} = V_{GL}(0) + \frac{C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right) \cdot \left(C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}\right)} \tag{5.33}$$

In practice, the nonlinear compensation required by (5.33) is implemented in the same circuit block that operates the Gamma Correction. Considering only the nonlinearity of the electrooptic T/V behavior, the Gamma Correction curve should be symmetrical in both positive and negative values, as already described in Section 4.5.2. This symmetry is lost if we introduce also the compensation of the dynamic part of kickback, as illustrated in Fig. 5.19. Note that due to the nonlinear dependence of C_{LC} on the applied voltage, curve (b) is not obtained by a simple shifting of curve (a). This implies that two different gamma curves must be constructed for both positive and negative polarity.

The kickback compensation for both the static and dynamic contributions is closely related to the driving scheme adopted [N1986, YKK1986, S1987, T1989, TNM1990]. In the following we will examine this issue with reference to the four polarity inversion techniques discussed before.

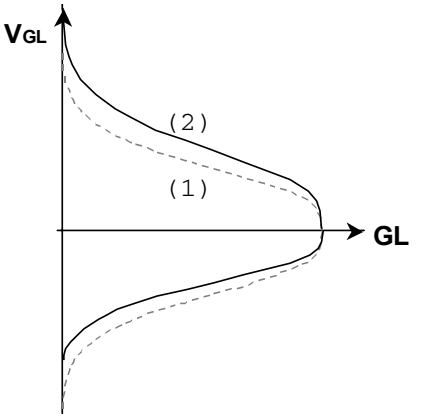


Fig. 5.19 Gamma correction curves: ideal symmetrical (1) and asymmetrical including dynamic kickback compensation (2)

5.5.1 2-Level Driving

In this scheme the Gate Driver provides a two-level output voltage, V_{ON} and V_{OFF}, for selected and unselected rows, as illustrated in Fig. 5.20. Voltage V_{COM} is held constant and consequently the Source Drivers signal swing must be $2V_{SAT}$ (≈ 10V) to

allow polarity inversion and thus covering the maximum excursion range given by V_{COM}–V_{SAT} to V_{COM}+V_{SAT}. Nominally, V_{COM} can be either equal to 0 V or to V_{SAT}.

The dynamic kickback contribution is compensated via the asymmetrical Gamma Correction curve described before. Considering the static contribution and (5.14), its compensation is achieved by shifting the nominal value of V_{COM} by a quantity ΔV_{COM}

$$\Delta V_{COM} = \Delta V_{ST} = \left(V_{OFF} - V_{ON}\right) \cdot \frac{C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\min}} \tag{5.34}$$

Figure 5.21 illustrates the driving voltages in the case of 2-Level Driving for a Cap-on-Common LCD panel structure. The compensation effect is apparent. After the charge injection, the magnitude of the V_{LC} voltages in both positive and negative polarity are equal.

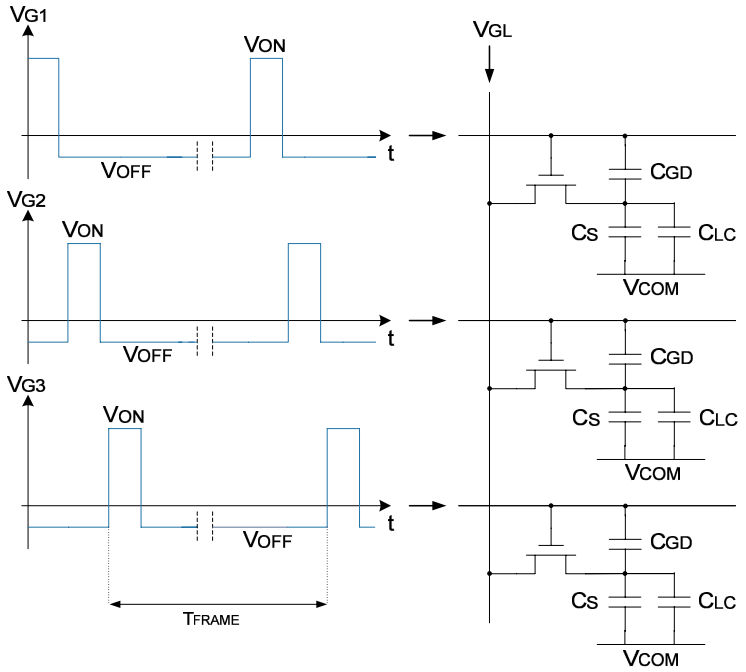


Fig. 5.20 Gate driver waveforms for three subsequent gate lines in the case of the 2-Level driving scheme

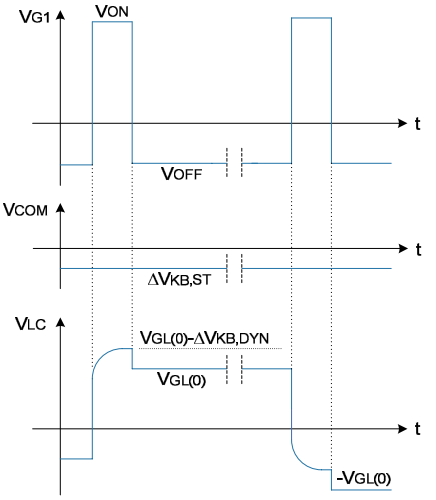


Fig. 5.21 Driving voltages in the case of 2-Level approach for a Cap-on-Common LCD panel structure

5.5.2 V_{COM} Switching

This technique operates the inversion polarity through the modulation of voltage V_{COM}, as illustrated in Fig. 5.22, where V_{GL} is the data voltage to be applied (in both polarities) to the LC pixel and V_{SD} is the output voltage of the Source Driver. Compared to the two-level approach, a Source Driver with a halved output swing is required. The approach is thereby suitable to be employed with low-voltage CMOS technologies.

Unfortunately, an additional error is introduced due to the charge injection from the common electrode when the TFT is OFF and V_{COM} is switching from 0 V to V_{SAT}, in order to allow the polarity inversion of the other rows (see Fig. 5.23). This problem is simply eliminated by introducing the same voltage change onto the gate voltage. Therefore, voltage V_{OFF} at the output of the Gate Driver can be either $V_{OFF,H}$ or $V_{OFF,L}$ so that

$$V_{OFF,H} - V_{OFF,L} = V_{COM,H} - V_{COM,L} \tag{5.35}$$

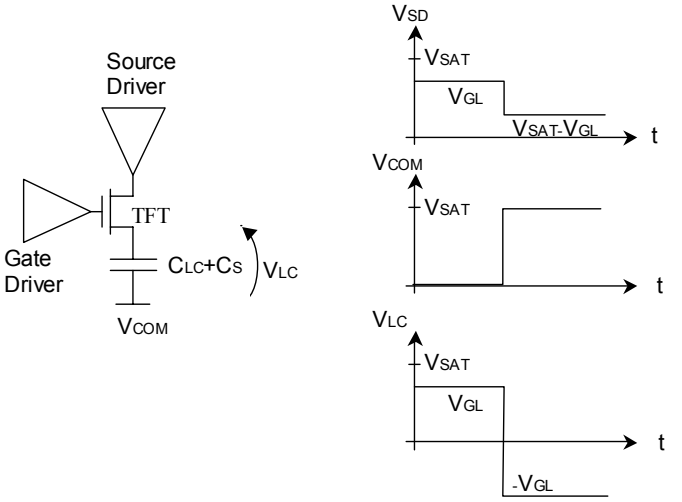


Fig. 5.22 Source Driver and V_{COM} waveforms for V_{COM}-switching driving scheme

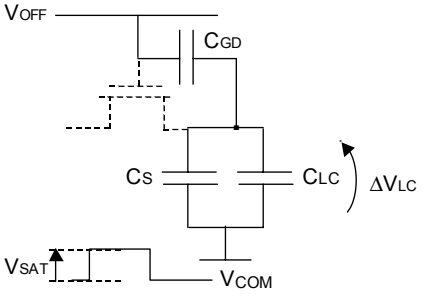


Fig. 5.23 Illustration of the error voltage (ΔV_{LC}) caused by the switching of V_{COM} when the row is unselected

The gate driving waveforms required in the V_{COM}-switching technique are exemplified in Fig. 5.24. To better illustrate the behavior, a Row Inversion method is assumed.

As far as the kickback is concerned, in this case the amount of kickback differs from positive to negative polarity, owing to the different C_{LC} and C_{GD} and also to the different step amplitude, that is $V_{ON} - V_{OFF,L}$ for negative polarity and $V_{ON} - V_{OFF,H}$ for positive polarity.

Consequently, the kickback amount is

$$\Delta V_{KB}^{+} = (V_{ON} - V_{OFF,H}) \cdot \left[\frac{C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\min}} + \right.$$
$$\left. - \frac{C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right) \cdot \left(C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}\right)} \right] \qquad (5.36a)$$
$$= \Delta V_{KB,ST}^{+} + \Delta V_{KB,DYN}^{+}$$

$$\Delta V_{KB}^{-} = (V_{ON} - V_{OFF,L}) \cdot \left[\frac{C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\max}} + \right.$$
$$\left. - \frac{C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right) \cdot \left(C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}\right)} \right] \qquad (5.36b)$$
$$= \Delta V_{KB,ST}^{-} + \Delta V_{KB,DYN}^{-}$$

The compensation of the static contribution is performed by shifting the value of V_{COM} by $\Delta V_{KB,ST}^{+}$ and $\Delta V_{KB,ST}^{-}$ and in turn the values $V_{OFF,H}$ and $V_{OFF,L}$. The expression of the pixel voltages in both polarities are

$$V_{LC}^{+} = V_{GL}^{+} + \Delta V_{KB}^{+} - \Delta V_{COM,L} \qquad (5.37a)$$

$$V_{LC}^{-} = V_{GL}^{-} + \Delta V_{KB}^{-} - \left(V_{SAT} + \Delta V_{COM,H}\right) \qquad (5.37b)$$

where $\Delta V_{COM,L}$ and $\Delta V_{COM,H}$ are the correction values of the low and high V_{COM} level, respectively. As stated before, 0 and V_{SAT} are the low and high V_{COM} ideal levels (neglecting any kickback).

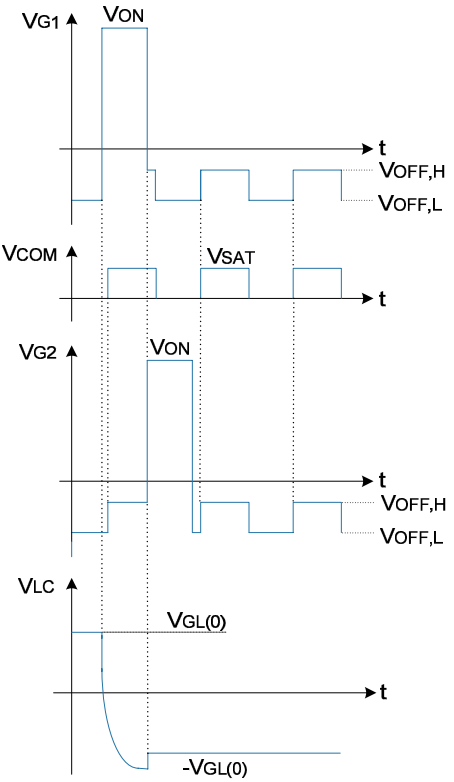


Fig. 5.24 Waveforms of two adjacent gate lines, common electrode, and pixel for V_{COM}-switching driving scheme

The dynamic contribution is compensated as usual via the Gamma Correction curve. Observe that for negative polarity the Gamma curve extends to negative voltage values. This should be avoided if source drivers with positive output swing are to be adopted. To obtain a completely positive Gamma curve it must be shifted by a constant value equal to the dynamic kickback of a *black* pixel. Rearranging (5.37) we get:

$$V_{LC}^{+} = V_{GL}^{+}(0) + \Delta V_{KB,ST}^{+} - (0 + \Delta V_{COM,L}) \tag{5.38a}$$

$$V_{LC}^{-} = V_{GL}^{-}(0) + \Delta V_{KB,DYN}^{-}(\text{Black}) + \Delta V_{KB,ST}^{-} - (V_{SAT} + \Delta V_{COM,H}) \tag{5.38b}$$

To obtain the correct pixel voltages $V_{LC}^{+} = V_{GL}^{+}(0)$ and $V_{LC}^{-} = V_{GL}^{-}(0) - V_{SAT}$, the required $\Delta V_{COM,L}$ and $\Delta V_{COM,H}$ are:

$$\Delta V_{COM,H} = \Delta V_{KB,ST}^{-} + \Delta V_{KB,DYN}^{-}(\text{Black}) \tag{5.39a}$$

$$\Delta V_{COM,L} = \Delta V^{+}_{KB,ST} \tag{5.39b}$$

Finally, from (5.35) and (5.39) we get:

$$V_{COM,H} = V_{SAT} + \left(V_1 - V_{OFF,H}\right) \cdot \frac{-C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\max}} \tag{5.40}$$

$$V_{COM,L} = \frac{-C_{GD,\max} \cdot \left[C_{GD,\max} \cdot V_{SAT} + \left(C_{LC,\max} + C_S\right) \cdot \left(V_1 - V_{OFF,H} + V_{SAT}\right) \right]}{\left(C_{LC,\min} + C_S\right) \cdot \left(C_{GD,\max} + C_{LC,\max} + C_S\right)} \tag{5.41}$$

$$V_{OFF,L} = V_{OFF,H} - V_{SAT} - \Delta V_{COM,H} + \Delta V_{COM,L} \tag{5.42}$$

Considering the negative polarity, the gamma correction amount is

$$V_{GL}^{-} = V_{GL}^{-}(0) - \Delta V^{-}_{KB,DYN} + \Delta V^{-}_{KB,DYN}(\text{Black}) \tag{5.43}$$

It should also be observed that the numerous commutations of the common electrode and Gate Lines, increase, in the case of Row Inversion, the power consumption. This is a clear limit of this approach for mobile applications. Besides, owing to the commutation of V_{COM}, techniques such as Column e Dot Inversion cannot be implemented. This scheme is however compatible with both Cap-on-Common and Cap-on-Gate structures.
As a numerical example, consider the typical values listed below:

$V_{SAT} = 5$ V, $V_1 = 18$ V, $V_{OFF,H} = -8$ V, $C_{GD,\max} = 50$fF, $C_{LC,\min} = 150$fF,
$C_{LC,\max} = 300$fF, $C_S = 400$fF

Using (5.40)–(542) we get the following voltages:

$V_{COM,H} = 3.267$ V, $V_{COM,L} = -2.661$ V, $V_{OFF,L} = -13.928$ V

5.5.3 3-Level Driving

Like in the 2-Level approach, a constant V_{COM} is here employed (a high-voltage Source Driver is hence needed). This approach exploits the Cap-on-Gate panel structure, where the storage capacitor C_S is connected to the adjacent Gate Line, as depicted in Fig. 5.25, showing also the driving waveforms. V_1 is the TFT ON voltage, V_3 is the OFF voltage, and V_2 is called a pre-pulse voltage.

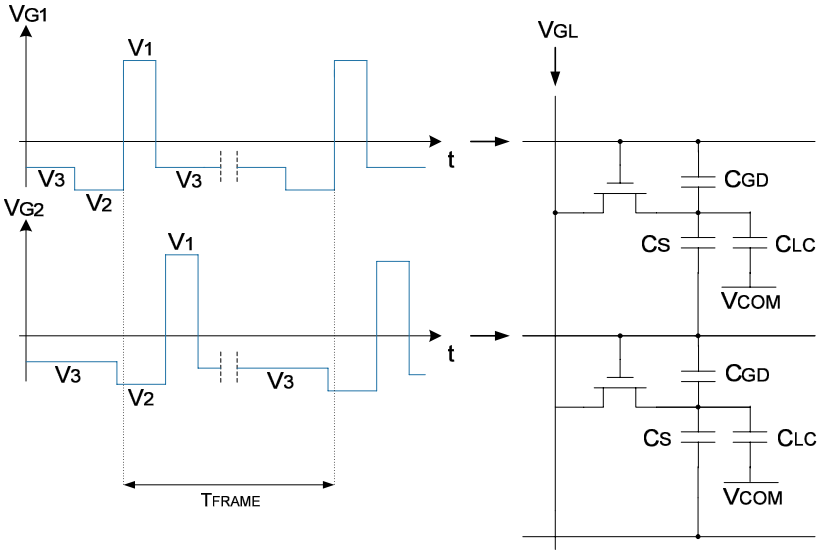


Fig. 5.25 Gate voltages in the case of 3-Level driving scheme

Separating the static and dynamic kickback contributions we get:

$$\Delta V_{KB,ST} = \left(V_3 - V_1\right) \cdot \frac{C_{GD,\max}}{C_{GD,\max} + C_{LC,\min} + C_S} - \left(V_3 - V_2\right) \cdot \frac{C_S}{C_{GD,\min} + C_{LC,\min} + C_S} \tag{5.44a}$$

$$\Delta V_{KB,DYN} = \left(V_3 - V_1\right) \cdot \frac{-C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right)\left(C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}\right)}$$

$$+ \left(V_3 - V_2\right) \cdot \frac{C_S \cdot \Delta C_{LC}}{\left(C_{GD,\min} + C_{LC,\min} + C_S\right)\left(C_{GD,\min} + C_{LC,\min} + C_S + \Delta C_{LC}\right)} \tag{5.44b}$$

After setting $\Delta V_{KB,ST} = 0$ we get

$$\begin{aligned} V_2 &= V_3 + \left(V_3 - V_1\right) \cdot \frac{C_{GD,\max}}{C_S} \cdot \frac{C_{GD,\min} + C_{LC,\min} + C_S}{C_{GD,\max} + C_{LC,\min} + C_S} \\ &\approx V_3 + \left(V_3 - V_1\right) \cdot \frac{C_{GD,\max}}{C_S} \end{aligned} \tag{5.45}$$

Substituting (5.45) into (5.44b) we get the dynamic kickback component

$$\Delta V_{KB,DYN} \approx (V_3 - V_1) \cdot \frac{-C_{GD,\max} \cdot \Delta C_{LC}}{C_{GD,\max} + C_S + C_{LC,\min}} \cdot \left(\frac{1}{C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}} - \frac{1}{C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}} \right) = 0 \tag{5.46}$$

As an important result, we see that with the aid of a pre-pulse voltage both static and dynamic kickback components are ideally eliminated, without requiring the use of Gamma correction. The Gamma curve can be therefore symmetrical, with an advantage both for circuit complexity and calibration task. Actually, due to the fact that C_{GD} is not constant, we cannot achieve a perfect cancellation of kickback. The driving voltages are illustrated in Fig. 5.26.

Assuming V_1=18 V, V_3= −8 V, $C_{GD,\max}$=50 fF, $C_{GD,\min}$=30 fF and C_S=400 fF, we get from (5.45) V_2= −11.142 V (and with the approximation −11.250 V).

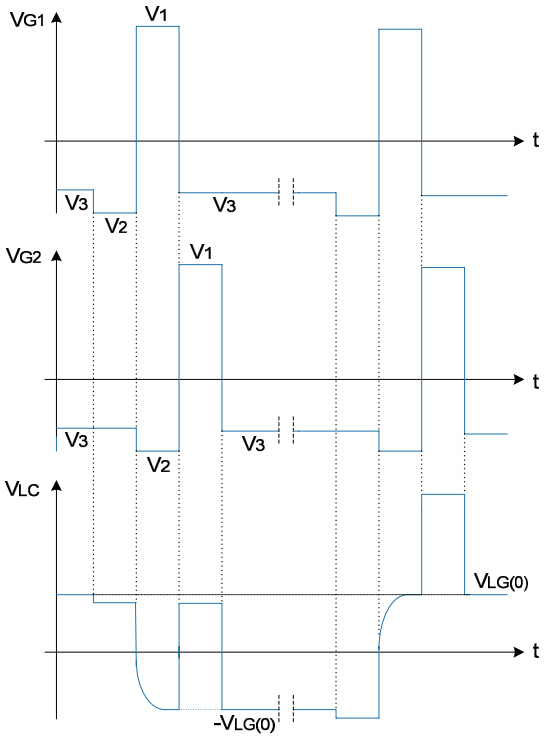


Fig. 5.26 Driving and pixel voltages in the case of 3-Level driving scheme

5.5.4 4-Level Driving

As for the 3-Level approach, also this driving scheme exploits the Cap-on-Gate structure. However, in this case the aim is to use a low-voltage source driver and a constant V_{COM}. The polarity inversion is here obtained by using four voltage levels in the gate line. These waveforms are shown in Fig. 5.27 (Frame Inversion is assumed).

Denoting as ΔV_{KB}^{+} and ΔV_{KB}^{-} the kickback in a positive and negative frame polarity, respectively, and separating the static and dynamic components we get:

$$\Delta V_{KB,ST}^{+} = \left(V_3 - V_1\right) \cdot \frac{C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\min}} + \left(V_3 - V_4\right) \cdot \frac{C_S}{C_{GD,\min} + C_S + C_{LC,\min}} \tag{5.47a}$$

$$\Delta V_{KB,ST}^{-} = \left(V_3 - V_1\right) \cdot \frac{C_{GD,\max}}{C_{GD,\max} + C_S + C_{LC,\min}} + \left(V_3 - V_2\right) \cdot \frac{C_S}{C_{GD,\min} + C_S + C_{LC,\min}} \tag{5.47b}$$

$$\Delta V_{KB,DYN}^{+} = \left(V_3 - V_1\right) \cdot \frac{-C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right)\left(C_{GD,\max} + C_S + C_{LC,min} + \Delta C_{LC}\right)} +$$

$$- \left(V_3 - V_4\right) \cdot \frac{C_S \cdot \Delta C_{LC}}{\left(C_{GD,\min} + C_S + C_{LC,min}\right)\left(C_{GD,\min} + C_S + C_{LC,\min} + \Delta C_{LC}\right)} \tag{5.48a}$$

$$\Delta V_{KB,DYN}^{-} = \left(V_3 - V_1\right) \cdot \frac{-C_{GD,\max} \cdot \Delta C_{LC}}{\left(C_{GD,\max} + C_S + C_{LC,\min}\right)\left(C_{GD,\max} + C_S + C_{LC,\min} + \Delta C_{LC}\right)} +$$

$$- \left(V_3 - V_2\right) \cdot \frac{C_S \cdot \Delta C_{LC}}{\left(C_{GS,\min} + C_S + C_{LC,\min}\right)\left(C_{GS,\min} + C_S + C_{LC,\min} + \Delta C_{LC}\right)} \tag{5.48b}$$

The pixel voltage is hence

$$V_{LC}^{+} = V_{GL}^{+} + \Delta V_{KB,ST}^{+} + \Delta V_{KB,DYN}^{+} - V_{COM} \tag{5.49a}$$

$$V_{LC}^{-} = V_{GL}^{-} + \Delta V_{KB,ST}^{-} + \Delta V_{KB,DYN}^{-} - V_{COM} \tag{5.49b}$$

where:

$$V_{GL}^{+} = V_{GL}^{+}(0) + \Delta V_{GAMMA}^{+},\ V_{GL}^{-} = \left[V_{SAT} - V_{GL}^{+}(0)\right] + \Delta V_{GAMMA}^{-},\ V_{LC}^{+} = -V_{LC}^{-}$$

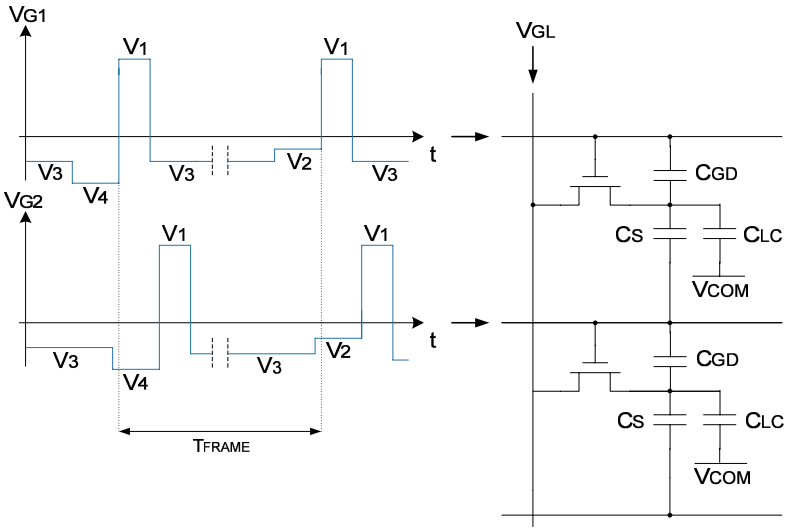


Fig. 5.27 Gate voltages in the case of 4-Level driving scheme (Frame Inversion is assumed)

Similarly to the previous case of V_{COM} modulation, in order to have a positive gamma voltage for both polarities we must set:

$$\Delta V_{GAMMA}^{+} = -\Delta V_{KB,DYN}^{+} \text{ and } \Delta V_{GAMMA}^{-} = -\Delta V_{KB,DYN}^{-} + \Delta V_{KB,DYN}^{-}(\text{Black})$$

$$\Delta V_{KB,ST}^{+} = V_{COM} \text{ and } \Delta V_{KB,ST}^{-} = V_{COM} - V_{SAT} - \left|\Delta V_{KB,DYN}^{-}(\text{Black})\right|$$

After setting $V_{COM} = V_{SAT}/2$, we get the prepulse voltages:

$$\begin{aligned} V_2 &= V_3 + (V_3 - V_1)\cdot\frac{C_{GD,\max}}{C_S}\cdot\frac{C_{GD,\min} + C_{LC,\max} + C_S}{C_{GD,\max} + C_{LC,\max} + C_S} \\ &\quad + \frac{V_{SAT}}{2}\cdot\frac{C_{GD,\min} + C_{LC,\max} + C_S}{C_S} \\ &\approx V_3 + (V_3 - V_1)\cdot\frac{C_{GD,\max}}{C_S} + \frac{V_{SAT}}{2}\cdot\frac{C_{GD,\min} + C_{LC,\max} + C_S}{C_S} \end{aligned} \tag{5.50a}$$

$$V_4 = V_3 + (V_3 - V_1)\cdot\frac{C_{GD,\max}}{C_S}\cdot\frac{C_{GD,\min}+C_{LC,\min}+C_S}{C_{GD,\max}+C_{LC,\min}+C_S} - \frac{V_{SAT}}{2}\cdot\frac{C_{GD,\min}+C_{LC,\min}+C_S}{C_S} \approx V_3 + (V_3 - V_1)\cdot\frac{C_{GD,\max}}{C_S} - \frac{V_{SAT}}{2}\cdot\frac{C_{GD,\min}+C_{LC,\min}+C_S}{C_S} \quad (5.50b)$$

We show in Fig. 5.28 the driving and pixel voltages in the case of Frame Inversion.

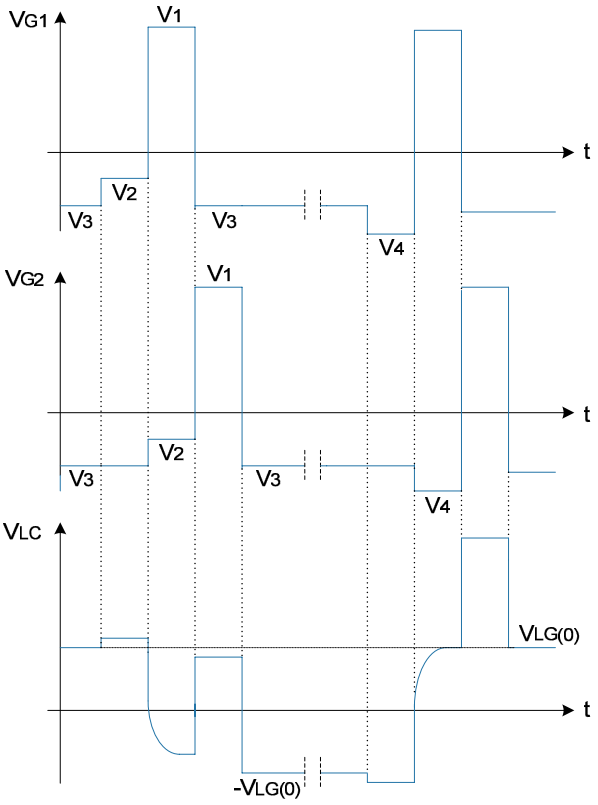


Fig. 5.28 Driving and pixel voltages in the case of 4-level driving scheme. Frame Inversion is considered

The advantage of the 4-level approach derives from the use of a low-voltage source driver and a constant V_{COM}, but a complex gamma correction to eliminate the kickback dynamic component. The approach is compatible only with Cap-on-Gate panels. Finally, either by increasing (for positive-polarity frames) or decreasing (for

negative-polarity frames) by the same amount all the ON pixels, it is possible to implement only those inversion methods in which the pixels of a given row have the same polarity, that is Row and Frame Inversion.

5.6 Concluding Remarks

The AMLCD industry has rapidly attracted a great interest by producers and originated a vast excitement in the consumers, so that now it has become an upstream dominant industry. As first investments were made in Japan and subsequently in Korea, Taiwan and recently in China, virtually all AMLCD panel fabrication lines are located in Asia. At the time of writing AMLCDs have penetrated completely the PC notebook market and by more than 50% that of PC monitors, while the TV sector represents the greatest potential of growth (in 2007, the number of LCD-TVs sold worldwide overcome that of CRT-TVs). This impressive and successful expansion has been possible thanks to the efforts of all divisions of the industry, from the manufacturers to component and equipment suppliers.

In this chapter we summarized the a-Si and poly-Si TFT electrical behaviors, we described the AMLCD panel structure and focused our attention on the dominant driving approaches. Conventional inversion polarity techniques were analyzed in detail with their related power consumption issues. Pre-emphasis and kickback compensation methods were addressed as well.

Based on these considerations, we can anticipate the first main differences between drivers for PMLCDs and AMLCDs:

(1) The pixels do not respond to average voltages, frame response effect is absent and MLA techniques are no longer required;

(2) Gray levels are generated by means of the sole source voltage (and not on both row and column voltages, as for PMLCDs), therefore an accurate Digital-to-Analog conversion is mandatory to obtain a source voltage from a digital RGB information. PWM techniques are no longer required;

(3) Due to the higher data transfer rates, low-speed serial interfaces cannot be used because are too slow.

To conclude the discussion, we briefly describe some further methods that have been devised to improve AMLCD picture quality. They are based on the human vision perception system[6] [YW2000, SAK2006, SL2007]. Of course, most of these techniques are meant for LCD TVs, but it is expected that they will be rapidly transferred to high-performance portable multimedia devices as well.

The first two approaches we treat are driving methods aimed to reduce the *motion blur* and in general to improve the quality of moving pictures [M2004].

[6]It is now recognized that optimized display performance can be only achieved by the understanding of the human color perception (see Appendix D), preferences, perceptible maximum contrast level (in general viewing circumstances and not only in dark rooms), and so on.

Studies on the human visual system show that the conventional display-and-hold driving method of LCDs, which maintains the previous frame image information for about 16.7 ms (=1/60 Hz) until the subsequent frame image, is the cause of *afterimage formation* on the retina and, in turn, the origin of motion blur perception [K2001, IYT2003]. This drawback is absent in CRTs with their inherent impulsive driving behaviour. Note that motion blur cannot be eliminated even if the LC response time approaches zero. This explains why, despite the use of progressively faster LCs and pre-emphasis techniques, we have now reached a limit in reducing motion blurring. The amount of afterimage on the human retina can be further reduced only by decreasing the frame time duration.

Fast Frame Rate (FFR) driving (i.e., the use of a frame frequency of 120 Hz) is at this purpose the most straightforward method [LSP2005, OIM2005], though there are issues to resolve in order to contrast the temperature increase in the data driver ICs without affecting the system cost.

Impulsive Driving is an attempt to recreate the CRT behavior through either *Black Data Insertion* [YKI2005, YTI2006] or *Backlight Blinking* [FNC2001, HST2001]. The former is based on the insertion of black data subframes between two consecutive video frames and is implemented via software. It takes advantage of the fast gray to black response of recent LC mixtures. For slower LCs the same effect can be simulated by pulsing the backlight. The technique is implemented via hardware through the backlight inverter and was proposed already in 1998 by a group of Japan Broadcasting Corporation (NHK) headed by Taiichiro Kurita [KSY1998]. To be effective, residual light leakage during the backlight turning OFF must be minimized. As a main drawback, both approaches reduce the overall display luminance.

Research has been carried out to improve also contrast and color reproduction.

LCDs provide reduced contrast when displaying very bright or very dark images. **Dynamic gamma** can be used to overcome this drawback. In this approach the gamma curve is adjusted on a frame by frame basis depending on the image content.

Another promising approach for contrast improvement is the **Backlight Dimming**, [SHS2004, SKT2005, SM2006], in which the whole screen is divided into some areas and LEDs are assembled on each one with independent brightness control function. The backlight intensity of different areas is hence separately controlled based on input video signal levels. A 100 000:1 contrast ratio was reported using this method [SHS2004], which takes advantage of the LEDs fast response. This approach allows reducing the power dissipation of the backlight as well. The better LED color property[7] will also improve color gamut in LCD TVs. To be completely exploited, this would require the introduction of an additional primary color (most probably Yellow) together with the traditional three RGB primaries (**Multi-Primary** color displays) [ELS2005, SL2007].

[7]A typical CCFL backlight will enable an LCD display to reproduce 60% of the colors that can be transmitted using an NTSC signal (see Appendix D). RGB LED backlight has the better color coverage spectrum (color gamut), which is about 110% NTSC (that of White LED is about 70–80% NTSC). Unfortunately, RGB LED backlight has the highest power consumption [CCC2007].

All these techniques are very important for the rapidly growing markets of LCD-TVs and home PC multi-media stations, where image quality is going to become a key factor. On the other side, the market pressure to reduce cost for mainstream desktop monitors (adopted massively by business companies for text and graphics usage) will cause a limited adoption of the above techniques into low-end displays. However, several improvements are foreseen also in the area of mobile AMLCD drivers. For example, Solomon Systech Ltd. (Hong-Kong), outlined the coming advances summarized in Table 5.3 already at the end of 2006.

Table 5.3 Some improvements expected in mobile LCD driver ICs [S2006a]

Features	Present	Coming advance
Resolution	QVGA	VGA
DAC	6-bit gray scale	8-bit gray scale
Motion	Pre-emphasis	Pre-emphasis and Black Data Insertion
Interface	Parallel and SPI	Custom parallel and high-speed serial*
Backlight	No control	LED Backlight Dimming
Contrast	No adjustment	Automatic adjustment according to ambient light level.
Touch panel	High-end feature	Popular feature

*High-speed serial interfaces are discussed in the next chapter.

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