Chapter 4

Drivers for Passive-Matrix LCDs

This chapter is devoted to the description of reliable architectures and circuit solutions suitable to efficiently implement *drivers* for passive-matrix LCDs. Since passive-matrix LCDs have a limited number of rows and columns (the present maximum resolution for hand-held devices adopting passive-matrix LCDs is the Quarter-VGA having 320 rows×240 columns), the driver is commonly a single-chip[1] mixed-signal integrated circuit (**driver IC**). It includes as main functionalities: microprocessor interface, control logic, display memory, temperature compensation, voltage-level generation/regulation, and drive (row and column) outputs.

It is worth noting that research has continuously produced new materials suitable for display applications, even substantially different from LCs (see Appendix A for alternative flat panel technologies). These materials need driving circuits with somewhat different requirements than those treated here [L2001]. Nevertheless, the architecture discussed here is conceptually of broad application and many of the building blocks presented are of general significance.

In this chapter the typical driver IC architecture is introduced in section 4.1. A discussion of the constituting blocks is performed in Sections 4.2–4.6. The features required to the IC fabrication technology suitable for the application are described in Section 4.7. Finally, a survey on the chip assembling methods is given in Section 4.8.

4.1 Driver Architecture

It was described in Section 3.2 that single line or multiple line addressing approaches are possible in PMLCDs. CSTN LCDs often adopt the MLA technique which offers the best performance. For this reason, unless otherwise stated, we will consider this driving approach in this chapter.

[1]Because of the greater number of rows and columns, large-area (active-matrix) LCDs cannot be driven by a single chip which would require an unfeasible number of pins. As we will see in Chapter 6, they adopt a different architecture made up of a controller board and several row and column driver ICs.

D.J.R. Cristaldi et al., *Liquid Crystal Display Drivers*, DOI 10.1007/978-90-481-2255-4_4,

The generic block diagram of a passive-matrix LCD driver[2] is illustrated in Fig. 4.1. Other than the LCD panel, that is represented for reference as it does not belong to the driver, we have indicated as main blocks the **Host Interface**, **LUT** (Look-up Table)/**Dither**, Display Data **RAM**, **Color Processing**, **MLA and Grey Generation**, **Control Logic**, **Timing Controller**, **OTP** (One Time Programmable) **Memory**, **Oscillator**, **Temperature Sensor**, **Temperature Compensation**, **DC/DC Converter**, and finally **Column and Row Drivers**. It is worth mentioning that some block functions have distributed allocation when actually implemented, but are here described as concentrated for the sake of clarity. Also, the diagram does not include the power supply, but two external supplies are usually required: one for the host interface and the other for the DC/DC converter and analog blocks. The value of the former is related to the voltage levels adopted by the standardized signalling approach (usually, it is equal to 1.8 V), the latter depends on the silicon process utilized and is somewhat higher (e.g., 2.8 V). Today there is a certain tendency to adopt only a single supply, but this trend has not produced standardization yet.

Some of the blocks included in Fig. 4.1 perform functions already explained in the previous chapter and should be familiar to the reader, other blocks and their related functions will be explained in the following.

Data coming from a micro controller unit (MCU host) can represent either commands or video information. They are initially interfaced and prepared to be respectively interpreted (by the Control Logic section) or stored (into the RAM). Video data are also optimized through Color Processing techniques (e.g., Gamma Correction). On-chip oscillators and stabilized DC voltage generators are also necessary for synchronization and generation of accurate reference voltages. Proper biasing with high-voltage boosting circuits is also required to generate pixel voltage levels greater than the supply one. Column and row voltages are finally provided as outputs through the Column and Row Drivers.

The implementation of all these functions should be optimized to contain chip size and cost,[3] as well as the required number of external components, such as capacitors used by the voltage multipliers (pumping capacitors) or needed to absorb large current spikes (bypass capacitors). Reduction of power consumption[4] and crosstalk with enhanced protection to electrostatic damage (ESD) are also important issues. Lastly, easily programmable display features are often desirable from the end user. As a result, both the utilized silicon process with its minimum lithographic resolution (0.18–0.25 μm are common) and the adopted circuit design techniques play an important role in the driver economy considering that, owing to the great number of output channels, the aspect ratio of the die is usually high (e.g., 20 mm×1 mm). However, unlike one could be induced to think by the large number of output pads, an IC driver for small-area LCDs is not PAD limited for two main reasons:

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[2]Another electrical section, the backlight inverter (a DC/AC converter) is present in an LCD, but it is implemented as a separate circuit.

[3]Given the strong competition in the flat-panel display market, the cost is perhaps the most crucial parameter. Thanks to the scaling-up and technological simplification the price of mobile devices has been steadily decreasing by approximately 30% a year.

[4]Power consumption of PMLCD drivers for mobile applications is usually around 2 mW.

(1) With the evolution of the market and technologies, the display manufacturers have reduced the assembly pitch to follow the lithographic scaling of silicon driver technologies.

(2) High-performance AMLCDs are potentially PAD-limited, but they may adopt LTPS technologies that allow the PAD number to be reduced thanks to the implementation of multiplexers directly on the glass. At this purpose, a single column line instead of three for the RGB subpixels is typically adopted; and some manufacturers have succeeded in implementing a 12-to-1 MUX.

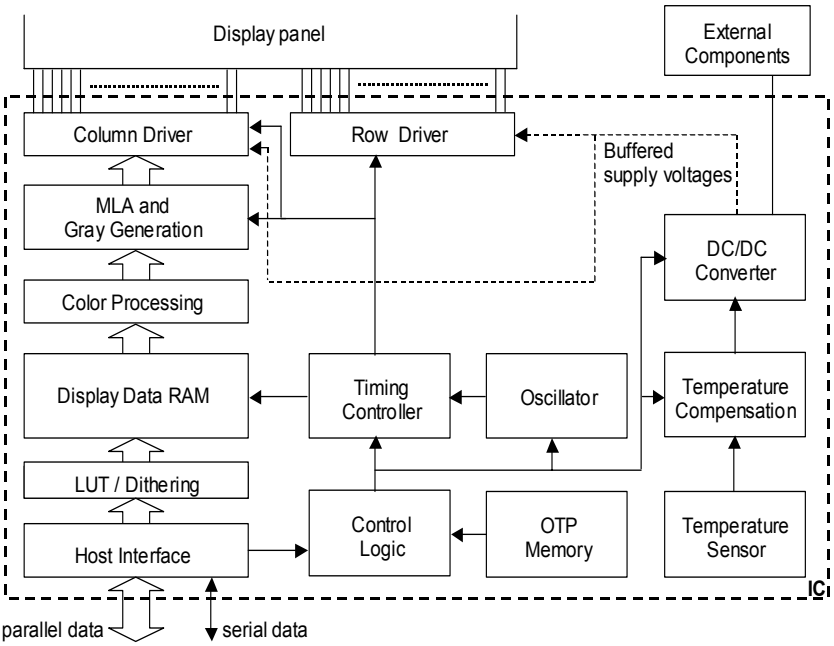


Fig. 4.1 Block diagram of a PM-LCD driver IC (*within dashed box*)

In the following sections we will explain in detail the behavior of a PMLCD driver by grouping its functions into 5 main categories, namely: (1) Host Interface, (2) Power Manager, (3) Driver Manager, (4) Image Processing and (5) Output Drivers.

4.2 Host Interface

4.2.1 Interfaces

Image data and commands are transferred from the MCU host to the driver, whereas diagnostic data and state information (e.g., driver ON/OFF condition) are transferred from the driver to the host. A bidirectional data link between the MCU and the driver is hence required. At this purpose, either parallel type or serial type communication interfaces have been exploited. In presence of multiple standards, to maximize flexibility and easy of use, a general driver IC is equipped with the most

popular industry standard host bus interfaces such as the (parallel type) **68 000** and **8080** and (serial type) **3 lines 9 bit** and **4 lines SPI** (Serial Peripheral Interface).

The two well-known parallel-type interfaces (introduced by Motorola and Intel, respectively) were the first exploited. A detailed description of these interfaces is beyond the scopes of this book. Here it is sufficient to say that they adopt CMOS standard signalling levels (that have progressively reduced from 3.3 V, 1.8 V, and in the next generation products to 1.2 V) and provide maximum speed rates up to 20 MHz for each channel.

Note that from the physical point of view, speed is ultimately limited by the RC time constant of the connection lines. However, the transfer rate between the host and the driver has significantly increased over the last years, to support the progressive migration of displayed data from text, to images, video, and full color compatibility. At this purpose, parallel-type interfaces were the first adopted for their higher transfer rates obtained by transmitting more bits in parallel. The main drawbacks of parallel connections are related to their cost and high exposure to mechanical breaks (of bus lines and connector contacts), which obviously may harm the whole system. The aforementioned problems are considerably reduced by adopting serial type interfaces, as they require a limited number of physical lines and are thus cheaper and more reliable.

We have mentioned two serial-type interfaces. These are briefly described below:

– 3 lines 9 bit from Nokia
the three lines are used for *enable*, *clock*, and *data*, the latter being in the 8-bit format plus 1 additional bit for datum/command discrimination.

– 4 lines Serial Peripheral Interface (SPI)
the function of the first three lines is the same as above, the fourth line is used for datum/command discrimination. Data are in the 8-bit format.

It should be observed that these are just two examples, since new interfaces are continuously developed. For example, Motorola adopts another interface type that uses 16 bit. The first 8 bit are used to code the command and the remaining 8 bit represent the data. It simplifies the subsequent elaboration task but can be less efficient for long data series transfer.

In conclusion, it is worth noting that these “low-speed” serial interfaces are typical of PMLCDs, owing to the limited data-transmission rate required. High-speed serial interfaces, required by AMLCDs, will be discussed in Section 6.2.

4.2.2 LUT/Dithering

Before being stored into the RAM, data at the output of the host interface may be remapped to fit the RAM word length. Two techniques may be needed: *insertion of additional bits* and *rounding*.

The former approach is required if the data length is smaller than the RAM word length. In this case, we need extending a reduced data color depth into the maximum one dictated by the RAM through a **Look-Up Table** (LUT) that is an associative array giving an output value for each of a range of index values. The LUT is also called *color map* or *palette*.

For example, consider a 18-bit RAM and 8-bit video data (as in the first case illustrated in Fig. 4.2). Assume that a number of 3 bit are used for Red and Green colors and 2 bit for Blue (3R 3G 2B). Data can be hence remapped to employ all 18 bit (6R 6G 6B). Other examples are included in Fig. 4.2.

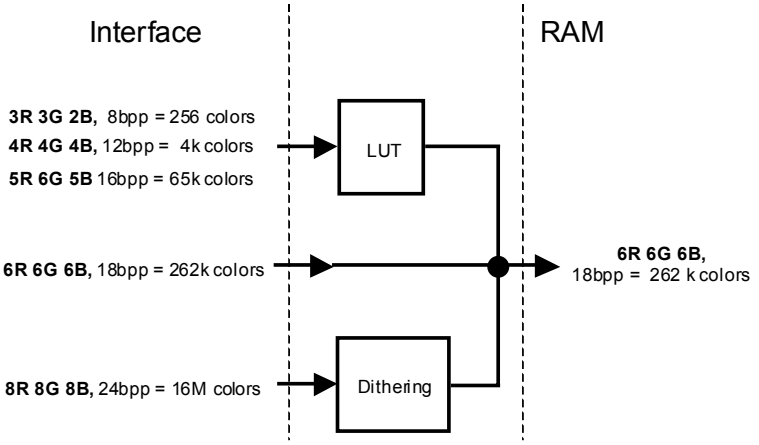


Fig. 4.2 Example of LUT/Dithering operation required in the case of a 18-bit video RAM

On the contrary, when the incoming data word length is greater than that allowed by the RAM we need to reduce the color depth, as illustrated in the last case of Fig. 4.2. At this purpose, the easiest solution is to truncate some bits. However, truncation may cause a significant error in the displayed image, like the generation of false contours. To limit this problem, several rounding (**dithering**) techniques have been developed such as conventional rounding, error feedback rounding, and dynamic rounding [J2001]. For example, error feedback rounding is performed by storing the residue of a truncation and adding it to the next addressed pixel. It substitutes less visible noise-like quantizing errors instead of contouring artefacts of simple truncation. An implementation scheme is shown in Fig. 4.3 where data word length is reduced from 16 to 8 bit. Note that the register included in the feedback path produces 16-bit output word in which the eight most significant bits are "0" and the remaining 8 bit are the 8 LSB of the previous output word.

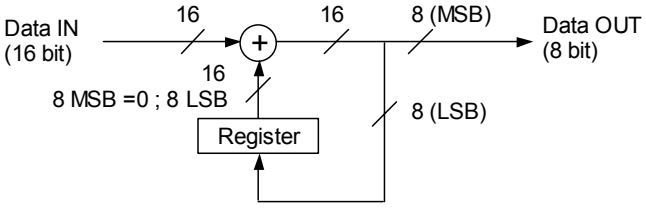


Fig. 4.3 Example of dithering algorithm using error feedback

4.3 Power Manager

The Power Manager section is devoted to the generation of all the bias and reference voltages (and currents) required by the driver circuits. Especially for hand-held devices, that can be subjected to dramatic temperature excursions during normal operation, it is essential that the reference voltages are temperature stabilized. The use of color graphics also worsens this problem since the color quality heavily depends on the absolute value of the LC threshold voltage and on the accuracy of the driving voltage level.

4.3.1 Temperature-Compensated Voltage Generator

All the internal reference voltages are generated from a reference bias circuit that is temperature compensated. A DC voltage, independent of temperature, is obtained through well-established circuits called *bandgap references*.[5]

A **bandgap** reference voltage has nominal zero temperature dependence as it is obtained by summing two voltages with proper weighting that have respectively negative and positive temperature coefficients. These voltages rely on the exponential voltage-to-current law of bipolar devices, for both positive (thermal voltage, V_T) and negative (base-emitter voltage, V_{BE}) temperature coefficients [W1971, K1973, B1974, BSU1999, MMF2001, GPC2003].

A bandgap reference circuit can be implemented in CMOS technologies by exploiting the inherent parasitic bipolar devices. Two examples of bandgap voltage generators are illustrated below.

The voltage reference in Fig. 4.4 is based on a differential amplifier. The bias currents, I_{C1} and I_{C2}, are set equal by imposing equal voltage drops across both the resistors R_3 and R_4 exploiting the virtual ground of the OpAmp.

Design equations are

$$I_{C1,2} = \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{V_T}{R_2} \ln\left(\frac{A_{E2}}{A_{E1}}\right) \tag{4.1}$$

$$V_{REF} = V_{BE1} + 2R_1 I_{C1,2} = V_{BE1} + 2V_T \frac{R_1}{R_2} \ln\left(\frac{A_{E2}}{A_{E1}}\right) \tag{4.2}$$

This circuit requires that npn BJTs are available in the adopted CMOS technology.

[5] As known, this terminology is due to the fact that limit for T->0 K of the obtained reference voltage is the *bandgap* voltage of silicon.

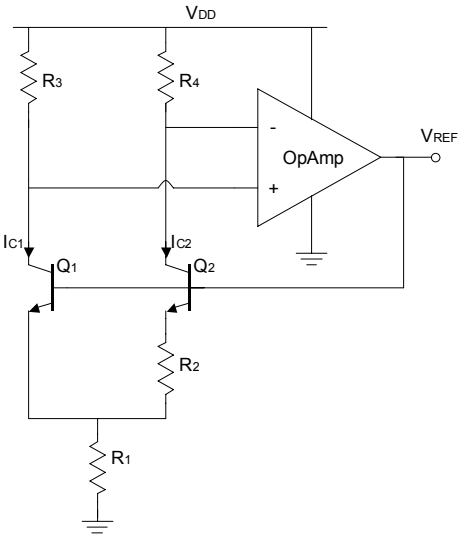


Fig. 4.4 Bandgap voltage reference with bipolar transistors

The circuit topology shown in Fig. 4.5 is fully compatible with a CMOS technology, because the npn transistors can be replaced by pnp or even simple pn junctions. Assuming the circuit properly biased, voltage V_{REF} is set to $V_{BE1}+(R_1+R_3)I_{C1}$. Considering the virtual ground of the OpAmp, current I_{C1} can be found by inspection and results in

$$I_{C1} = \frac{V_T}{R_3} \ln\left(\frac{A_{E1}}{A_{E2}} \frac{I_{C2}}{I_{C1}} \right) \tag{4.3}$$

The virtual ground also forces the voltage drops across R_1 and R_2 to be equal, that is $I_{C1}/I_{C2}=R_2/R_1$. Substituting this expression in (4.3), V_{REF} results to be

$$V_{REF} = V_{BE1} + V_T \left(1 + \frac{R_1}{R_3} \right) \ln\left(\frac{A_{E1}}{A_{E2}} \frac{R_1}{R_2} \right) \tag{4.4}$$

Generally, transistors Q_1 and Q_2 are equal so that their emitter ratio is unitary and the output voltage mainly depends on resistive ratios.

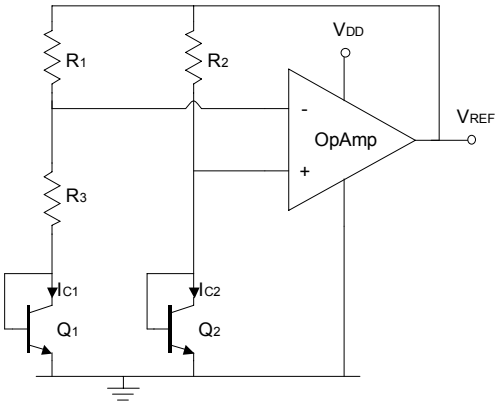


Fig. 4.5 Bandgap voltage reference circuit compatible with CMOS technologies

Figure 4.6 shows a typical behavior of the voltage versus temperature obtained by such circuits. They provide a temperature drift performance in the range of about 20–100 ppm/°C.

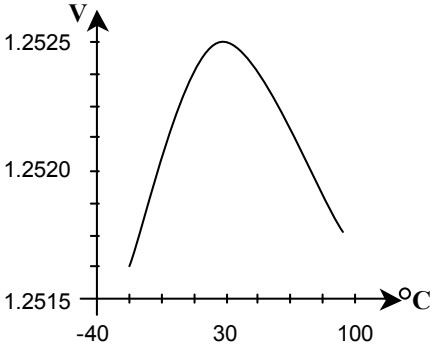


Fig. 4.6 Typical behavior of bandgap reference voltage versus temperature

4.3.2 Temperature Sensor

It was explained in Section 2.2.2 that the electro-optic (T/V) characteristic is dependent on the temperature. This problem is illustrated in Fig. 4.7a, where three curves are plotted for different temperatures $T_1 > T_A > T_2$, where T_A is the ambient temperature (be careful that letter T is used for both Transmittance and Temperature). From the figure it is seen that V_{TH} (and also V_{SAT}) decreases with the temperature, this is because the viscosity of the LC mixture decreases with the temperature and hence a reduced energy is required for the realignment. More specifically, the typical curve of V_{TH} versus temperature for STN LCDs is illustrated with solid curve in Fig. 4.7b.

As described in (3.18) and (3.19), V_{LCD} is proportional to V_{TH}, therefore in order to avoid that display contrast is affected by temperature variations, V_{LCD} must follow the same V_{TH} temperature behaviour. At the system level, V_{LCD} can be reconstructed by a piece-wise curve. This allows a simplification of the design and the minimization of data stored in the OTP. For example, the dashed curve in Fig. 4.7b represents one of the possible implementations of the curve into three segments having two intersections at temperatures T_L and T_H. T_L and T_H as well as the slopes of the three segments can be fine-tuned by the module maker according to the adopted LCD mixture and then stored in the OTP.

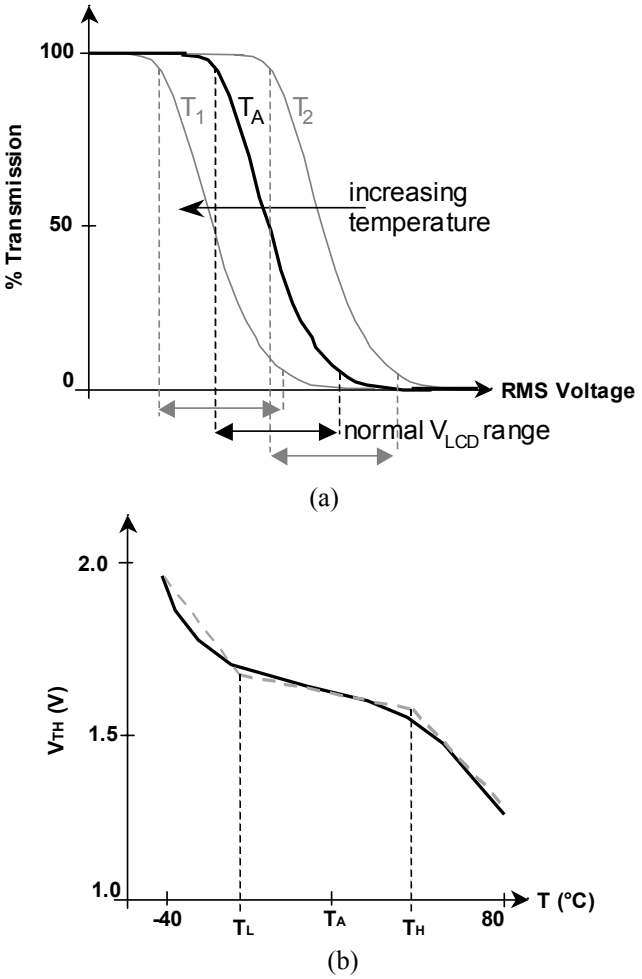


Fig. 4.7 (**a**) Electro-optic transfer function for three different temperatures, $T_1 > T_A > T_2$, highlighting the associated V_{LCD} ranges. (**b**) Threshold voltage versus temperature (*solid line*), and a possible segmentation (*dashed line*)

A temperature sensor is used to monitor the junction temperature of the driver, which is supposed to be very close to the display temperature. This information is

used not only in the block that generates the temperature segmentation of V_{LCD}, but also to change the frame frequency adapting it to the operating conditions of the LCD mixture. A possible block diagram of a temperature sensor is shown in Fig. 4.8.

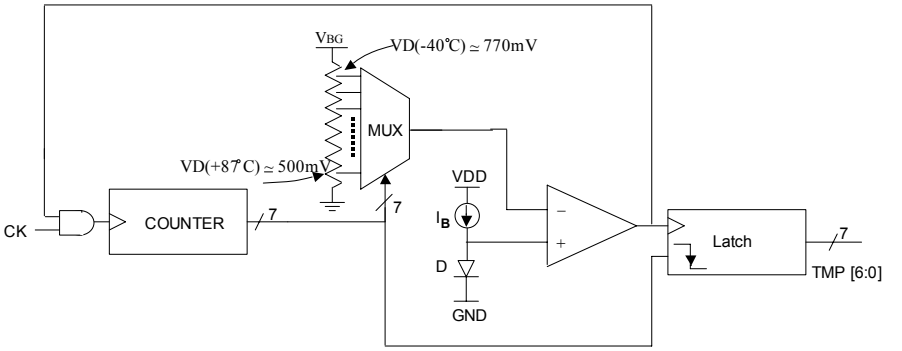


Fig. 4.8 Block scheme of the Temperature Sensor

CK is a synchronization signal coming from the Local Oscillator and feeding the 7-bit Counter. If the input feedback voltage at the AND gate is high, then the Counter output is increased by 1 bit at each clock pulse. The Counter output is then converted to an analog voltage through the resistor-string DAC and compared with the junction voltage of diode, D. The diode is forward biased through a constant current I_B and its useful voltage range is comprised between $V_D(-40°C) = 770$ mV and $V_D(+87°C) = 500$ mV with a slope of –2 mV/°C. As far as the DAC output voltage is higher than the diode voltage, the counter will increase its output. The count up is stopped as soon as the output comparator switches down and the counter result is transferred to the Latch Register.

Observe that the DAC output corresponds to 770 mV for the lowest input word, 00HEX (i.e., the output voltage decreases for increasing input word).

A digital low pass filter can be inserted after the Latch Register to average the temperature value over a few (e.g., 4) acquisitions.

With a 7-bit variable TMP[6:0], the temperature ranging from the minimum value, –40°C, to the maximum 87°C can be detected with a resolution of 1°C.

Finally, the expression of the segmented V_{LCD} as a function of the temperature is given by

$$V_{LCD} = \begin{cases} V_{LCD,TA} + (T_L - T_A)S_{TA} + (T - T_L)S_{TL} & \text{for} \quad T < T_L \\ V_{LCD,TA} + (T - T_A)S_{TA} & \text{for} \quad T_L < T < T_H \\ V_{LCD,TA} + (T_H - T_A)S_{TA} + (T - T_H)S_{TH} & \text{for} \quad T > T_H \end{cases} \tag{4.5}$$

in which $V_{LCD,TA}$ is the nominal V_{LCD} voltage at ambient temperature, whereas S_{TA}, S_{TL}, and S_{TH} are the slopes of the segments defined by the module maker and stored in the OTP. Figure 4.9 illustrates an example of the segmented V_{LCD}. In the figure

are also included V_{LCD,TA_MAX} and V_{LCD,TA_MIN}, that are the boundaries of the range in which V_{LCD} may vary as a function of the threshold voltage and the number of display rows. In general, for a color STN LCD with 128 rows the maximum V_{LCD} variation at ambient temperature is comprised between 5 V and 15 V.

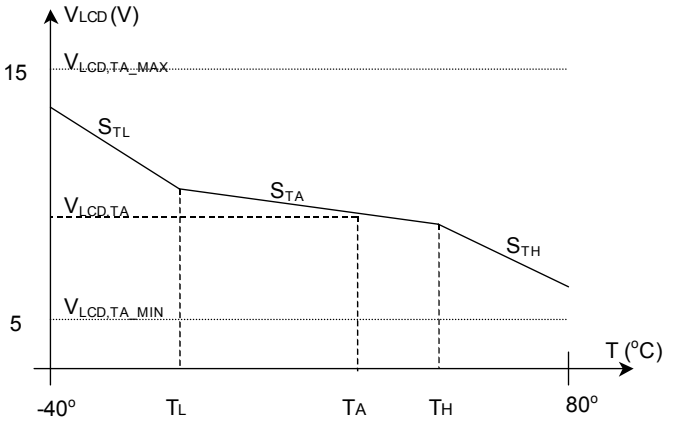


Fig. 4.9 Example of a segmented temperature programmable V_{LCD} voltage. The temperature range is split into three segments. Parameters $V_{LCD,TA}$, S_{TL}, S_{TA} and S_{TH} are the only stored into the OTP

4.3.3 DC/DC Converter

For battery-operated portable devices, the external supply is kept low to contain power consumption, therefore integer multiplication factors (×2, ×3, ×4 and even more) in both positive and negative amplitudes are required to generate the row and column voltages. A DC/DC converter that uses only switches (diodes originally) and capacitors is referred to as charge pump [D1976]. This inductorless architecture is amenable for integration and causes relatively low electromagnetic interferences (EMI). It is popular in low noise applications such as EEPROM, implantable pacemakers and, of course, small-size (up to around 8 in.) LCDs [GP1996, M1997, WW1998, YKC2003, SK2008].

The simplified scheme of a voltage multiplier ideally providing an output voltage, V_{out}, equal to $3V_{DD}$ is depicted in Fig. 4.10. The circuit includes three stages, each made up of a diode and a capacitor. C_{IN} models the input generator capacitance, while C_{P1} and C_{P2} are the **pumping capacitors** and C_B is the **bulk capacitor** with function of storage and filtering, acting as a voltage generator for the load. A square-wave oscillator provides two phases that drive one terminal of the pumping capacitors. After a certain transient, dictated by the charging time of the generator-diode-capacitor system and the frequency of the oscillator, C_{P1} is charged to V_{DD}-V_D, and C_{P2} to $2V_{DD}$-$2V_D$ and C_{OUT} to $3V_{DD}$-$3V_D$, in which V_D is the diode voltage drop. The typical behavior of V_{OUT} is depicted in Fig. 4.11. More details on charge pumps can be found in Chapter 7.

Fully integrated multipliers (i.e., without requiring external components) are of course preferred. But this depends on the current drive capability required. Indeed, to obtain large output currents we need large out-of-chip capacitors to avoid fast discharging.

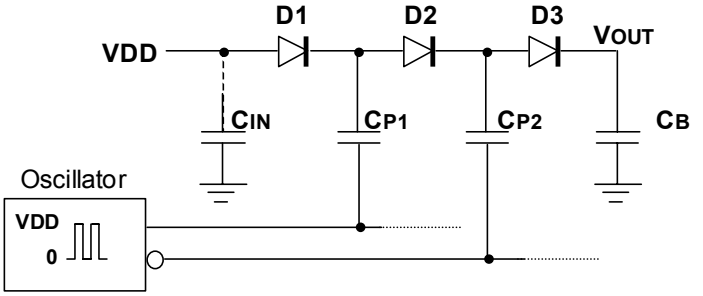


Fig. 4.10 Simplified scheme of a ×3 charge pump

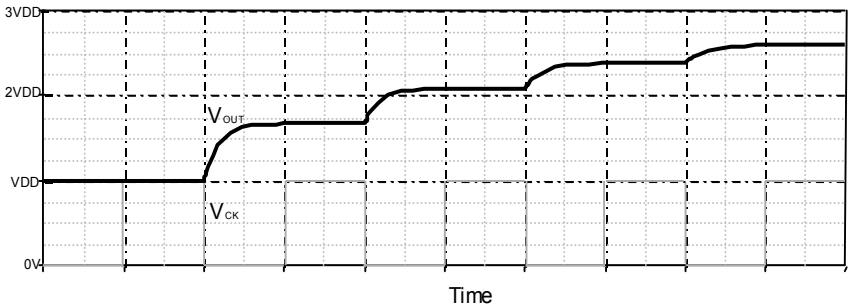


Fig. 4.11 Typical behavior of charge pump output voltage, V_{OUT}, and square wave, V_{CK}

Observe that owing to the high-valued bulk capacitor, a buffer amplifier is not needed to drive the row/column loads. This is instead required for voltages that are obtained by resistive partition. At this purpose, see Fig. 4.12 that illustrates a possible way to generate the voltages for a MLA-4 LCD.

The scheme generates the six required supply voltages $\pm V_R$, $\pm V_C$, and $\pm V_C/2$ (V_{COM} is the common voltage externally connected to ground). Four of them, $\pm V_R$ and $\pm V_C$, are obtained from charge pumps configured in closed loop, CP1, CP2, CP3, CP4, respectively. Each loop being constituted by an error amplifier, a voltage-controlled oscillator (VCO), and a charge pump. The loop works as follows. Consider for instance the loop generating V_R, and assume that it tends to decrease because of the load current demand. Then, also V_R' decreases, the output voltage of the error amplifier EA1 increases as well as the VCO1 frequency and, as a result, CP1 pumps more charges to its bulk capacitor, increasing (regulating) V_R.

The other two voltages, $\pm V_C/2$, are obtained from simple resistive partitioning (resistors R_1–R_2) followed by a Linear Drop-Out Regulator (LDO) buffer. Buffer B1 is supplied between $+V_C$ and V_{COM}, whereas buffer B2 is supplied between V_{COM} and

$-V_C$. Two de-multiplexers and resistive dividers are also embedded into the above mentioned feedback loops. Their role is to set proper row, $+V_R$, and Bias Ratio, defined in (3.10), through coded words V_{LCD}[…] and BR[…]. The last resistor divider (R_5–R_5) is used to generate $-V_R$ from $+V_R$.

It is important to observe, in conclusion, that this architecture adopts a *centralized* driving voltages buffering, as opposite to the *distributed* buffering approach that is usually followed in AMLCDs (see Section 6.3.1).

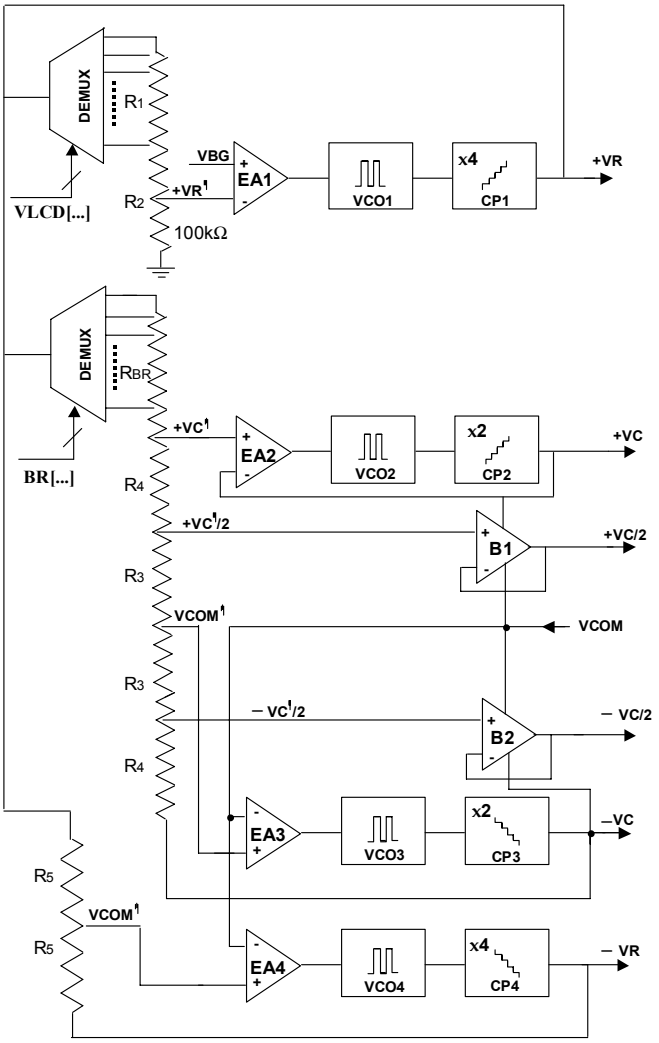


Fig. 4.12 Power Supply for LCD driver using MLA-4 technique

4.4 Driver Manager

4.4.1 One Time Programmable Memory

We have seen that the effectiveness of the LCD matrix in color reproduction depends mainly on the absolute values of parameters such as the LC threshold voltage and on the accuracy of the driving voltage levels. Any tolerance of these values must be hence compensated for. This task is performed by recording permanently in a dedicated non-volatile memory block the value of critical parameters, such as characteristics of the LC mixture, gamma curve data (see Section 4.5.2), the values of the reference voltages, etc., as well as configuration parameters. At this purpose, it is used a Memory called OTP (One Time Programmable) memory which can be implemented in a poly-fuse or anti-fuse technology.

The values of the aforementioned parameters are first measured by the module makers, for each production lot of LC mixture, as these may change from one lot to another one, and then written in the OTP. For instance an OTP word can be 22 bit long: 16 are used to code effective data and 6 are used to implement an Error Correction Code (ECC).

After each system reset or power on, the OTP is automatically initialized. Parameters stored in the non-volatile memory are read and latched in a volatile register situated in the Control Logic section (discussed in Section 4.4.3) and then the OTP is switched off to avoid current consumption. In the end-user application there is the possibility to upgrade the parameters stored in the OTP. This depends on the status of a "Protection Mode" bit present in the OTP. If it is low, said parameters can be upgraded, if it is high, the parameters cannot be upgraded.

4.4.2 Oscillator (Internal Clock Generator)

An internal oscillator, preferably fully integrated (without requiring external components) is included in the driver IC. It generates the master clock signal (at the maximum frequency), from which all the other synchronization signals are derived by frequency division.

A possible scheme of a relaxation oscillator is shown in Fig. 4.13 [P2002]. It is made up of two capacitors C_1 and C_2 alternatively fed by two constant current sources, I_{OSC}, or discharged by MOS transistors, M_1 and M_2, acting as switches. Assuming one of the switches (e.g., M1) be OFF, then the voltage across the associated capacitor increases linearly with the law $(I_{OSC}/C_1)t$ and when it reaches the threshold, V_{TH}, of M1A the drain voltage of M1A goes to "0" as well as the outputs of NOT_3 and NOT_5 (output). Hence, M1 is switched ON and C_1 is discharged, while M2 is switched OFF and capacitor C_2 starts to charge with the same law as C_1. Assuming a duty cycle of 50%, $C_1=C_2=C$, and the oscillation frequency is given by

$$f_{OSC} = \frac{I_{OSC}}{2CV_{TH}} \tag{4.6}$$

and is electrically controlled by I_{OSC}. For instance, assuming V_{TH}=0.8 V, a 5-MHz oscillation frequency is obtained with I_{OSC}=8 μA and C=1 pF.

Observe that M1A and M2A perform logically as NOT gates, but they are in common source configuration in order to provide a threshold voltage independent of V_{DD} and to limit the cross-conduction current to I_B.

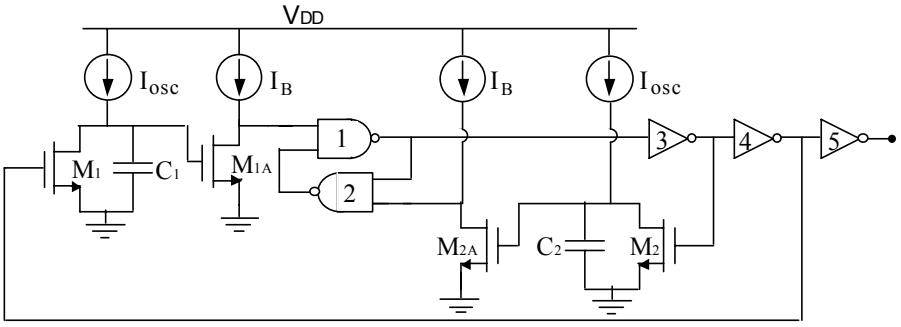


Fig. 4.13 Schematic of a relaxation oscillator [P2002]

Current I_{OSC} must be accurately set starting from the bandgap voltage, V_{BG}, an adjustable resistor and current mirrors, as illustrated in Fig. 4.14. Voltage V_{REF} is derived from V_{BG} by resistive partition and replicated across R_{ADJ}, where I_{REF} is generated ($I_{REF}=V_{REF}/R_{ADJ}$). R_{ADJ} is a resistor tuned during testing procedure to compensate for process variations in mass production.

The multiplexer, MUX, is usually implemented through a binary-tree selector (a three-bit version is depicted in Fig. 4.15).

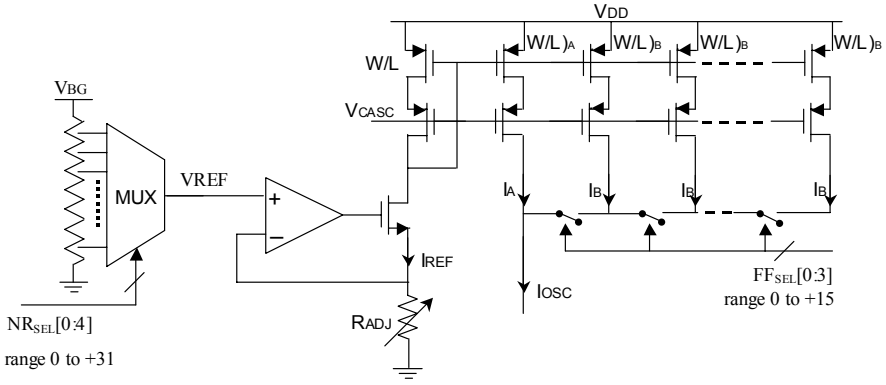


Fig. 4.14 Scheme for the generation of I_{OSC}

Referring to Fig. 4.14, if $I_A=k_1I_{REF}$ and $I_B=k_2I_{REF}$ we write the expression of I_{OSC}

$$I_{OSC} = I_A + FF_{SEL} \cdot I_B = I_{REF}\left(k_1 + k_2 \cdot FF_{SEL}\right) \tag{4.7}$$
$$= \frac{NR_{SEL}}{N}\frac{V_{BG}}{R_{ADJ}}\left(k_1 + k_2 \cdot FF_{SEL}\right)$$

where N is the number of display rows, NR_{SEL} is a 5-bit control word that represents the subset of addressable rows (the user may operate only a portion of the display rows, this mode is usually referred to as *partial display mode*). FF_{SEL} is a 4-bit control word that represents the preferred frame frequency (required for instance to set the idle mode, or to allow frequency change with the temperature and LC mixture). Both are stored in the OTP and tuned by the module maker.

In conclusion, the above equation shows that the oscillation frequency can be set according to the addressable rows and frame frequency selected.

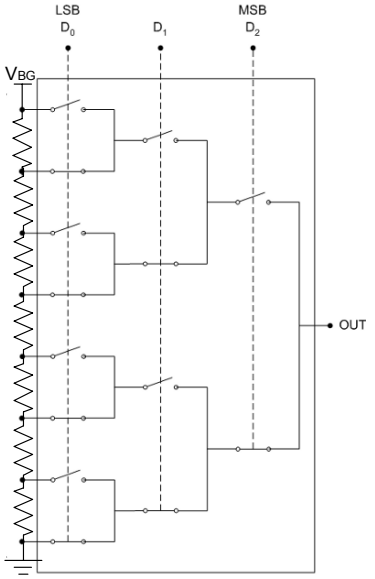


Fig. 4.15 String resistor DAC with three-bit multiplexer (MUX) scheme

4.4.3 Control Logic

The principal task of the Control Logic section is to decode the incoming command (Instruction Decoder) and to take the appropriate actions. It supervises the initialization phase of Timing Controller, Oscillator, DC/DC Converter and Temperature Compensation blocks. It also contains a (volatile) register where OTP parameters are latched at power on.

Advanced tasks offered by this section may include 2D graphic acceleration features to reduce the required processing power from the MCU and leaving it free

for other features. For instance, graphic functions are implemented that facilitate the user with simple instructions to draw lines, rectangles, copy or move objects and even define pop-up windows, while speeding up the application system.

4.5 Image Processing

The incoming pixel dataflow is stored into the RAM and subsequently goes through a data elaboration pipeline that performs color processing.

4.5.1 Display Data RAM

The column data of each frame, before being displayed, are stored into a static random access memory, Video SRAM, that is included into the driver. In practice, each pixel of the display is mapped into the RAM. To display color images, each RAM location must be a *C*-word, where *C* is the number of color bits. For instance, a 262k-color display requires 18 bit to code the column data. For a 132×162 display the required RAM dimension is $N \cdot M \cdot C$ bit=$132 \cdot 162 \cdot 18$=384,912 bit.

The RAM is essential for power saving when displaying the same image for a long time (like in PMLCD applications). In this case the image data are stored into the RAM and are no longer transmitted by the host processor.

Usually, when data are written in the RAM several displaying modes are possible such as for instance: *normal horizontal*, *normal vertical*, *horizontally mirrored* and *vertically mirrored*.

It is worth noting that CMOS processes with progressively reduced channel lengths are needed to implement single-chip drivers able to manage 4k, 65k, 262k color data, due to the RAM requirements in terms of area occupation. However, finer processes tolerate reduced voltages and hence a trade-off between required performance and suitable technology may arise, which is solved by the development of specific processes, as discussed in Section 4.7.

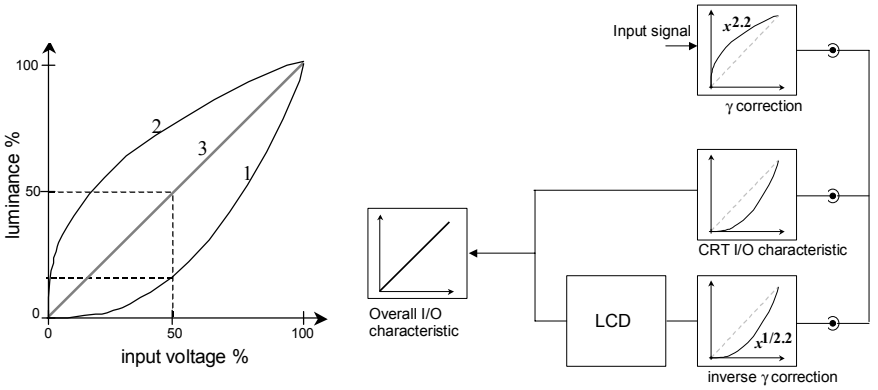
4.5.2 Color Processing

Color processing includes gamma expansion, correction of nonlinear electro-optical transfer function and, in principle, color space conversion with black/white points adjustment, all performed in the digital domain.

(a) Gamma correction ensures accurate reproduction of color and image detail over a wide range of luminance. To fully understand the subject, we must refer first to the CRT performance, because gamma correction was originally applied to this class of displays. As illustrated in Fig. 4.16a, curve 1, a CRT does not respond to an input voltage linearly, its luminance is approximately proportional to the input voltage raised to the 2.5 power. This number is known as **gamma** (γ) [P1993]. In general any kind of display has a nonlinear T/V characteristic, so that the normalized luminance, *L*, is proportional to some power of the normalized signal amplitude, *x*, according to $L = x^{\gamma}$ where $L, x \in [0 \ldots 1]$ and $\gamma > 1$.

As a result, in a CRT, linear RGB data must be predistorted (gamma corrected) before being displayed to compensate for the nonlinearity of electro-optic transfer.

This correction effectively accomplishes a compression of the video signal through the inverse electro-optic transferfunction of the display, $x^{1/\gamma}$ (see curve 2 in Fig. 4.16a), so that the whole system (gamma-correction plus CRT display) response approaches the ideal straight line (see curve 3 in Fig. 4.16a). The input voltage is hence raised to the 0.4 power (i.e., 1/2.5). In reality, since also the human visual system (eyes to brain transferfunction) is nonlinear, such exponent is changed into 0.45 and video standards assume accordingly a display gamma of about 2.2 for CRT displays.[6]



(a) (b)

Fig. 4.16 (**a**) CRT luminance versus input voltage: (1) actual curve, x^{γ}, (2) gamma correction curve, $x^{1/\gamma}$ and (3) ideal (linear) response, x. (**b**) TV broadcasting system. LCD is assumed linear but requires its own γ correction

In the early period of CRT TVs, it was decided to apply the correction directly at the video cameras; a less expensive solution than having to provide gamma correction to every TV set, see Fig. 4.16b.

This means that nowadays, if we want to display TV-coded (and also MPEG-coded) video on an LCD, we must take the gamma correction into account and introduce a transfer function that raises the associated data voltages to the power of 2.2 (x^{γ}, gamma expansion, or inverse gamma correction). This scenario is further complicated by the fact that there are several standards defining different gamma compression functions with slightly different γ values, such as ITU Rec. 709 (TV), CIE L*, sRGB (WEB), etc. [IEC1998, IEC1999].

Of course, gamma expansion must be matched with the standard used to encode incoming images or video.[7] As a consequence, an LCD driver IC cannot operate with a fixed gamma value.

Besides, an adjustable γ is needed for other two main reasons detailed below.

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[6]Besides, human eyes are more sensitive to luminance changes in dark areas than to similar-sized changes in bright areas. Therefore, the compression should be reduced in low gray levels because that becomes much significant in dark areas. The solution is to use $\gamma = 1.8$ for $0 \le x \le 0.35$ and $\gamma = 2.2$ for $0.35 < x \le 1$.

[7]In addition, most commercial digital cameras dynamically vary the amount of gamma.

First, a specific gamma correction for the electro-optic nonlinearity of the LCD itself must be devised. This nonlinear behavior depends on variations in manufacturing and process parameters from a production line (LC mixture, polarizers, backlight, etc.). Thus, different panels have different T/V curves and require different gamma values (otherwise, different panels next to each other will have slightly different color response). It should be observed at this purpose that the T/V curves are not exact analytical functions but they are expressed as approximated interpolation of experimental data.

Second, factors such as ambient illumination can play an important role in our perception of gray scale and color. Without the ability to adjust gamma, the reproduced image will suffer from lack of detail in shadow areas (black crush) or oversaturated whites.

Considering a normally white LCD and its T/V nonlinearity, we represent in Fig. 4.17 the gamma correction curve required to display equally distributed gray levels, *GL*, by applying non-equally distributed voltage levels V_{GL}. A curve for positive and negative values is needed by polarity inversion driving techniques.

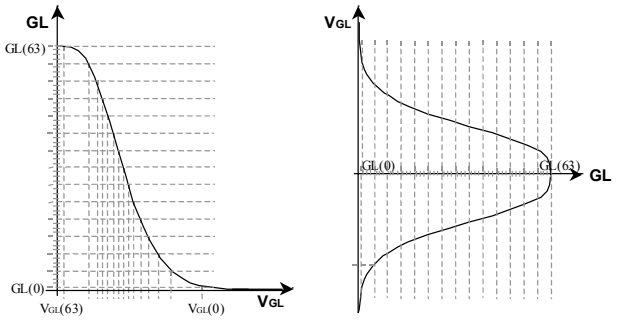


Fig. 4.17 LCD Gamma Correction curve: (**a**) nonlinear characteristic, (**b**) for positive and negative voltages

(b) Color space conversion (see also the Appendix D) can be used to translate RGB components from color space used to code still picture or video data, such as PAL, Rec. 709 (TV) or sRGB (WEB), etc., to color space that have as tristimulus base those that are *physically* reproduced by the particular display device. Indeed, if the RGB primaries of the display device have different chromaticities with respect to either interchange or transmission primaries, then an accurate color reproduction cannot be achieved. A 3×3 matrix is used to transform the color space from the interchange primaries to the display device primaries. This 3×3 matrix takes place in linear-light (tristimulus) space, after gamma expansion. The 3×3 matrix is unambiguously defined by primaries and white reference chromaticities of both interchange and display device color spaces. Hence, by suitably changing the matrix it is possible to change the white reference maintaining the same color primaries. Black and white points are the optical outputs of the display device when RGB

inputs are respectively [0, 0, 0] and [255, 255, 255] (considering 24-bit RGB, that uses 8 bit per color component). But the color characteristics of these points depend on characteristics of display components such as backlight, liquid crystal cell, color filters, etc. It is then possible to adjust these two points by adjusting electrical minimum and maximum values for each RGB component.

Actually, in passive displays, in which color quality is not the main concern, this task is heavily simplified and $\mathbf{T_{1\to 2}}$ is a straightforward diagonal matrix.

From the above considerations it emerges that the **pixel elaboration flow** has to be adaptable to different ambient conditions, to different encoding standards and to a wide range of display devices, and this has to be done by using a limited storage medium such as the OTP Memory previously described.

Figure 4.18 shows the three elaboration steps performed by a typical Driver IC. The incoming pixel data flow (R′, G′, B′) is described in perceptual domain. The first operation is gamma expansion; typical values of γ are 1.0, 1.8, 2.2 and 2.5. It is possible to store in the OTP memory a custom γ value. After gamma expansion, the pixel data flow (R_1, G_1, B_1) is described in physical (intensity) domain. Now it is possible to transform color tristimulus from source space (R_1, G_1, B_1) to destination space (R_2, G_2, B_2) by using the 3×3 conversion matrix $\mathbf{T_{1\to 2}}$. In this step it is possible to adjust black point voltages by adding constants (c_R, c_G, c_B) to color components. White point voltages can by adjusted by proper choosing $\mathbf{T_{1\to 2}}$ matrix. The last step is to correct the nonlinearity of the electro-optical transfer function (EOTF) of LCD. To do this a Look Up Table (**Gamma LUT**) is used. In this LUT the inverse LCD T-V function is stored. It is possible to use different inverse T-V functions for each color component ($EOTF_R^{-1}$, $EOTF_G^{-1}$, $EOTF_B^{-1}$). The outputs are the voltages of elaborated pixel data flow (V_R, V_G, V_B), that is the RMS value driving the columns of the LCD allowing the desired pixel luminance (L_R, L_G, L_B).

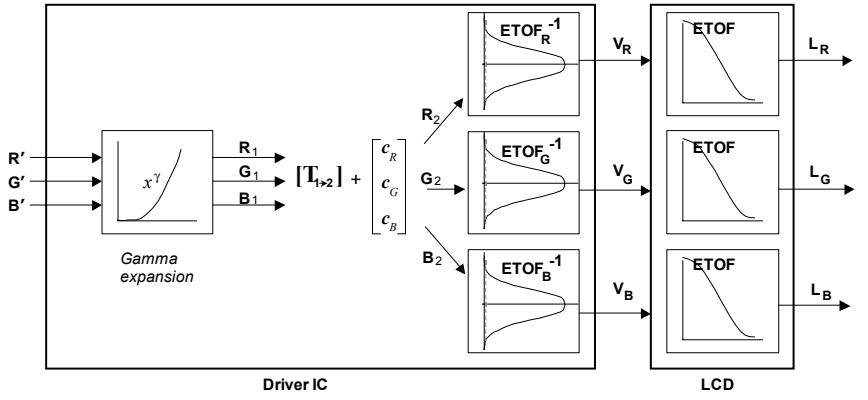


Fig. 4.18 Pixel elaboration steps

4.5.3 MLA and Gray Generation

Purpose of this block is to implement a **Column Logic** in order to latch Video RAM output, generate PWM/FRC control signals, calculate MLA waveforms and provide them to analog column drivers. Since these functions are tightly connected to the column (and row) drivers, their implementation issues will be discussed in Section 4.6.

4.5.4 Timing Controller (TCON)

This block generates the clock signals for (1) RAM access, (2) MLA and PWM/FRC elaboration and (3) n-line inversion. It synchronizes the column and row operations by selecting the proper rows with associated RAM data. These synchronization signals are all derived by division from the on-chip oscillator signal (described in Section 4.4.2). In the case of MLA, the orthogonal functions could be in principle memorized into a dedicated ROM. However, due to the small number of matrix elements usually needed (up to MLA-4 approach, at least), they are managed within the Timing Controller.

4.6 Output Drivers

The output drivers have the role to interface the driver IC with the LCD rows and the columns. These lines offer relatively large capacitive loads and should hence be driven with a sufficient current drive capability. This task is obtained by the analog buffers, directly connected at the output of the voltage generation section (DC/DC converters). Therefore, the architecture of the output drivers simplifies considerably and, ultimately, reduces to a multiplexer.

4.6.1 Row Drivers

It was described in Section 3.2 that both *single line* and *multiple line addressing* approaches are possible in PMLCDs.

In the former case, considering first the A&P approach, the row drivers are simple multiplexers designed to select one out of three voltages. As already illustrated in Fig. 3.9, the row voltage of a selected row can be $+V_R$ (or $-V_R$, for frames with reversed polarity), while unselected rows are addressed by a mid voltage (0 V).

The row driver for the IA&P technique must select one out of four voltages, i.e., V_R+V_C for the selected row and V_C for unselected rows in positive-polarity frames (and respectively 0 and V_R in negative-polarity frames). Note that the above voltages are those depicted in Fig. 3.10, but shifted of $+V_C$ to exploit positive values only.

A possible row driver architecture for IA&P is depicted in Fig. 4.19. The N-stage shift register (see Section 6.4 for shift register architectures) selects one row at a time through the bank of (row select) switches S_{RS}. For illustration, row 1 is the selected one. The voltages with the proper frame polarity are obtained through switches S_{FP}.

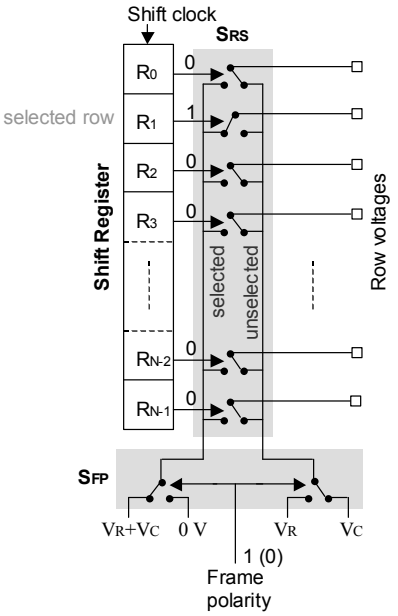


Fig. 4.19 Row driver block diagram for Improved Alt and Pleshko approach

Consider now the case of MLA-*p* addressing. We have seen in Section 3.2.2 that in this approach *p* lines at a time are addressed and the row signals are derived from orthogonal matrices, whose elements have just two values. Hardware complexity of the row (and column) driver depends on the number of voltage levels in the addressing waveforms, therefore those matrices minimizing the number of voltage levels in the scanning waveforms are preferred.

Also in this case, the row drivers are multiplexers that are designed to select one out of the three voltages i.e., $+V_R$ or $-V_R$, corresponding to elements +1 or –1 of matrix column (select pattern), and a mid voltage (0) corresponding to the unselected rows. The block diagram is very simple and can be deduced from that of a column driver for MLA described in the next section.

4.6.2 Column Drivers

Again, let us first consider single line addressing. In the A&P approach, the **column drivers** are multiplexers designed to select one of the two voltages i.e., $+V_C$ or $-V_C$, for ON and OFF pixels, respectively (the voltages are the same but with reversed meaning, for frames with reversed polarity). The column drivers used in the IA&P approach must instead select one out of four voltages, i.e., 0 or $2V_C$ for ON and OFF pixels, in positive frames, and V_R or V_R–$2V_C$ for ON and OFF pixels, in negative frames (see Fig. 3.10 after shifting all waveforms by $+V_C$).

Consider now the case of MLA-*p*. The column signal is given by the *dot product* between the row select pattern and the data pattern in the selected subgroup of rows (as explained in Section 3.2). Assume that *p* is the number of grouped lines and that *p*+1 is the number of voltage levels in the column waveforms. The number of data

bits x must be consequently not lower than $\log_2(p+1)$. If M are the columns, there are hence M stages of shift register and latch and every stage has x bit each. After serially shifting the data corresponding to all column lines, the content of the shift registers are transferred in parallel to the latches and can be applied simultaneously to the column electrodes even though the dot products are computed sequentially. The schematic diagram of a column driver following this strategy is illustrated in Fig. 4.20 [RS2005].

This solution has the advantage of small area occupation, but requires high power consumption because the shift registers must work at the highest frequency (which hence coincides with f_{OSC} of the local oscillator) given by $f_F \cdot N \cdot M \cdot p = f_{OSC}$. For instance, if f_F= 60 Hz, N=160, M=128 and p=4, we get that the required local oscillator frequency is approximately f_{OSC} = 5 MHz.

An alternative low-power column driver scheme is depicted in Fig. 4.21.

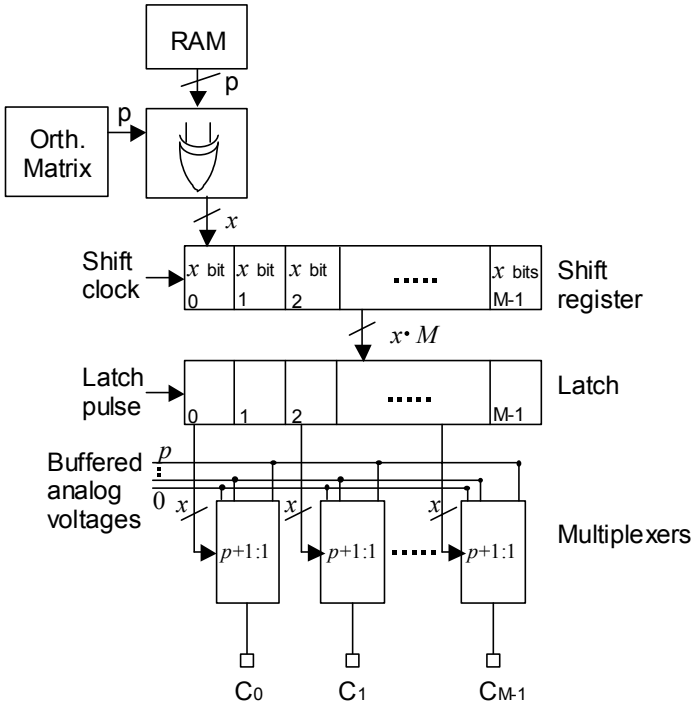


Fig. 4.20 Block diagram of a column driver used for MLA. (The operation performed by the XOR block is detailed in Fig. 4.21)

The column data patterns for each MLA row sub-group are stored into the Frame Buffer Memory and the XOR gates followed by the summer function perform the required product with the proper column of the orthogonal matrix. For instance, in Fig. 4.21 a MLA-4 approach is considered. The associated matrix is the 4×4 unity matrix shown at the left and the product with the first matrix column is performed. It is important to observe that to allow binary-logic computation, each −1 matrix entry is replaced by 0. In the figure it is also assumed that the data pattern for the

considered row subgroup is 1011 (meaning that in the considered row subgroup the first, third and fourth pixels are ON while the second pixel is OFF). The result of the XOR and subsequent summing computation is associated (through multiplexers) with the analog voltage that will be applied to the column. More precisely, the values 000, 001, 010, 011 and 100 are respectively associated with $-V_C$, $-V_C/2$, 0, $+V_C/2$ and $+V_C$. In the case exemplified the computation gives 010 that means 0 V. Compared to the previous solution, this one requires a lower clock frequency expressed by $f_F \cdot N \cdot p$, i.e., M times lower. Indeed, with the same data of the previous example this one works with a frequency equal to 38.4 kHz. The lower consumption allows high-resolution PWM (up to 64 levels) to be implemented. Actually, the above considered column driver schemes are all for black and white displays. Gray levels through the PWM approach can be obtained with a modification of the scheme in Fig. 4.21, as illustrated in Fig. 4.22, where a 64-PWM technique is considered. Now, each cell of the frame buffer memory contains the number of bits encoding the gray levels (6 in our example). Besides, PWM generator blocks (implemented through comparators) are inserted at the output of the buffer. They compare the output of a 6-bit counter with the incoming 6-bit data word. The comparator output goes high only if the gray-level-encoding word is greater than the counter word.

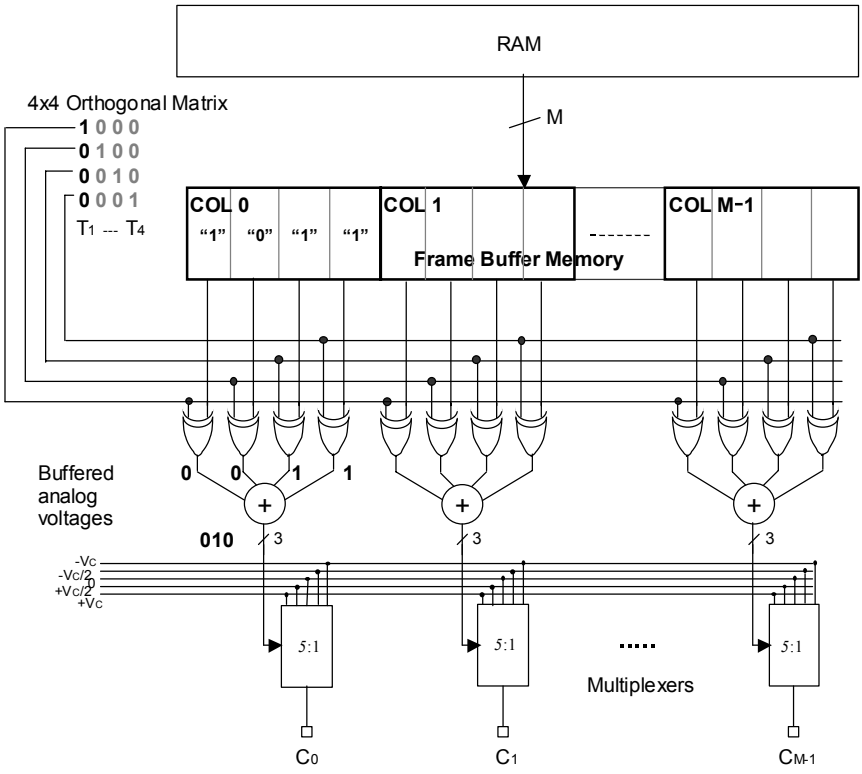


Fig. 4.21 Block diagram of another column-driver scheme for MLA-4

Considering again $f_F = 60$ Hz, N=160, M=128, p=4, n_{GL}=64(=2^6), we get approximately that the required maximum frequency of the local oscillator is $f_{OSC} = f_F \cdot N \cdot p \cdot n_{GL}$=2.46 MHz which is practical for mobile applications owing to the associated relatively low power dissipation.

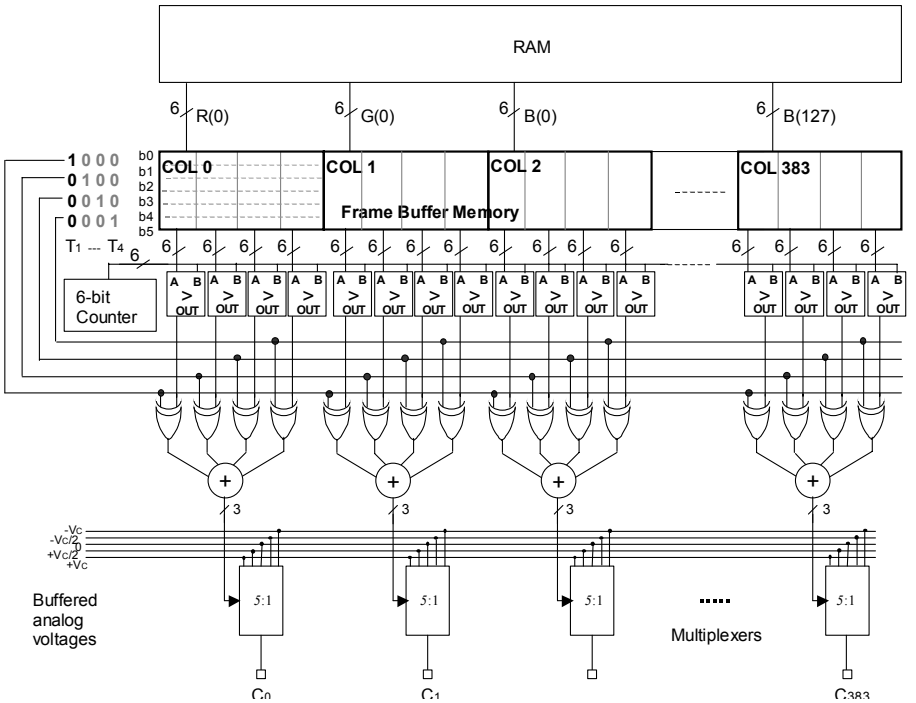


Fig. 4.22 Block diagram of column driver for color LCD adopting MLA-4 and PWM

4.7 Silicon Processes for Display Drivers

The silicon process required to implement single-chip driver ICs is quite challenging. Other than providing mixed-signal functionalities and allowing the integration of SRAM banks, it must posses also high-voltage capability (from 20 to 40 V).[8] In addiction, the demand for increased resolution and number of colors mandates for high gate density. Therefore, special technologies compatible with advanced CMOS families, but based on High Voltage Gate (HVG) CMOS devices have been developed.

Considering the specific case of mobile devices for consumer electronics, the market is very competitive and products have very short life (from 1 to 3 years).

[8]A process with these behaviors is of course developed by silicon foundries not only to cover passive-matrix and active-matrix LCDs (see Chapters 5 and 6) but also emissive (OLED) displays.

Keeping low the cost is thereby mandatory. This issue is addressed through the use of mature CMOS technologies (0.35 μm–0.13 μm), reduction of available process steps (e.g., limited number of metal layers) and efforts on IO area reduction including either *Circuit Under PAD* (CUP)[9] or *Bond over Active* (BOA)[10] approaches.

This section is largely based on [ABC2005], a paper describing the BCD-HVG8 (Bipolar, CMOS and DMOS) process family developed by STMicroelectronics. The HVG8 process exploits a 0.18-μm standard CMOS technology with several enhancements such as:

(1) Shallow Trench Isolation (STI) for CMOS isolation;

(2) Borderless Contacts;

(3) Dual Gate Oxide for 1.8-V/5-V CMOS devices (whose main electrical characteristics are summarized in Table 4.1). The low leakage current of the 1.8-V devices allows also the realization of compact SRAM banks based on the 6T cell (bit size 4.45 μm^2, in line with all available advanced 0.18-μm CMOS processes). Figure 4.22a shows the schematic of a SRAM cell and the micrograph of a SRAM bank is depicted in Fig. 4.23a. The vertical geometries are diffusions (transistor source/drain terminals) and the horizontal ones are polysilicon layers (transistor gate terminal). Metal contacts and paths are not shown in the photograph 4.22b. Symbol X means to row decoder;

(4) A number of 5 Al-Cu metal levels are allowed with the last one realized by either Al-Cu or pure Cu thick layer (though only three metal levels are utilized for LCD driver implementations, to keep fabrication costs low). The higher thickness of the upper metal allows long low-voltage-drop lines realization. This feature is very useful in display drivers because of their typical high aspect ratio.

The high voltage options offered by the HVG8 process are several and include:

(1) 20-V/32-V/40-V HVG MOS transistors through thick gate oxide;

(2) High voltage MOS transistors with low voltage (1.8/5 V) thin gate oxides (Drift MOS) for Antifuse One Time Programmable (OTP) memory blocks (OTP bit density in the range of 1 $kbit/mm^2$ has been achieved);

(3) LDMOS transistors for OLED drivers where large currents are needed.

[9]To save chip space, active circuitry is placed underneath the bonding pads**.** The CUP technique, which violates the rule of conventional layout for a chip, uses a variety of support structures that contain metals, dielectrics and their combinations designed to protect device components and to minimize damage caused by probe testing and subsequent assembly.

[10]Typical wirebond pad designs consist of a top-level metal that does not include any circuitry beneath the bonding region. The BOA technique was developed to utilize this region beneath wirebond pads in order to minimize die area.

Table 4.1 Main electrical parameters of HVG8 1.8-V and 5-V CMOS

	Parameter	**1.8 V (L_{min}=0.18 μm)**	**5 V (L_{min}=0.6 μm)**
nMOS	V_T (mV)	680	850
	I_{on} (μA/μm)	510	500
	I_{off} (pA/μm)	2	<1
pMOS	V_T (mV)	–770	–775
	I_{on} (μA/μm)	–220	–290
	I_{off} (pA/μm)	–3	–1

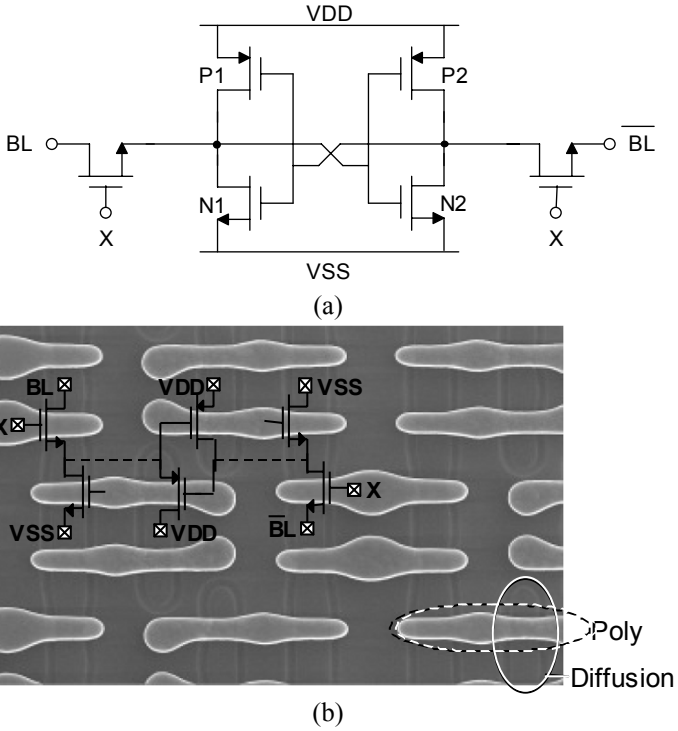


Fig. 4.22 (**a**) SRAM cell schematic, (**b**) micrograph of a SRAM bank in HVG8 technology

4.8 Packaging and Assembling Techniques

In this section we will describe the two main technologies that allow the electrical connection of the display to the driving circuits and of the driving circuits to the PCB. The same techniques described are not restricted to PMLCDs but are used also for Active Matrix LCDs.

Due to the great number of connections and the near impossibility of soldering ITO, both **Chip on Flex** (COF) and **Chip on Glass** (COG) approaches are widely used for driver IC attachment.

Anisotropically Conductive Adhesive Films (ACFs) are usually exploited to as an interconnection material for COG and COF [YP1998, S2004]. ACFs are composite materials consisting of polymer matrix, i.e., the adhesive and conductive particles, as illustrated in Fig. 4.23.

The fraction of conductive particles varies between 0.5 and 5% of the volume. The particle types vary from solid metal particles to polymer spheres coated with metal, the latter being most popular for high-density display applications [WT1999].

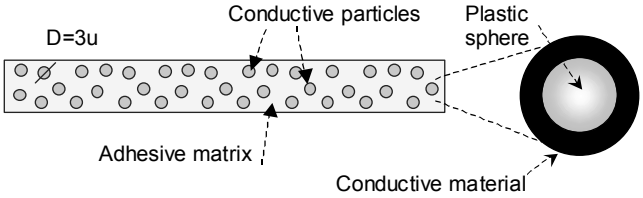


Fig. 4.23 Anisotropically Conductive Adhesive Films (ACFs) are used to electrically connect the Driver ICs to either the track on glass or tape automated bonding

4.8.1 Chip on Flex

In the original approach (first used by SHARP in 1985), the driver IC is packaged in a flexible **Tape Carrier Package** (TCP) and attached to the glass with **Tape Automated Bonding** (TAB) as illustrated in Fig. 4.24.

To allow flexibility the TCP has slits at regular distances (see Fig. 4.25a), and the tape can be bent only in a position corresponding to a slit. To improve performance and reduce costs, a new approach was developed called Chip on Film (1998).

The appearance of TCP or COF is similar, as both techniques rely in mounting the IC on a tape (see Fig. 4.25a, b). However, COF offers some substantial advantages: (1) it is free of slits and can be flexed in any position and with a greater freedom (oblique bend is possible), (2) it allows a finer bonding pitch (< 35 μm), (3) it allows high density packaging. Figure 4.26a shows the micrograph of a gold bump, while Fig. 4.26b shows the connections between the inner leads and bumps (in this case ACF is not used, but instead a gold-tin eutectic between the bump and the tin of the inner leads is formed [ML1986]).

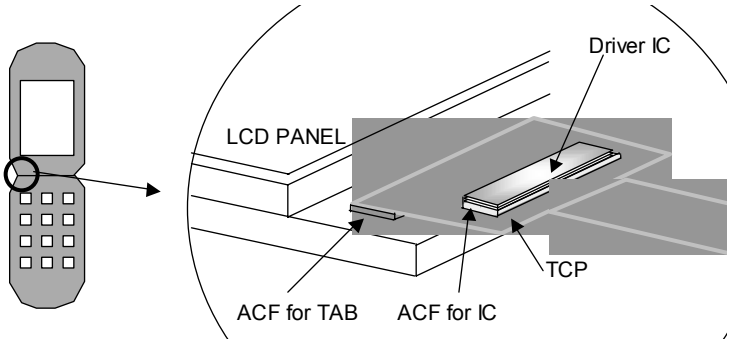
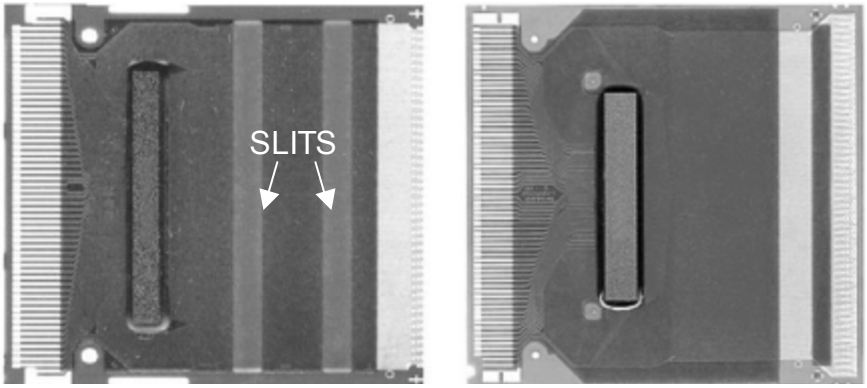
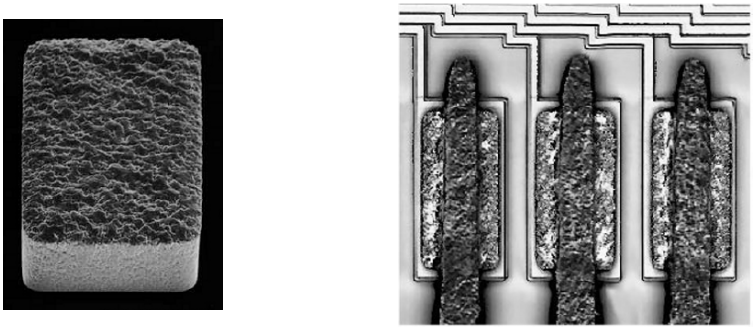


Fig. 4.24 TCP approach



(a) (b)

Fig. 4.25 Examples of (**a**) COF and (**b**) TCP [TNF2003]



(a) (b)

Fig. 4.26 Micrographs of (**a**) a gold bump and (**b**) connection between bumps and inner leads in COF via gold-tin eutectic bonding [TNF2003]

4.8.2 Chip on Glass

COG was first introduced in 1983 by Citizen and since then the method diffused significantly [KL1999]. In this approach the IC is mounted directly on the glass substrate, avoiding the use of the flex and reducing costs. Figure 4.27 depicts an LCD panel with Driver IC connected via COG approach. The drive lines of an LCD are typically brought to a single glass bonding ledge, and routed along the inactive sides of the display to their intended destinations.

As illustrated in Fig. 4.28, conventional IC wire bonding is here replaced by the formation of gold bumps. After prebonding the ACF to the glass with mild heat and low pressure, the driver IC is aligned in such a way that its bump pattern matches the pad pattern on the glass. Then, the IC is pressed against the ACF and glass applying heat through the bonding tool. Conductive particles should be trapped between each bump-pad pair in order to ensure conductivity. The adhesive allows anisotropic conduction, only in the vertical direction. Extra polymer should be pressed out from under the IC.

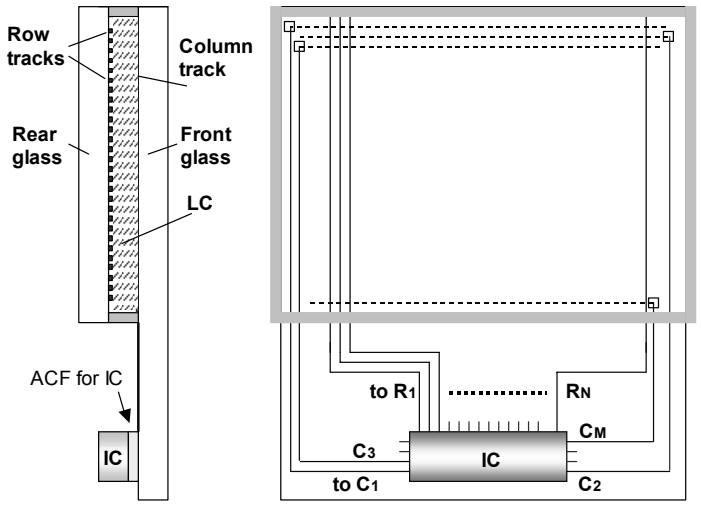


Fig. 4.27 LC panel with COG driver IC

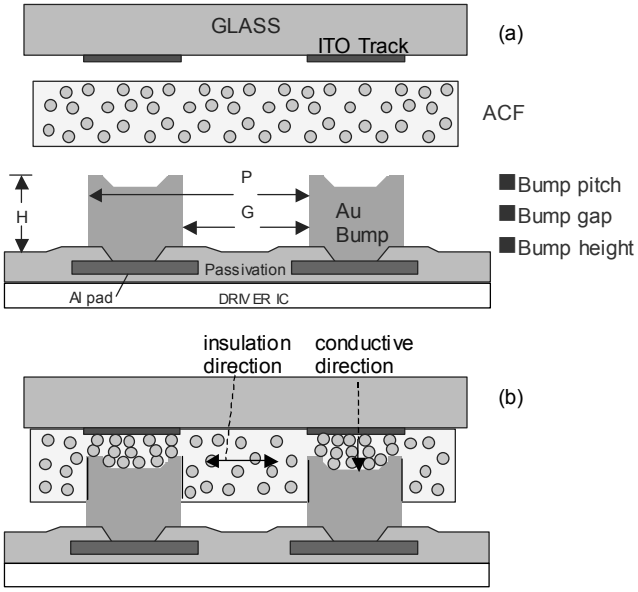


Fig. 4.28 COG technique. Cross section of a driver IC, Bumps, ACF, and Glass with typical dimensions: (**a**) before and (**b**) after electrical connection is formed

4.9 Concluding Remarks

We conclude this chapter by presenting an example of CSTN LCD ('C' stands for color) driver IC developed by STMicroelectronics, called the STE2028. It is designed for a 162×132-RGB LCD with 262k colors. It adopts the HVG technology and provides fully integrated booster (with the exception of the bulk capacitors), a 385-kbit SRAM and a 0.8-kbit OTP memory. It exploits MLA-4, n-line inversion and both PWM and FRC algorithms. It allows also partial display mode, enabling screen saver controls for power consumption reduction. The chip size is around 17 mm^2. Figure 4.29 shows the complete layout. Figure 4.30 illustrates the percentage of analog and digital component sections of the driver.

The complete block diagram is illustrated in Fig. 4.31. The reader will recognize many of the blocks although indicated with somewhat slightly different nomenclature (eg., MLS instead of MLA).

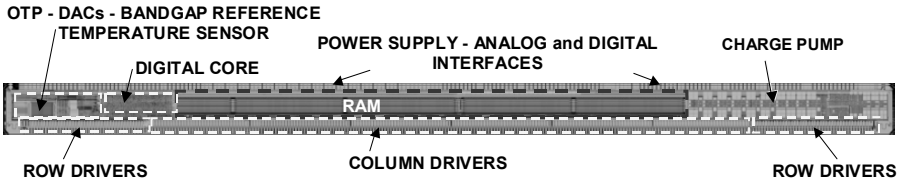


Fig. 4.29 Layout of the STE2028 LCD driver

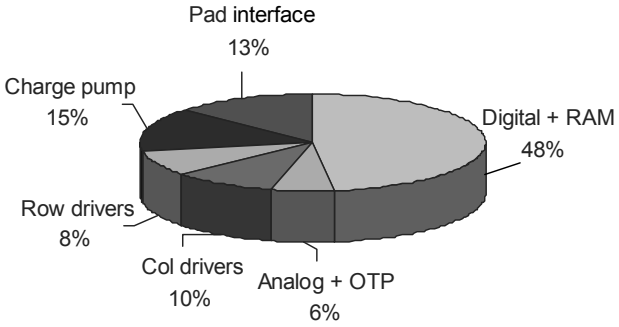


Fig. 4.30 Block partitioning of the STE2028 LCD driver

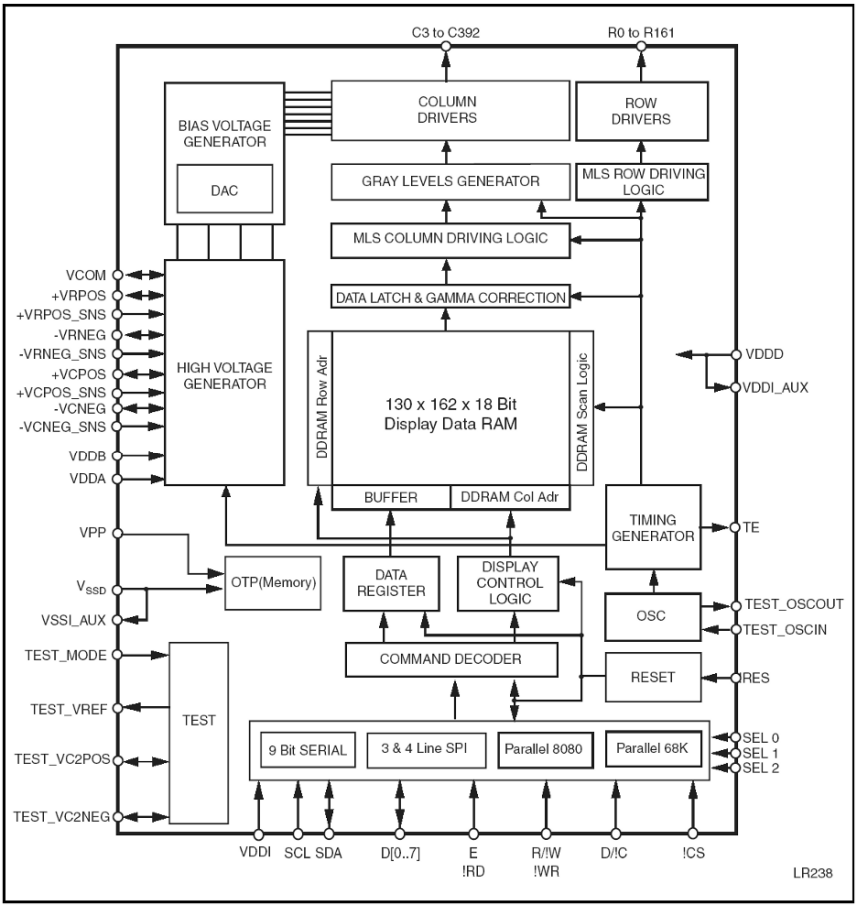


Fig. 4.31 Block diagram of the STE2028 LCD driver IC (Courtesy of STMicroelectronics)

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