Chapter 1
Getting Started to Explore "Integrated Nanoelectronics"

Abstract A prelude to the subject is provided by delving into the present scenario and research trends in nanoelectronics and relating them to the organization of contents of the book. The chapter will provide a snapshot into the diversity of topical coverage and their mutual interrelationship, serving as a launching pad to begin exploration of this vast field.

1.1 What "Integrated Nanoelectronics" Is About?

The impact of nanotechnology on electronics needs hardly to be emphasized. Nanotechnology makes semiconductor chips smaller and light in weight. It makes them cheaper. It reduces power consumption. It makes data communication faster. Integrated nanoelectronics or nanotechnology of integrated circuits is revolutionizing our lifestyles and improving the overall quality of human life everyday [1–3].

For long, the MOSFET device used in the CMOS configuration has been the workhorse of integrated circuit industry. The CMOS structure has been constantly miniaturized and is fast reaching the physical limits. The objective of this book is to survey the MOSFET geometries and architectures, along with necessary process modifications that have emerged with constant downscaling of the primitive designs. A family of nanotechnologies is also supporting CMOS and can be incorporated with CMOS to enhance capabilities. These include the optical, mechanical, and biosensors, together with magnetic memories. These CMOS-supportive nanotechnologies constitute another major area of interest that will be discussed.

As the physical barriers are insurmountable for CMOS, this lone star in the sky of nanoelectronics may no longer be able to bear the burden of nanoelectronics. Many new stars are appearing on the horizon. Although these new stars are not equally bright but they may gain in intensity as time passes by. These upcoming technologies fall under the "Beyond CMOS" category. These potential stars, which are likely to supersede CMOS to fulfill the needs of nanoelectronics, form another interesting area.

V.K. Khanna, *Integrated Nanoelectronics*,
NanoScience and Technology, DOI 10.1007/978-81-322-3625-2_1

The above ideas are crammed into the following poem:

Integrated Electronics Marches On Gloriously….

From 1947-the invention of bipolar transistor,
and 1958-the first integrated circuit,
Electronic integrated circuits or Integrated electronics,
Built on monolithic silicon blocks,
With interconnected active and passive components
Have overcome many roadblocks.
Leapfrogging many hurdles and rocks,
Advancing from macro to microelectronics,
Down to nanoelectronics,
And reaching integrated nanoelectronics.
By applying nanotechnolgy to electronics,
Based on CMOS technologies,
And supporting nanotechnologies,
Photonics, NEMS and biotechnologies.
Also beyond CMOS,
There are carbon nanotubes and nanowires.
2-D materials and quantum dot cellular automata,
Electronic spin and single electronics,
RFSQ and molecular electronics.
Devices and circuits are fast shrinking,
Progressing from miniaturization to super-miniaturization,
New structures and architectures are evolving.
Self-assembly may hold the key to nanofabrication.
Future options are achievable and realistic,
Making us very hopeful and optimistic.
Let us strive with all our might,
The future is very bright!

1.2 Subdivision of the Book

The book is divided into five parts. Part I introduces the elementary topics. Part II is devoted to CMOS nanoelectronics. Part III addresses nanotechnological allies of CMOS. Part IV deals with "beyond CMOS" nanoelectronics. Part V treats nanofabrication and nanocharacterization aspects.

1.3 Organization of the Book

1.3.1 Part I: Preliminaries

Part I contains two chapters. Chapter 2 introduces the subject matter of this book. Nanoelectronics and associated nanotechnologies are defined and their mutual interrelationship is described. Chapter 3 explains the basic terminology of nanomaterials. The unique properties of these materials responsible for their special behavior are highlighted.

1.3.2 Part II: CMOS Nanoelectronics

Part II spanning over Chaps. 4–7 is concerned with the classical MOSFET and its downscaled versions. In Chap. 4, the readers are familiarized with the MOSFET and CMOS structures, the related self-aligned fabrication processes and CMOS logic gates. Then the influence of constant field and constant voltage scaling on MOSFET performance is outlined. Knowledge of basic MOSFET electronics is assumed.

Chapter 5 describes the unfavorable phenomena which come into play when the channel length of a MOSFET becomes comparable in dimension with the space charge region widths of source and drain junctions. These MOSFETs are referred to as short-channel devices. Many unwanted effects such as drain-induced barrier lowering, velocity saturation, carrier mobility degradation, etc., begin to seriously impoverish the device characteristics in these low-dimensional MOSFETs. Nonetheless, these MOSFETs have been able to meet the downscaling challenges by making suitable structural and doping profile changes and using novel materials such as high-κ dielectrics.

The succeeding Chap. 6 takes a look at a different class of MOSFETs which are fabricated on silicon-on-insulator (SOI) wafers containing a thick bottom silicon layer called the handle wafer over which there is a buried oxide layer with a silicon layer at the top in which the device is built. These SOI-MOSFETs have been realized in partially depleted and fully depleted forms. Pros and cons of the two forms are brought out.

In Chap. 7, popular MOSFET varieties, namely the FINFET and tri-gate FET are dealt with. These MOSFET varieties mark a changeover from the ancient two-dimensional MOSFET to the present three-dimensional edifices. They were felt essential because the gate terminal was losing its effectiveness in the planar MOSFET at scaling limits. So, the main intent of these three-dimensional MOSFETs is to make the gate more effective in controlling the channel.

1.3.3 Part III: CMOS-Supportive Nanotechnologies

Part III comprises Chaps. 8–11. Chapter 8 is concerned with nanophotonics. Interaction of light with metallic nanoparticles gives rise to surface plasmon resonance phenomena which form the basis of several useful sensors. Nanophotonics also offers the opportunities of building logic circuits. Laser capabilities are significantly improved by inserting quantum dots in the active region. Photonic nanocrystals offer interesting applications as optical filters. The next Chap. 9 presents a brief treatment of nanoelectromechanical systems, which are a step further to microelectromechanical systems in miniaturization. The operation of several nanosensors for pressure, displacement, etc., is discussed along with NEMS actuators like nanogripper, nanotweezer, and so forth. The focal theme of Chap. 10 is nanobiosensors which represent the confluence of nanoelectronics with biotechnology. Research endeavors in this interdisciplinary field have led to many sensors for biological analytes such as glucose, DNA hybridization, and toxins like organophosphorous pesticides. Chapter 11 on spintronics provides a succinct overview of magnetic memories based on the giant magnetoresistance effect as well as those utilizing magnetic tunnel junctions. These memories have made ingress into the present-day computers, vastly augmenting the storage capacity.

1.3.4 Part IV: Beyond CMOS Nanoelectronics

Part IV makes a departure from the mainstream CMOS and treats the alternative options that have been proposed over the years as successors of CMOS. None of these options have gained popularity up to a level of even a small fraction of that enjoyed by CMOS today. In Chap. 12, attention is directed towards resonant tunneling diodes, which are superfast devices based on quantum-mechanical tunneling through thin insulating films for terahertz frequencies utilizing the negative differential resistance. Another tunneling-based device is also treated, viz., the tunnel field-effect transistor. Tunnel FETs are steep subthreshold slope switches permitting supply voltage scaling for extremely low power computing. Their working principle is band-to-band tunneling mechanism which can be controlled through gate voltage. Chapter 13 is a preparatory chapter for understanding the single electron transistor to be described in Chap. 14. Concept of tunnel junction is developed and its equivalent circuit model is discussed. Coulomb blockade or Kondo effect is a charge quantization effect related to the electrostatic energy that must be added or subtracted from a conducting island for electron transference to it or removal of electron from it. A quantum dot circuit operation is analyzed as a prelude to single electron transistor action. Difference in operational behavior between circuits made with big and small quantum dots is pointed out in terms of energy band diagrams. Chapter 14 is devoted to theoretical formulation of single electron transistor. The mathematical framework is followed by energy band concepts. Two types of logic

circuits possible using SET devices are briefly indicated. Voltage-based NOT, AND, and OR circuits are explained. Chapter 15 describes the use of semiconductor nanowire, particularly, silicon nanowire as a building block element of nanoelectronic circuits. Vapor–liquid–solid (VLS) technique of silicon nanowire growth is presented. Simultaneous growth of a large number of nanowires at exactly defined locations allows fabrication of circuits in a controlled fashion. Another important structural unit of nanoelectronic circuits is the carbon nanotube, which is the topic of Chap. 16. Single and multiwall CNTs are distinguished. Arm chair, zigzag, and chiral CNT classes are demarcated. Special electrical, mechanical, and optical properties of CNTs are discussed. Amongst the various available methods of CNT deposition such as arc discharge, laser ablation, etc., chemical vapor deposition stands out prominently as a technique for nanoelectronics fabrication. A remarkable feature of CNTs is that they allow device fabrication by a doping-free process through appropriate choice of materials for contact electrodes. Pass-transistor logic seems to be more favored for CNT nanoelectronics. Both semiconductor nanowires and carbon nanotubes are one-dimensional nanostructures. From these one-dimensional nanomaterials, we move to two-dimensional materials, notably graphene and transition metal dichalcogenides. Chapter 17 concentrates on graphene. Many methods have been devised to prepare graphene such as by cleaving multilayer graphite using adhesive tape or a diamond wedge, by sonicating graphite, exfoliation of graphene by electrochemical synthesis, by heating silicon carbide at high temperatures, etc. Graphene is an allotropic modification of carbon. It is a planar sheet of carbon atoms, which is one atomic layer thick. The atomic arrangement in graphene is shaped like a hexagonal honeycomb lattice. Graphene is associated with many special attributes, a few of which are it being the thinnest compound, the lightest but strongest material, and the best thermal and electrical conductor. Due to its incredible properties, graphene has been hailed as a supermaterial. It offers manifold opportunities to electronic engineers to manufacture flexible circuits. Its shortcoming is the absence of an energy bandgap which must be opened up by structural modification destroying some of its superb qualities. Undoubtedly, graphene is touted to bring breakthrough results reshaping nanoelectronics but we have to wait and watch. Similar to graphene is the family of two-dimensional dichalcogenide materials such as molybdenum disulphide and tungsten disulphide but unlike graphene they show an energy gap allowing fabrication of transistors with high on/off current ratio and thickness of one or few atomic layers. These materials are derived by exfoliation, and prepared by chemical vapor deposition or molecular beam epitaxy. Chapter 18 is devoted to nanoelectronics using TMD materials. The ensuing two chapters take the reader into the world of transistorless logic paradigms. Chapter 19 deals with quantum dot cellular automata which consist of cells of four quantum dots in which electrons reside in either of the two pairs of diagonally opposite quantum dots, corresponding to the binary states of the system. The spacing between quantum dots is typically 20 nm while intercell separation is 60 nm. Electrons can tunnel between quantum dots. Due to their mutual electrostatic repulsion, the assignment of electron positions on the two diagonals constitutes the fundamental principle of this logic. QDCA is a

field-assisted computing technology. It does not use any wires as in transistor circuits. The two basic logic gates are the majority gate and the NOT gate. The QDCA scheme promises higher chip density together with fast speed but presently faces fabrication difficulties. Chapter 20 discusses an analogous logic using nanomagnets. Information is conveyed and processed with the help of these nanomagnets. Similar to the quantum dot cellular automata is magnetic cellular quantum automata (MCQA). These automata retain information after switching off electrical power. Moreover, they are more radiation-resistant. Chapter 21 is concerned with cryogenic rapid flux quantum logic. In this logic, overdamped Josephson junctions are used as switching elements in place of transistors. Transmission of picosecond duration voltage pulses correlated with the transference of a single quantum of magnetic flux pertains to logic high state whereas their non-transmission represents logic low state. These voltage pulses are transmitted at 100 GHz and above, promising high speed. Chapter 22 deals with molecular electronics which uses either single molecules or small ensembles of molecules to perform digital logic operations. The field is still in infancy. Reproducible fabrication of molecular structures remains a big challenge.

1.3.5 Part V: Nanomanufacturing

Part V contains three chapters which are concerned with fabrication of nanoelectronic devices/circuits and evaluation of the materials and processes. Nanofabrication follows two principal approaches. One way is to start with big blocks and reduce their sizes to get smaller functional elements. This is the top-down approach described in Chap. 23. Recapitulating optical lithography and recounting its limitation according to the wavelength of light, we move on to extreme UV lithography, followed by electron beam lithography using electron waves, and then to electron beam projection lithography, which is a method to avoid the throughput disadvantage of electron beam lithography. Soft lithography, nanoimprint, and block copolymer lithographies are also described.

Another nanofabrication strategy is to start from smaller units and these units grow bigger to yield the required device, just as a seed grows into a big plant. This is the bottom-up approach discussed in Chap. 24. These methods include the sol-gel technique, and various forms of physical and chemical vapor deposition. Atomic layer deposition is a widely used bottom-up method. Other common methods are molecular self-assembly and DNA nanoengineering.

Whatever be the course followed, top-down or bottom-up, the semiconductor manufacturer needs accurate instruments for in-process measurements and monitoring. These tools are described in Chap. 25. First and foremost come the different types of scanning probe microscopies, e.g., scanning tunneling and atomic force microscopies. Besides electronic microscopic techniques such as those employing scanning and transmission modes are finding widespread applications. Then there are many X-ray-based techniques like energy dispersive X-ray analysis X-ray

powder diffraction, X-ray photoelectron spectroscopy, etc. Amongst spectroscopic techniques, FT-IR, UV-visible, and Raman spectroscopies are the main instruments of any characterization laboratory. Facilities for determining the size and distribution of nanoparticles help in controlling the properties of nanodispersions. Laser Doppler vibrometry is an optical method for measuring the displacements and velocities of vibrating objects.

1.4 Discussion and Conclusions

The aims and scope of the book were briefly presented and the subject matter to be covered was summarized chapter-wise to enable the inquisitive reader to forge ahead smoothly.

Review Exercises

1.1 Give three examples illustrating the impact of nanotechnology on the performance of integrated circuits.
1.2 Name a semiconductor device which has been the main "burden bearer" of IC industry.
1.3 Name three nanotechnological allies of CMOS technology which are used to enhance its capabilities.
1.4 Explain what is meant by a short-channel MOSFET? What phenomena plague the performance of such MOSFETs? What basic idea is applied to deal with these phenomena?
1.5 What does the acronym "SOI" stand for? Describe the arrangement of layers in an SOI wafer.
1.6 What is the dimensionality shift in MOSFET geometry from planar to FINFET and multigate devices? Why was it necessary?
1.7 Which nanophotonic phenomenon concerned with metals is widely used in nanosensors? Is it possible to perform logic operations optically?
1.8 NEMS complement nanoelectronics through sensors and actuators. Give some examples.
1.9 Nanobiotechnology complements nanoelectronics via nanobiosensors. Give examples.
1.10 What types of spintronic memories are used in nanoelectronics? Cite two examples.
1.11 Which tunneling-based devices are useful for nanoelectronics?
1.12 What is Coulomb blockade effect? Is it possible to make voltage-based logic circuits using single electron transistor?
1.13 Is it possible to grow silicon nanowires of required diameters at defined positions on a wafer?

1.14 Can carbon nanotube transistors be fabricated without doping?
1.15 Why is graphene said to be a supermaterial? What is its principal drawback?
1.16 In what respect is a two-dimensional dichalcogenide superior to graphene?
1.17 Can we altogether avoid the use of transistors for computation? What computational paradigms do not use transistors?
1.18 What are the switching devices used in rapid single flux quantum logic? How are logic high and logic low states represented in this system?
1.19 What are the rudimentary functional units used in molecular electronics?
1.20 What fabrication approach is followed in normal semiconductor chip manufacturing? Bottom-up or top-down. Can optical lithographic technique be used for patterning layers at nanoscale?
1.21 Can you name two bottom-up fabrication techniques?
1.22 What types of scanning probe microscopes do you know?
1.23 Name two kinds of X-ray-based measurement techniques.
1.24 Name three types of spectroscopic methods.
1.25 What is the instrument used to characterize vibrating objects?

References

1. Chau R, Doyle B, Datta S et al (2007) Integrated nanoelectronics for the future. Nat Mater 6:810–812. doi:10.1038/nmat2014
2. Bogue R (2010) The fabrication and assembly of nanoelectronic devices. Assembly Autom 30(3):206–212
3. Collaert N (ed) (2013) CMOS nanoelectronics: innovative devices, architectures and applications. Pan Stanford Publishing Pte. Ltd., 438 pp