Optimized Approach for Reversible Code Converters Using Quantum Dot Cellular Automata

Neeraj Kumar Misra, Subodh Wairya and V.K. Singh

Abstract Reversible logic has gained importance in the present development of low-power and high-speed digital systems in nanotechnology. In this manuscript, we have introduced and optimized the reversible Binary to Gray and Gray to Binary code converters circuit using two new types of reversible gates. Two new types of 3×3 reversible gates, namely BG-1 gate (Binary to Gray) and GB-1 gate (Gray to Binary), have been proposed to design converter circuits without any garbage outputs. In addition, useful theorems have been developed, associated with the number of gates, garbage outputs, constant input and quantum cost of the reversible converters. The QCA Designer v2.0.3 tool is used for simulation to test the workability of reversible code converters. The simulation results show that the design works correctly and extracted parameters are better than the previously reported designs. Area and lower bound parameter analysis also show that the design is based on the optimized approach.

Keywords Reversible logic · Code converter · BG-1 gate · GB-1 gate · Garbage output · Quantum cost · Quantum dot cellular automata

1 Introduction

Nowadays at the transistor level, the designer uses CMOS but it has physical limitations such as current leakage, short channel effect, power consumption, large layout area and delay [1–4]. It is predicted that these physical limitations of CMOS will result at the end of conventional CMOS. The vision is towards QCA (Quantum dot cellular automata). It principally focuses on high device density, low delay and low power circuits. QCA performs computation using electric or magnetic field

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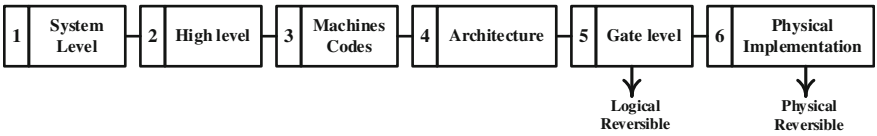

Fig. 1 Approach level of the digital hardware system

polarization [5]. The advancement in digital hardware systems and subsystems has emerged in higher computational density circuits and energy loss has been reduced.

In the early 1960s, Landauer [6] shows that each logic bit of information, KT ln2 joules of energy loss is due to missing bits of information. However, according to Bennett [7], there would be no energy loss and it can be avoided by using the digital hardware designed by reversible gates. Moreover, digital hardware systems are not only logically reversible but also physically reversible. In the design of logically reversible digital hardware system, gate level approach is used. The distinctive feature of the gate is one-to-one mapping between inputs and outputs and output logic can be recovered from input logic [8–11]. Physical reversibility of a digital system can be defined in a way such that if computation is in backward direction without energy loss, then that system design is fulfilling the criteria of physical reversibility. In the flow chart (shown in Fig. 1) of the designing approach, the various levels are shown; fifth level shows the logical reversibility and sixth level shows the physical reversibility.

The paper is organized as follows: Sect. 2 depicts the reversible logic and QCA terminology. Section 3 depicts the design of new code converters using two new types of 3×3 reversible gates. Sections 3.2 and 3.3 describe the Binary to Gray and Gray to Binary code converters with QCA block diagrams and layouts. Section 4 performs a simulation setup result and comparative performance analysis result with the existing approach for the proposed converters in terms of cell complexity, clock cycle and area occupancy. The last section concludes this paper.

2 Background Study

In this section, we present some preliminary knowledge about QCA, reversible logic and their behaviours along with lower bound parameters.

Basics of QCA: The fundamental unit of a QCA device is the QCA cell. These cells contain four quantum dots positioned near the corners of the cell, where another two free electrons can reside [5, 12–15]. Cells have two polarization states (Fig. 1a). These states permit the cells to represent binary value. By setting $P = +1$ polarization (binary 1), while a cell with $P = -1$ polarization (binary 0). The majority vote condition is most used frequently (shown in Fig. 2d). In this, the output is defined by $Maj = (AB + BC + CA)$. If the set one input is at 1, it works as 2-input OR gate. If the set one input is at 0, it works as 2-input AND gate.

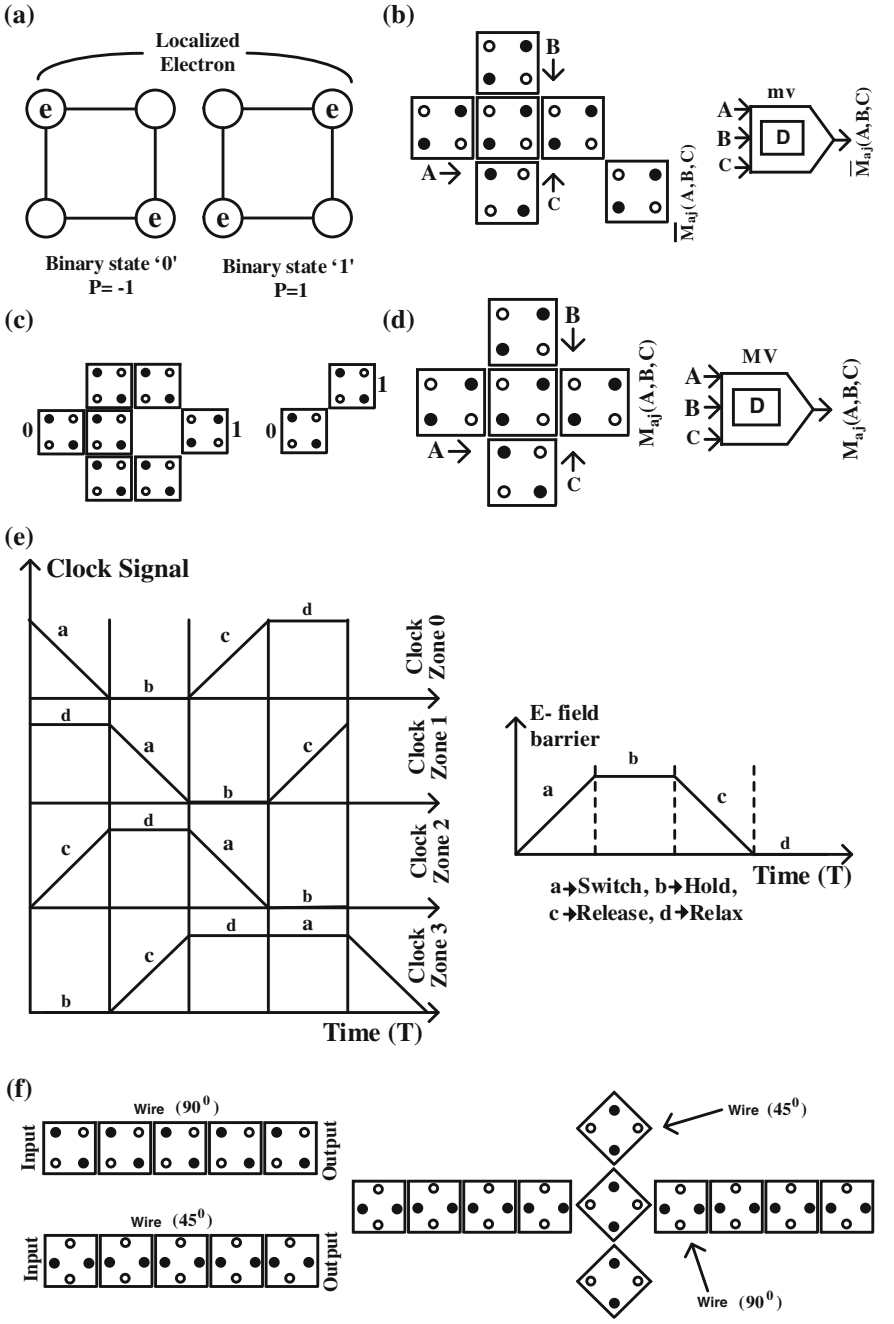

Fig. 2 **a** QCA cell with two binary interpretations of the states. **b** QCA minority voter. **c** QCA inverter. **d** QCA majority vote. **e** QCA phase and clock cycle. **f** QCA binary wire

Reversible logic gate: A reversible logic gate is an X-input and X-output logic gate that produces a unique output pattern for each possible input pattern [2, 3, 14, 16]. In reversible circuit design, the challenging task is to optimize parameters such as gate count, garbage outputs and quantum cost, otherwise the efficiency of circuit will degrade and also its cost.

Garbage outputs, sometime unwanted output, should be minimum.

Gate count and constant input should be minimum.

Total logical calculation and quantum cost should be minimum.

Fan-out is not allowed. That states each output can only singularly link to a preceding input.

3 Proposed Reversible Code Converters

In this section, we design an optimized and improved version of reversible 3-bit Binary to Gray and Gray to Binary code converters. Converters are design circuits in which a logic presented in one code is converted to another code.

3.1 New Type of Reversible Gates

In this subsection, we have designed two new types of 3×3 reversible gates that are used to construct the Binary to Gray and Gray to Binary code converters. BG-1 gate is a 3×3 type reversible gate and input vector corresponding to a unique output vector that can be uniquely determined. In Table 1, the input values are (0, 1, 2, 3, 4, 5, 6, 7) and the corresponding output values are (0, 3, 6, 5, 4, 7, 2, 1). Figure 3a, b depict the block diagram and equivalent quantum realization of the BG-1 gate. The quantum cost, of the BG-1 gate is 2. Another 3×3 type reversible gate is named as GB-1 (Gray to binary) gate. The corresponding truth table of GB-1 gate is shown in Table 2 in which the input values are (0, 1, 2, 3, 4, 5, 6, 7) and the corresponding output values are (0, 7, 6, 1, 4, 3, 2, 5). Figure 4a, b depict the block diagram and equivalent quantum realization of GB-1 gate. The quantum cost of the GB-1 gate is 2.

Table 1 Reversibility of the new type of BG-1 gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	0	0	1

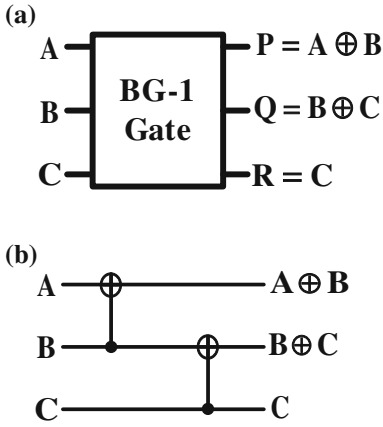

Fig. 3 **a** Block diagram of BG-1 Gate. **b** Quantum implementation of BG-1

Table 2 Reversibility of the new type of GB-1 gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	1	0	1

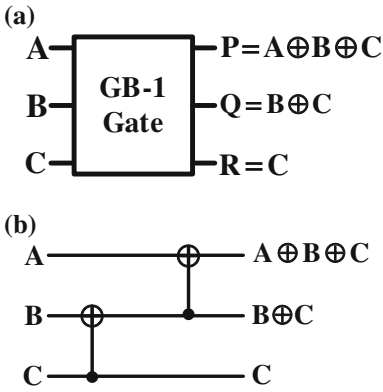

Fig. 4 **a** Block diagram of BG-1 Gate. **b** Quantum implementation of GB-1

3.2 Architecture of the Proposed Binary to Gray Code Converter

The QCA layout and block diagram of BG-1 gate are depicted in Fig. 5b, c. In the QCA layout, BG-1 gate is composed of 46 cells. Three inputs (binary code) to the cell are labelled as B_0, B_1 and B_2. The centre cell is the device cell (majority voter) that executes the operation of AND, OR with appropriate polarization. The other cell, labelled as G_0, G_1 and G_2 synthesize outputs (gray code). From the truth table, Table 1, it is obvious that $\mathbf{G_0 = B_0 \oplus B_1}$, $\mathbf{G_1 = B_1 \oplus B_2}$ and $\mathbf{G_2 = B_2}$. For setting (input A = B_0, B = B_1 and C = B_2) in BG-1 gate (shown in Fig. 5a).

The QCA block diagram of the Binary to Gray is drawn in Fig. 5c and can perform the majority of logic functions as

$$\mathbf{G_0 = M(M(\overline{B_1}, 0, B_0), M(B_1, 0, \overline{B_0}), 1),}$$
$$\mathbf{G_1 = M(M(\overline{B_1}, 0, B_2), M(B_1, 0, \overline{B_2}), 1),}$$
$$\mathbf{G_2 = B_2}$$

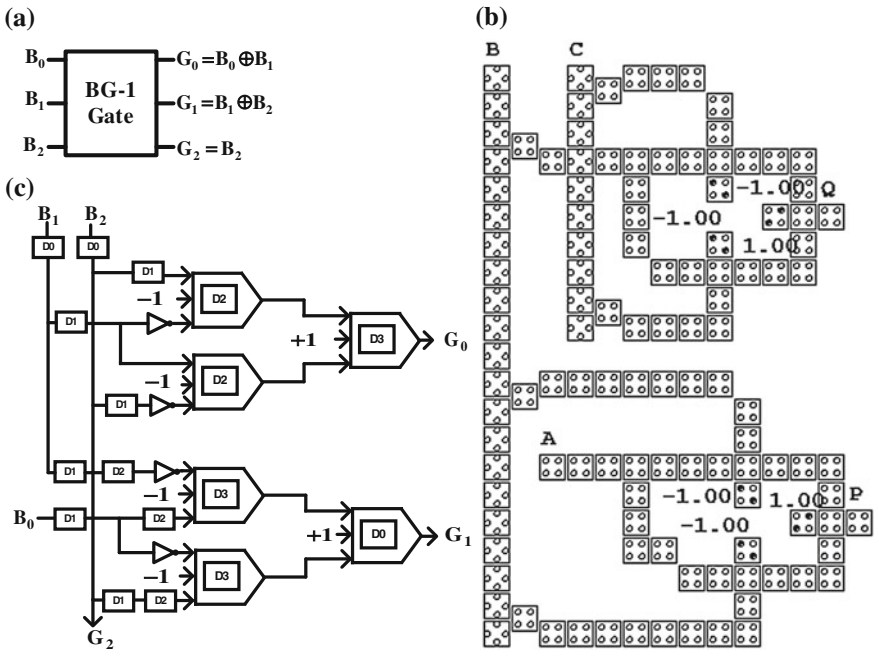

Fig. 5 **a** Block diagram of BG-1 to Gray converter. **b** QCA layout of Binary to Gray code converter. **c** QCA block diagram of Binary to Gray code converter

3.3 *Architecture of the Proposed Gray to Binary Code Converters*

The QCA layout and block diagram of GB-1 gate are depicted in Fig. 6b, c. The QCA layout of GB-1 gate is composed of 64 cells. Three gray code inputs G_0, G_1 and G_2 are applied instantly into the device cell (majority vote) that executes the operation of AND, OR with appropriate polarization. The other cell, labelled as B_0, B_1 and B_2 synthesize outputs (binary code). From the truth Table 2 we synthesis Boolean expressions as $\mathbf{B_0 = G_0 \oplus G_1 \oplus G_2}$, $\mathbf{B_1 = G_1 \oplus G_2}$ and $\mathbf{B_2 = G_2}$. For setting (input $A = G_1$, $B = G_2$ and $C = G_0$) in GB-1 gate (shown in Fig. 6a). The QCA block diagram of the Binary to Gray converter is drawn in Fig. 6c and can perform the majority and minority logic functions as

$$\mathbf{B_0 = M_{aj}(M_{aj}(G_1, G_2, 1), \overline{M}_{aj}(G_1, G_2, 0), G_0, 0), \overline{M}_{aj}((M_{aj}(G_1, G_2, 1), \overline{M}_{aj}(G_1, G_2, 0), 0), G_0, 0), 0)}$$

$$\mathbf{B_1 = M_{aj}(M_{aj}(G_1, G_2, 1), \overline{M}_{aj}(G_1, G_2, 0), 0),\ B_2 = G_2}$$

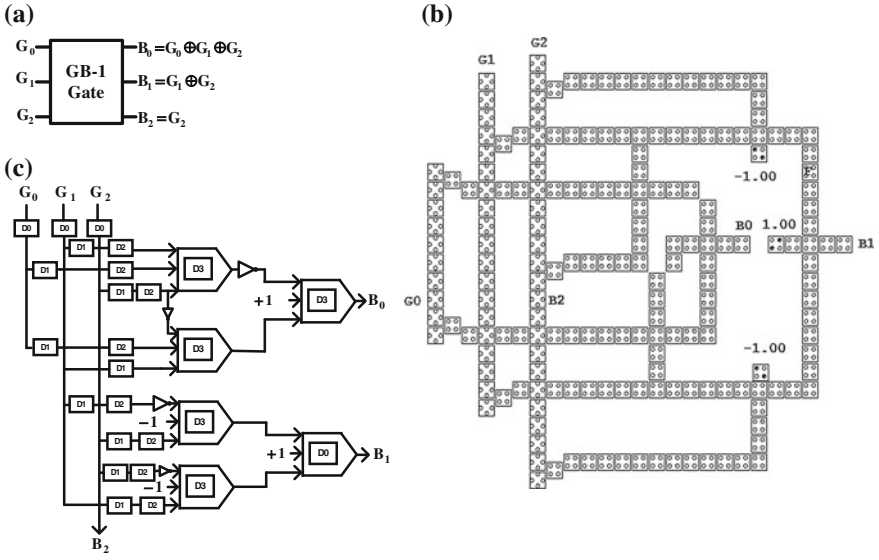

Fig. 6 **a** Block diagram of GB-1. **b** QCA layout of Gray to Binary code converter. **c** QCA block diagram of Gray to Binary code converter

4 Simulation Setup Results

The two different code converters have been laid out and simulated by using QCADesigner v2.0.3 tool. In this simulation, we used the bistable approximation and the following set parameters: (number of samples 12800, radius of effect 65 nm, clock amplitude factor 2, convergence tolerance 0.001000, relative permittivity 12.9, clock high and low are $9.8e^{22}$ and $3.8e^{23}$, respectively, maximum iterations per sample 100, cell size 18 nm × 18 nm and dot diameter 5 nm) (Figs. 7 and 8).

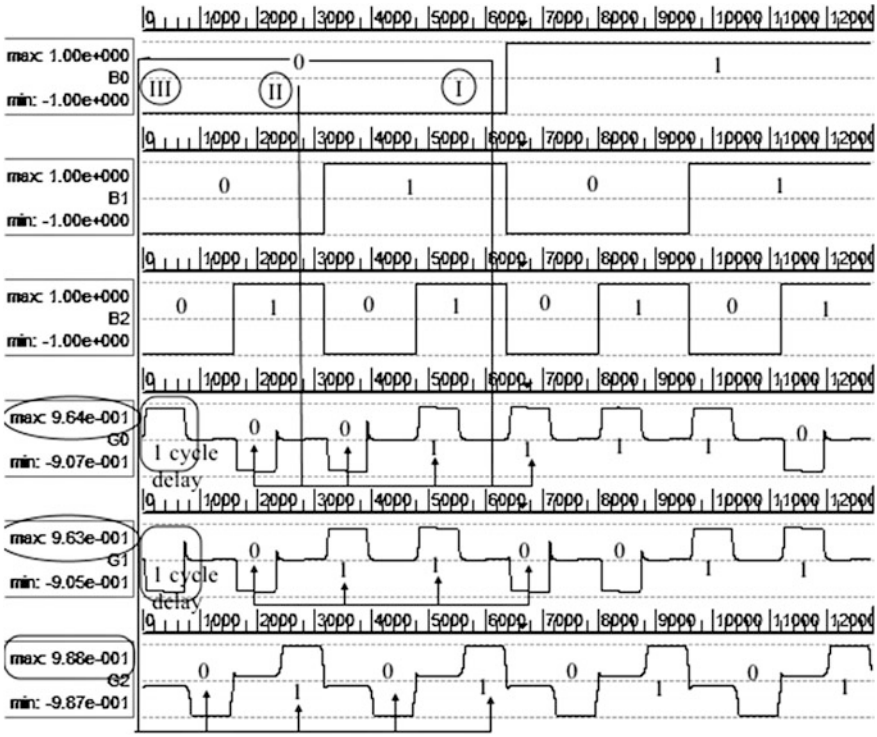

Fig. 7 Simulation results for Binary to Gray code converter

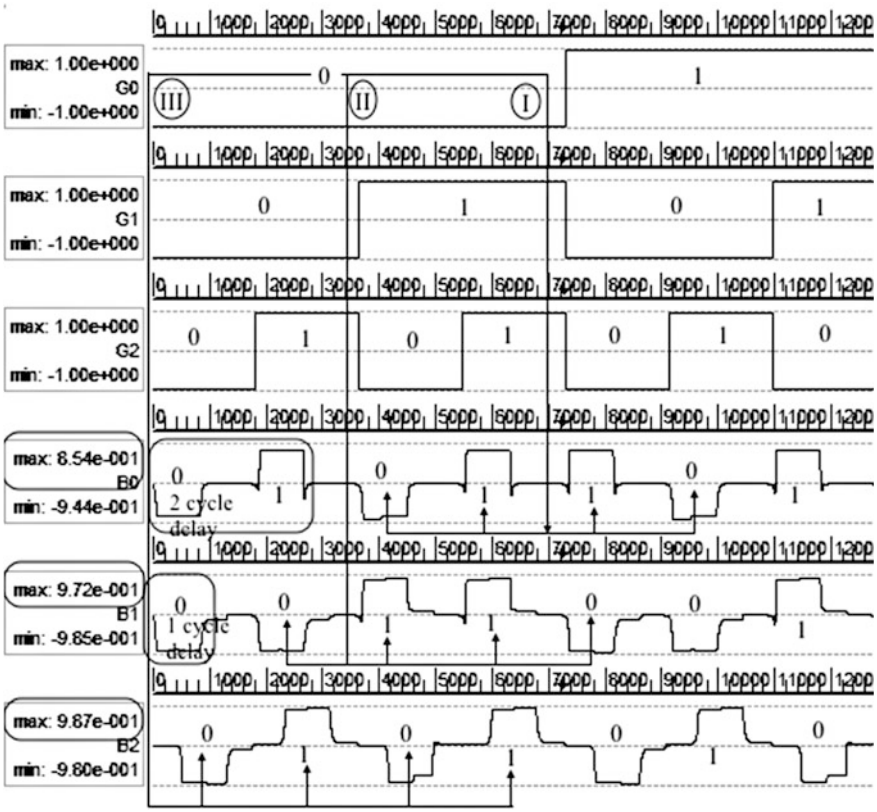

Fig. 8 Simulation results for Gray to Binary code converter

5 The Comparative Performance Tables 3, 4 and 5 of New Designs

The comparative performance Tables 3, 4 and 5 sketches the performance of our proposed designs with existing designs in terms of number of majority gate (MV), cell count and latency. The QCA layouts used the designs of L-shaped wire, majority vote (MV) and inverters. The stability and robustness of these designs can be tested based on cell count, area and latency.

Table 3 Comparative analysis of the various reversible Binary to Gray code converter

Designs	NOG	GO	CI	QC	Delay	TLC
Proposed	1	0	0	2	1	2α
[17]	2	1	0	2	1	2α
[16]	3	0	0	3	3	3α
[18]	3	3	0	3	3	3α

Table 4 Comparative analysis of the various Gray to Binary code converters

Designs	NOG	GO	CI	QC	Delay	TLC
Proposed	1	0	0	2	1	3α
[17]	2	0	0	2	2	3α
[16]	3	0	0	3	3	3α
[18]	5	3	2	5	5	3α + 2β

Table 5 Code converter designs comparison table

Designs	No. of MV used	Complexity (# cell)	Latency	Total Area (nm^2)	Cell area (nm^2)	Area usage (%)
[14] (Binary to Gray)	6 Majority + 4 Inverter	118	Not mentioned	92,664	38,232	45
[14] (Gray to Binary)	6 Majority + 4 Inverter	112	Not mentioned	139,968	36,288	41.25
Proposed (Binary to Gray)	6 Majority + 7 Inverter	90	1 + 1 + 0 = 2	95,658	29,160	30.04
Proposed (Gray to Binary)	6 Majority + 9 Inverter	194	2 + 2 + 0 = 4	280,171	62,856	22.43

6 Conclusion

This paper has presented the QCA implementations of a Binary to Gray and Gray to Binary code converters using two new types of reversible gates. For the first time ever proposed in the literature with an optimal approach and using emerging nanotechnology archetype QCA Designer tool. The new types of gates have a capability to optimize reversible parameters for the design of converters. The nanoscale Binary to Gray converter design requires, area (proposed design has 95,658 nm^2 compared with 38.232 nm^2 [17]), number of MVs used (proposed design has 6Majority + 3inverters compared with 6Majority + 4inverter [17]) and complexity (proposed design requires 46 cells compared with 118 [17]), whereas

the nanoscale Gray to Binary converter requires, area (proposed design has 20,736 nm^2 compared with 36.288 nm^2 [17], number of MVs used (proposed design has 6Majority + 1inverter compared to 6Majority + 4inverter [17]) and complexity (proposed 64 cells compared with 112 [17]). Moreover, we have verified the functionality of the proposed converters in QCA-Designer tool. Finally, converter circuit reveals the major QCA advantages such as less area utilized, high device density and latency. The proposed design outperforms the existing ones in terms of scalability and efficiency. The proposed converter circuits will be useful in many applications such as inside computer operations, communication systems many digital circuits, etc.

References

1. Wairya, S., Nagaria, R.K., Tiwari, S.: Performance analysis of high speed hybrid CMOS full adder circuits for low voltage VLSI design. VLSI Des. **7** (2012)
2. Misra, N.K., Wairya, S., Singh, V.K.: Preternatural low-power reversible decoder design in 90 nm technology node. Int. J. Sci. Eng. Res. **5**(6), 969–978 (2014)
3. Misra, N.K., Mukesh, M.K., Wairya, S., Kumar, A.: Cost efficient design of reversible adder circuits for low power applications. Int. J. Comput. Appl. **117**(19), 37–45 (2015)
4. Misra, N.K., Wairya, S., Singh, V.K.: An inventive design of 4*4 bit reversible NS gate. In: Recent Advances and Innovations in Engineering (ICRAIE), pp. 1–6, IEEE (2014)
5. Walus, K., Dysart, T.J., Jullien, G., Budiman, R.A.: QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**(1), 26–31 (1973)
6. Landauer, R.: Irreversibility and heat generation in the computing process. IBM J. Res. Dev. **5**(3), 183–191 (1961)
7. Bennett, C.H.: Logical reversibility of computation. IBM J. Res. Dev. **17**(6), 525–532 (1973)
8. Saravanan, P., Kalpana, P.: A novel and systematic approach to implement reversible gates in quantum dot cellular automata. Quantum **2**(5), 15 (2013)
9. Misra, N.K., Wairya, S., Singh, V.K.: Approaches to design feasible error control scheme based on reversible series gates. Eur. J. Sci. Res. **129**(3), 224–240 (2015)
10. Saravanan, M., Manic, K.S.: Energy efficient code converters using reversible logic gates. In: IEEE International Conference on Green High Performance Computing (ICGHPC), pp. 1–6 (2013)
11. Misra, N.K., Wairya, S., Singh, V.K.: Evolution of structure of some binary group-based Nbit comparator. NTO-2 N Decoder Byreversible Technique (2014)
12. Angizi, S., Alkaldy, E., Bagherzadeh, N., Navi, K.: Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. J. Low Power Electron. **10**(2), 259–271 (2014)
13. Sarker, A., Bahar, A.N., Biswas, P.K., & Morshed, M.: A novel presentation of Peres Gate (Pg) in Quantum-Dot Cellular Automata (QCA). Eur. Sci. J. **10**(21) (2014)
14. Thapliyal, H., Ranganathan, N.: Conservative QCA gate (CQCA) for designing concurrently testable molecular QCA circuits. In: 22nd International Conference on IEEE VLSI Design, pp. 511–516 (2009)
15. Sen, B., Dutta, M., Goswami, M., Sikdar, B.K.: Modular Design of testable reversible ALU by QCA multiplexer with increase in programmability. Microelectron. J. **45**(11), 1522–1532 (2014)
16. Haghparast, M., Hajizadeh, M., Hajizadeh, R., Bashiri, R.: On the synthesis of different nanometric reversible converters. Middle-East J. Sci. Res. **7**(5), 715–720 (2011)

17. Das, J.C., De, D.: Reversible binary to grey and grey to binary code converter using QCA. IETE J. Res. (ahead-of-print) 1–7 (2015)
18. Saligram, R., & Rakshith,T. R.: Novel code converter employing reversible logic. Int. J. Comput. Appl. **781** (2012)