2-Dimensional 2-Dot 1-Electron Quantum Cellular Automata-Based Dynamic Memory Design

Mili Ghosh, Debarka Mukhopadhyay and Paramartha Dutta

Abstract Quantum dot cellular automata (QCA) is supposed to be the most promising technology which is an efficient nanotechnology and overcomes the limitations of the CMOS technology. Thus this technology is considered as the most preferable replacement of CMOS. This paper presents a design methodology of dynamic memory using 2-dot 1-electron QCA. According to the best of our knowledge, this has not been reported yet. The proposed design is supposed to be an optimum design with respect to cell requirement.

Keywords Dynamic memory · 2-dot QCA · Memory loop · Majority voter · Planar crossing

1 Introduction

From the last few decades, the names of CMOS technology and the digital industry are taken synonymously. However, in recent times CMOS technology faces serious challenges due to rapid development in digital industry with increased cost [1]. QCA is one of the most promising emerging nanotechnologies which satisfies the said urge. Its high-density cost-effective capability with high-speed nanoscale architecture makes it an ideal replacement of CMOS technology in the near future. 2-dot 1-electron QCA is one of the recent structural forms of QCA which depicts binary

M. Ghosh (✉) · P. Dutta
Department of Computer & System Sciences, Visva Bharati University, Santiniketan, India
e-mail: ghosh.mili90@gmail.com

P. Dutta
e-mail: paramartha.dutta@gmail.com

D. Mukhopadhyay
Department of Computer Science & Engineering, Bengal Institute of Technology and Management, Santiniketan, India
e-mail: debarka.mukhopadhyay@gmail.com

S. Das et al. (eds.), *Proceedings of the 4th International Conference on Frontiers in Intelligent Computing: Theory and Applications (FICTA) 2015*, Advances in Intelligent Systems and Computing 404, DOI 10.1007/978-81-322-2695-6_30

information with the position of a single electron within a cell. As other forms of QCA, 2-dot 1-electron QCA transfers information using cell-to-cell interaction which follows the Coulomb's law. The advantages of 2-dot 1-electron QCA by the time are well known [2].

The domain of memory design using 4-dot 2-electron QCA has been widely explored. There exist numerous previous reportings in this domain such as [3–5]. In case of 4-dot 2-electron, the domain of parallel memory is also explored such as [6]. Here, we will focus only on the serial memory structures. The 2-dot 1-electron QCA is one of the latest domains of nanotechnology. So a few previous reportings exist in this domain such as [2, 7]. The basic components of any 2-dot 1-electron QCA are binary wire, majority voter gate, inverter, and planar crossing of wires as proposed in [2]. Clocking as stated in [8–10] is the most important aspect of any QCA design. In this article, we propose a design methodology of dynamic memory using 2-dot 1-electron QCA. The implementation of dynamic memory in 2-dot 1-electron QCA is completely planar. In [3], a square cell-based approach of memory design has been proposed. It basically uses a loop-based memory layout in 4-dot 2-electron QCA and enables data storage with the use of loopback construct. It consists of a majority voter gate and a feedback loop. Another reporting is done as in [4] known as H-memory architecture. The design resembles a binary tree structure with control circuit at each step. This design facilitates high density with equal access time. Memory designs using QCA using alternative clocking mechanism is reported in [5]. This memory structure provides a special arrangement for majority voter gate in which the signal wires behave differently with the clock phase. This approach uses the majority voter gate as a memory element and behaves accordingly as a shift register.

2 Basics of 2-Dot 1-Electron QCA

The base of QCA technology lies on the concept of cells. Cells are the building blocks of any QCA design. The most common form of QCA is 4-dot 2-electron QCA which contains four quantum dots and two electrons. The 2-dot 1-electron QCA consists of two quantum dots and one electron. The electron can tunnel between the quantum dots. 2-dot 1-electron QCA cells can align either horizontally or vertically as shown in Fig. 1. Figure 1 also shows how the electron alignment within a cell carries

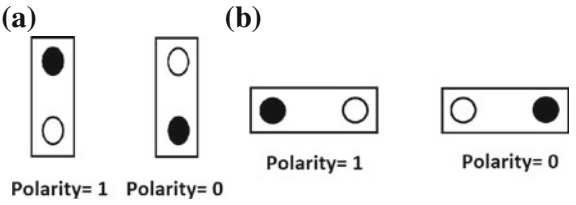

Fig. 1 Binary encoding in 2-dot 1-electron QCA cell **a** with vertical alignment and **b** with horizontal alignment

(i) Inverting (ii) Non-inverting (iii) Non-inverting (iv) Inverting

Fig. 2 Inversion by corner cell placement

binary information. This shows the most general convention. The basic components of any 2-dot 1-electron QCA architecture are wire, majority voter gate, and inverter as mentioned in [2]. The corner placement of 2-dot 1-electron QCA cells are shown in Fig. 2.

2.1 Clocking Mechanism

Clocking in case of QCA plays a significant role [11]. The purpose of clocking a QCA circuit is a bit different from that used in CMOS clocking. 2-dot 1-electron QCA uses the same clocking mechanism as general QCA clocking. QCA uses quasi-adiabatic clocking mechanism. In case of CMOS digital designs, clocking is used for the purpose of synchronization, whereas in case of QCA, clocking is used for controlling the data flow and supplying energy to weak input signals. QCA clocking has four phases: switch, hold, release, and relax. The electron potentials are initially low [12] and start to increase gradually in the switch phase. In the hold phase, the electron potentials are maximum and the cells do not have any definite polarity at this stage. During the release phase, the electron potentials start to lower and the cells gradually attain their polarity. During the relax phase, the electron potentials are minimum and the cells attain definite polarity. The actual computation of QCA is done in the release phase. Every QCA architecture is divided into four clock zones and each clocking zone consists of four phases. Each clock zone is $\frac{\pi}{2}$ out of phase with the next clock zone as shown in Fig. 3. The color scheme convention we use in this article to specify different clock zones is shown in Fig. 4.

3 Dynamic Memory

Dynamic memory is the most common type of memory used presently. Dynamic memory stores each bit of data in a separate unit. It is a kind of volatile memory, as it loses its data, once power is removed. Dynamic memory has to be refreshed periodically to maintain the data in the memory. Dynamic memory is preferred over static memory due to its structural simplicity. Thus, the basic characteristics of dynamic memory include

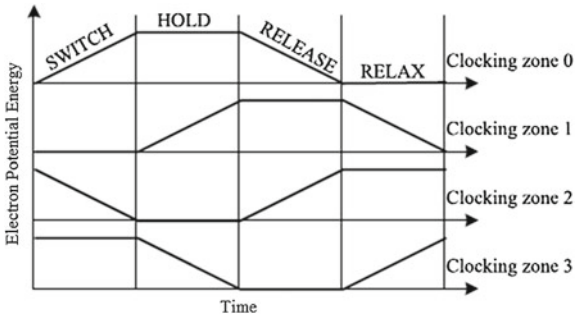

Fig. 3 2-dot 1-electron QCA clocking

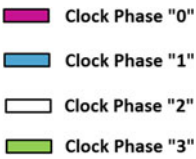

Fig. 4 Color code of different clock zones

1. Dynamic memory loses its data with removal of power.
2. Dynamic memory has to be refreshed periodically to retain the data in the memory.

3.1 Design of Dynamic Memory

A simple loop-based design of the dynamic memory is proposed in this article. As shown in Fig. 5, a feedback loop is incorporated to retain the data stored. We use a majority voter gate along with a feedback loop to serve the purpose of data. The 2-dot 1-electron QCA implementation is shown in Fig. 6. In QCA, to retain the state of a cell, one has to refresh it time to time. This ensures the dynamism in memory

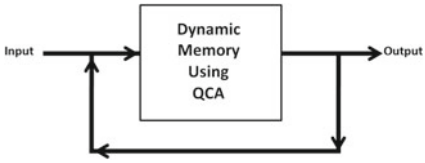

Fig. 5 Block diagram of dynamic memory

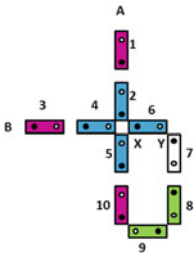

Fig. 6 Dynamic memory implementation using 2-dot 1-electron QCA with cell positions

realization. So we exploit this property of QCA to design dynamic memory unit. The majority voter gate in QCA has three input cells. In the proposed design, one of the inputs is used to feed the loopback data to the majority voter gate. The rest two inputs, denoted by A and B respectively, are assigned according to the user need. If we want to retain the previous input, we have to apply input 0 and 1 to the inputs of the proposed design A and B or the reverse. The third input of the majority voter gate in 2-dot 1-electron QCA is inverted naturally. So we apply the inverse of the previous data input to the third input of the majority voter gate in the design as shown in Fig. 6. In both cases, the majority voter gate will retain the previous data, which can be assured from Eq. 1. To write a new value say N to the memory, inputs A and B both are made equal to the value N. Then, the data value N persists in the memory as per Eq. 2.

$$\begin{aligned} M(1, 0, Prev') = M(0, 1, Prev) &= 1.0 + 0.(Prev')' + 1.(Prev')' \\ &= 1.0 + 0.Prev + 1.Prev \\ &= Prev \end{aligned} \tag{1}$$

$$\begin{aligned} M(N, N, Prev') &= N.N + N.(Prev')' + N.(Prev')' \\ &= N.N + N.Prev + N.Prev \\ &= N \end{aligned} \tag{2}$$

A multibit dynamic memory implementation can be done as shown in Fig. 7. A shown in the figure, separate dynamic memory 1 bit unit for each bit has to be incorporated. Thus to construct N bit dynamic memory unit we have to use N such 1 bit unit. The 2-dot 1-electron QCA implementation of N bit dynamic memory is shown in Fig. 8.

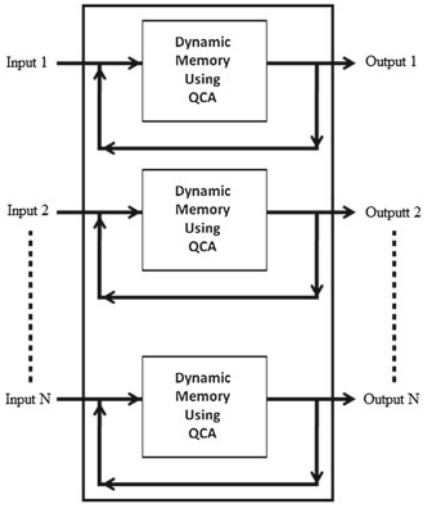

Fig. 7 Block diagram of N bit dynamic memory

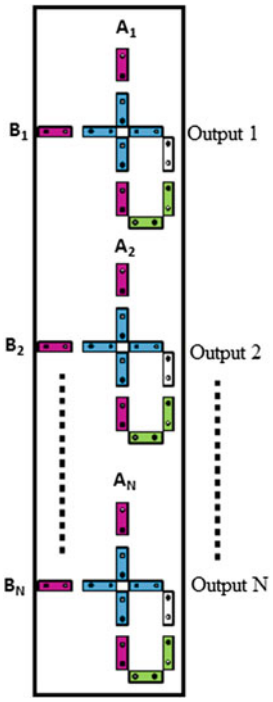

Fig. 8 N bit dynamic memory 2-Dot 1-electron QCA

3.2 Determination of Output State

As open-source simulator QCA Designer [13] of 4-dot 2-electron QCA, there does not exist such an open-source simulator for 2-dot 1-electron QCA. So we justify our proposed design using potential energy calculations as had been done in [14, 15].

The potential energy between two point electron charges is evaluated by Eq. 3.

$$U = Kq_1q_2/r \tag{3}$$

$$Kq_1q_2 = 9 \times 10^9 \times (1.6)^2 \times 10^{-38} \tag{4}$$

$$U_T = \sum_{t=1}^{n} U_t \tag{5}$$

where U is the potential energy between two point charges, q_1 and q_2 are the point electric charges, K is the Boltzman constant, and r is the distance between the two point charges. The term U_T is the total potential energy of a particular electron position within a 2-dot 1-electron QCA cell. An electron has negative charge and a quantum dot has induced positive charge. The potential energies exist between each neighbor electron with the respective electron position of the output cells. Electron tends to latch at a position at which the potential energy is minimum. So the

Table 1 Output state of dynamic memory

Cell	Electron position	Total potential energy	Comments
1	–	–	Input cell with polarity 0
2	–	–	Attains the polarity of cell 1
3	–	–	Input cell with polarity 1
4	–	–	Attains the polarity of cell 3
5 (*initial*)	–	–	Initially with polarity 0
6	x	-3.33×10^{-20} J	Electron will latch at position × due to less energy
6	y	-0.54×10^{-20} J	
7	–	–	Attains polarity of cell 6 due to cell placement as shown in Fig. 2(iii)
8	–	–	Attains the polarity of cell 7
9	–	–	Attains inverse polarity of cell 8 due to cell placement as shown in Fig. 2(i)
10	–	–	Attains polarity of cell 9 due to cell placement as shown in Fig. 2(ii)
5	–	–	Attains the polarity of cell 10

comparison of the total potential energies for the possible positions of an electron shows which electron position is more stable. The size of each 2-dot 1-electron QCA cell is 13 nm × 5 nm and the inter dot distance between two adjacent cells is 5 nm [2].

Figure 6 shows the dynamic memory design with 2-dot 1-electron QCA with cell numbers. The potential energy calculations are shown in Table 1.

4 Stability and Compactness of Proposed Design

Stability plays an important role to determine the acceptability and efficiency of a design. There are certain properties which ensure stability of a design. These are as follows:

1. Input signals of a Majority Voter gate must reach the inputs at the same time and with the same strength.
2. All the cells of a Majority Voter gate must be at the same clock zone.
3. The output of a Majority Voter gate must be taken off either at the same clock or at the next clock.

The proposed design met all the conditions and ensures stability as well. Another important measure of any 2-dot 1-electron QCA is compactness. 2-dot 1-electron QCA cells have rectangular structure. Let us assume that the cells have a size of $a \times b$. The design of dynamic memory as seen in Fig. 6 consists of 10 such cells. The area of coverage of the design is $12ab$ and the cell coverage area is $10ab$. Thus

the ratio of coverage area is 10 : 12. So the index of compactness of the proposed design is 83 %. Thus the design facilitates with a high degree of compactness.

Robustness is another measure for any QCA architecture. To achieve robust signal transmission through a QCA architecture, it is desirable that more than one cell are incorporated per intermediate (non-input and non-output) clock zone. In [16], the maximum number of cells that can be accommodated within a clock zone has been derived. The reported design of dynamic memory consists of two clock zones which consists of only one cell as we can see in Fig. 6 cells 7 and 10. So the number of cells will be increased by two to achieve higher degree of robustness. However, the proposed design ensures stability as well as high degree of compactness.

5 Conclusion

We have proposed a design of dynamic memory using 2-dot 1-electron QCA. The design has been verified using potential energy calculations. We also give the stability measure and degree of compactness of the proposed design.

Acknowledgments The authors would like to thank the Department of Computer and System Sciences, Visva-Bharati, Santiniketan and the Department of Computer Science and Engineering, Bengal Institute of Technology and Management, Santiniketan for their infrastructure support. The authors gratefully acknowledge the support of INSPIRE Fellowship (Serial No. 1513–2012, INSPIRE Reg. No. IF31027) for pursuing Doctoral Research in any Indian University by Department of Science and Technology, Ministry of Science and Technology, Government of India.

References

1. International Technology Roadmap for Semiconductor (ITRS): http://www.itrs.net
2. Hook, L.R., IV, Lee, S.C.: Design and simulation of 2-d 2-dot quantum-dot cellular automata logic. IEEE Trans. Nanotechnol. **10**, 996–1003 (2011)
3. Berzon, D., Fountain, T.J.: A memory design in QCAs using the squares formalism. In: Proceedings of the Great Lakes Symposium on VLSI, pp. 166–169. IEEE, Mar 1999
4. Frost, S.E., Rodrigues, A.F., Janiszewski, A.W., Rausch, R.T., Kogge, P.M.: Memory in motion: a study of storage structures in QCA. In: Proceedings 1st Workshop on Non-Silicon Computing (2002)
5. Vankamamidi, V., Ottavi, M., Lombardi, F.: A Line-based parallel memory for QCA Implementation. IEEE Trans. Nanotechnol. **4**, 690–698 (2005)
6. Ottavi, M., Pontarelli, S., Vankamamidi, V., Salsano, A., Lombardi, F.: Design of a QCA memory with parallel read/serial write. In: Proceedings. IEEE Computer Society Annual Symposium on VLSI, pp. 292–294. IEEE, May 2005
7. Hook, L.R., IV, Lee, S.C.: Collinear 2-dot QCA nano-electronic wire structure to improve QCA computing device reliability. In: Proceedings SPIE Smart Structure Conference, vol. 1 (2011)
8. Vetteth, A., Walus, K., Dimitrov, V.S., Jullien, G.A.: Quantum-Dot Cellulur Automata of Flip Flop. ATIPS Laboratory, Alberta (2003)
9. Mukhopadhyay, D., Dinda, S., Dutta, P.: Designing and implementation of quantum cellular automata 2:1 multiplexer circuit. Int. J. Comput. Appl. **25**, 21–24 (2011)

10. Dutta, P., Mukhopadhyay, D.: New architecture for flip flops using quantum-dot cellular automata. In: Proceedings of the 48th Annual Convention of Computer Society of India. Vol II Advances in Intelligent Systems and Computing, vol. 249, pp. 707–714. Springer (2013)
11. Dutta, P., Mukhopadhyay, D.: A Study on energy optimized 4 dot 2 electron two dimensional quantum dot cellular automata logical reversible flip-flops. Microelectron. J. **46**, 519–530 (2015) (Elsevier)
12. Blum, K.: Density Matrix Theory and Applications. Springer Series on Atomic, Optical and Plasma Physics (2012)
13. Walus, K., Dysart, T., Jullien, G.A., Budiman, R.A.: QCA designer: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**, 26–31 (2004)
14. Mukhopadhyay, D., Dutta, P.: Qca based novel unit reversible multiplexer. Adv. Sci. Lett. **16**, 163–168 (2012)
15. Ghosh, M., Mukhopadhyay, D., Dutta, P.: A 2 dot 1 electron quantum cellular automata based parallel memory. In: Information Systems Design and Intelligent Applications. Advances in Intelligent Systems and Computing, vol. 339, pp. 627–636. Springer (2015)
16. Huang, J., Momemzadeh, M., Lombardi, F.: Design of Sequential Circuits by Quantum-dot Cellular Automata. Microelectron. J. **38**, 525–537 (2007) (Elsevier)