Design Specifications of Reversible Logic Using CMOS and Quantum Dot Cellular Automata

Shaik Shabeena and Jyotirmoy Pathak

Abstract Reversible Logic is solitary emerging technology that that promises zero-power dissipation. Multiple function generation, low-power VLSI, optical information processing, and quantum computing are the main applications of this logic. Without the reversible logic quantum computing is not implemented. This paper focuses on the designing of reversible logic gates and their design specifications using CMOS and QCA. The reversible gates are used in redesigning of intricate systems that are embedded with reversible circuits as a primal component and execute multiple sets of instruction in quantum computers. The reversible circuits shape the indispensable building block architecture of quantum-based computers as all quantum operations are destined to be reversible. These gates are implemented and results are shown in Cadence Virtuoso and QCADesigner version 2.0.3.

Keywords Reversible logic · Reversible gates · Quantum dot cellular automata (QCA) · Nanoelectronics · Cadence virtuoso

1 Introduction

In today's rising technology, power dissipation is the major issue. When high-technology circuits are implemented then some information loss will be present. Owing to this information loss, energy will dissipate. According to Landauer's theory, the amount of data loss is ktln2 joules for one bit as energy dissipation process [1]. For conservative logic schematic, every single operation dissipates some amount of heat energy in the form of information loss. This happens because of second law of thermodynamics; in any method once information is lost it cannot

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be recovered. After Landauer's theory, in the year 1973 Bennett proposed a theory to avoid the waste of information wholly; and circuits must be designed using reversibility concept [2].

This reversibility concept actuates energy solution to many upcoming fields of nanotechnology which is related to quantum computing [3]. The gates which regenerate the inputs from the available outputs are known as reversible gates. It has equal number of IN and OUT lines whereas the unused output lines in any circuit were taken as garbage signal and the fan-out must be one. The main principle behind reversibility concept is to store the cells which are having charge electrically when switching operations are done and then there is no waste of information. Then it will be able to use again through reversible computing [3].

However, the industry is besieged to make small-scale transistors and improvement in clocking speed. To overcome all the precincts of CMOS, researchers are looking for alternative emerging technology. The quantum dots are semiconductor material and the size is in nanometers. In 1993, QCA is introduced by Lent et al. QCA technology is an alternative to CMOS. This can be considered as rising technology of nanoelectronics to replace the current transistors in semiconductor design. Unlike the conservative transistor which transfers information through voltage or current, in QCA the circuits are transferring these bits of information through the cells interaction [4]. The circuit consumes extremely low power and there is no need of interconnections at all [3].

This paper is described as follows: Sect. 2 focus upon outline of reversible gates as well as QCA technology. Section 3 explains execution of reversible logic gates in 0.09 μm and QCA technology. Section 4 introduces results of reversible gates. Section 5 gives overall design specifications of reversible gates. Section 6 concludes the paper.

2 Reversibility in QCA

2.1 Reversible Gates

In a quantum system, reversible computation can be performed only when it encompasses of reversible logic gates. When a system acts as reversible then its input and output lines can be unique and input lines are generated from output lines. And there is one-to-one present between its inputs and outputs [5].

In reversible gates, power dissipation is a vital specification in circuit design. It can be minimized (theoretically zero) and by the use of these dissipation-less gates, we can achieve nil-power-dissipation circuits [6]. To achieve a nonreversible function, it must be implanted into a reversible one, and this will produce garbage outputs and constant inputs. Garbage outputs mean unused outputs in circuit that means for the outputs that are not cared. The essential reversible logic gates and their schematics are shown below [3].

1. *Feynman Gate* (Fig. 1)
2. *Toffoli Gate* (Fig. 2)
3. *Fredkin Gate* (Fig. 3)
4. *Peres Gate* (Fig. 4)

2.2 Quantum Dot Cellular Automata

In contrast to electronics which is based on transistors, QCA does not work on the transport of electrons, but by the arrangement of electrons in a small, limited area of only a few square nanometers. It is implemented by quadratic cells, therefore it is called QCA. In these small squares, precisely, four potential wells are located; one well is situated in each corner of QCA cell. In individual QCA cell, exactly two electrons are sealed. These two electrons can only reside in the potential well (Fig. 5).

There are two diagonals in a square, which means the electrons can dwell in exactly two possible variations in a QCA cell. It means each cell can be in two states. Much precisely, a high voltage is often interpreted as binary '1' and a low voltage as binary '0' [7].

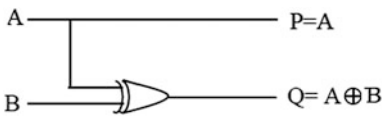

Fig. 1 Structure of Feynman gate

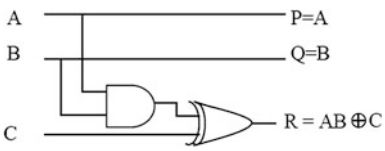

Fig. 2 Structure of Toffoli gate

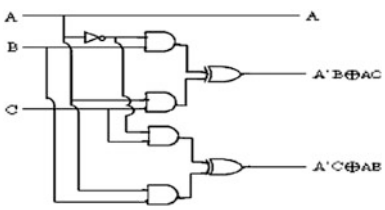

Fig. 3 Structure of Fredkin gate

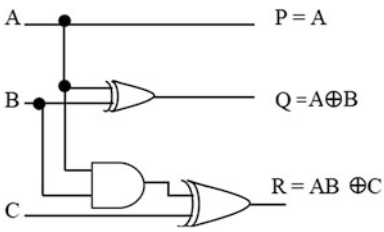

Fig. 4 Structure of Peres gate

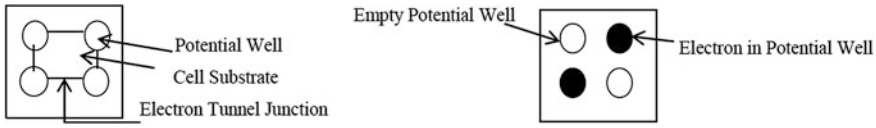

Fig. 5 Structure of QCA cell

If two QCA cells are placed side by side then there is a possibility to interchange their states. The QCA cell that has to transfer its state to a next cell must have its tunnel junctions connected, and the tunnel junctions in the side cells have to be exposed to allow the electrons to move via the tunnel junctions between the two potential wells (Figs. 6, 7, 8, 9, 10, 11, 12 and 13).

3 Implementation of Reversible Gates

Reversible gates can be implemented by using both Cadence Virtuoso and QCA Designer tool version 2.0.3 [8].

3.1 Using 0.09 μm Technology

1. Feynman Gate
2. Toffoli Gate
3. Fredkin Gate
4. Peres Gate

3.2 Using Quantum Technology

1. Feynman Gate

The implemented Feynman gate consists of two AND gates, two inverters, and one OR gates.

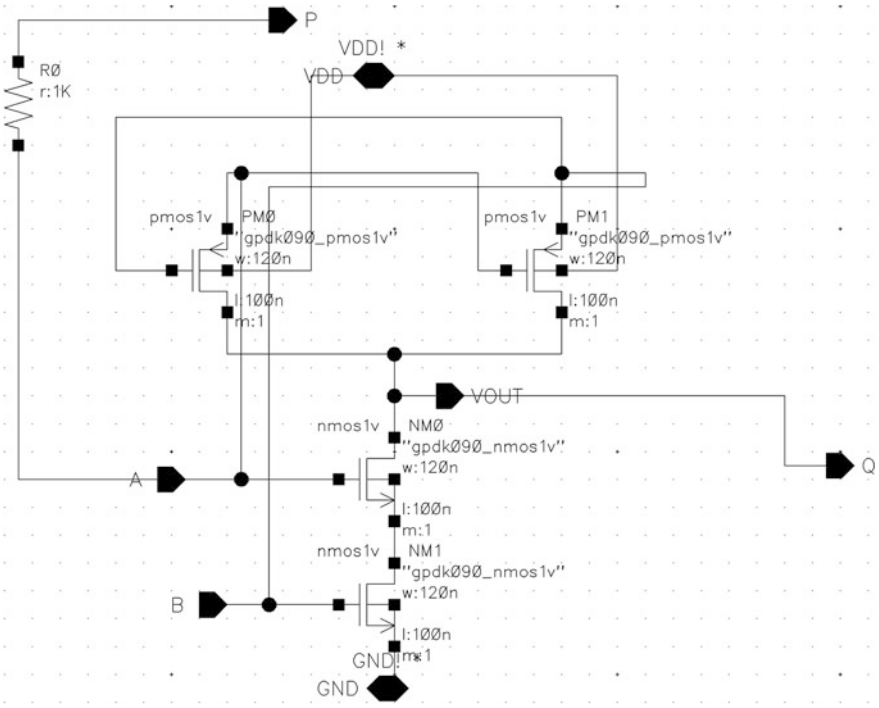

Fig. 6 CMOS-based Feynman gate

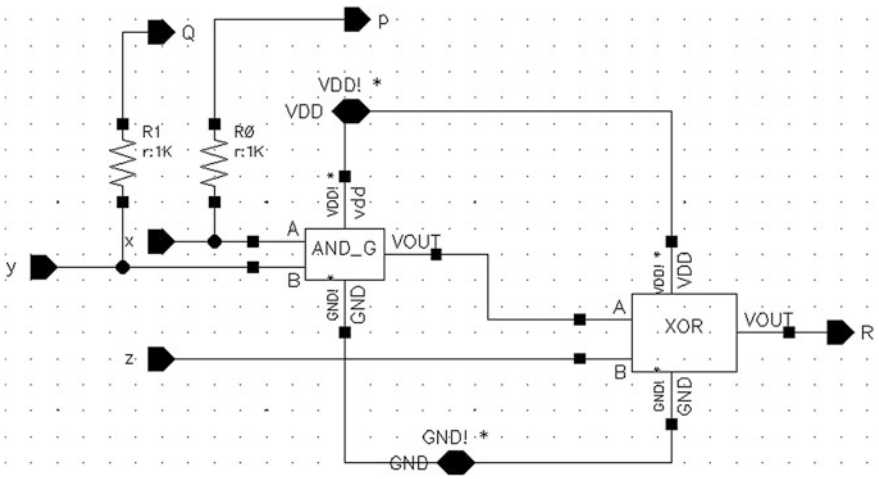

Fig. 7 CMOS-based Toffoli gate

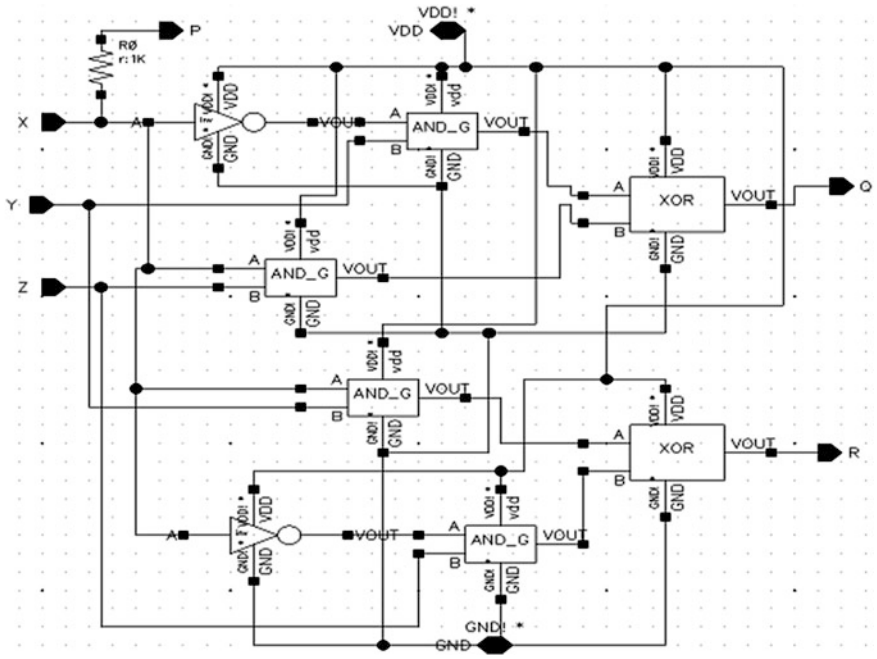

Fig. 8 CMOS-based Fredkin gate

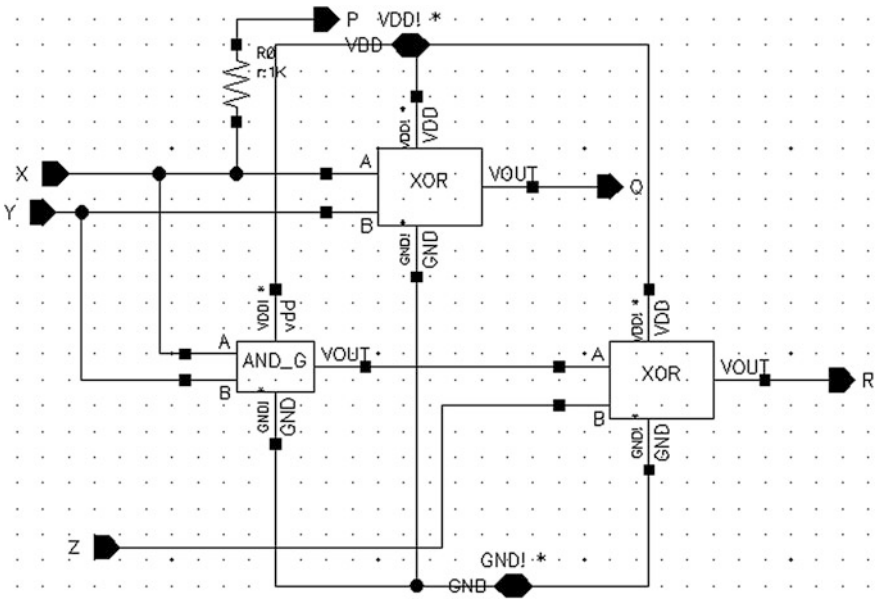

Fig. 9 CMOS-based Peres gate

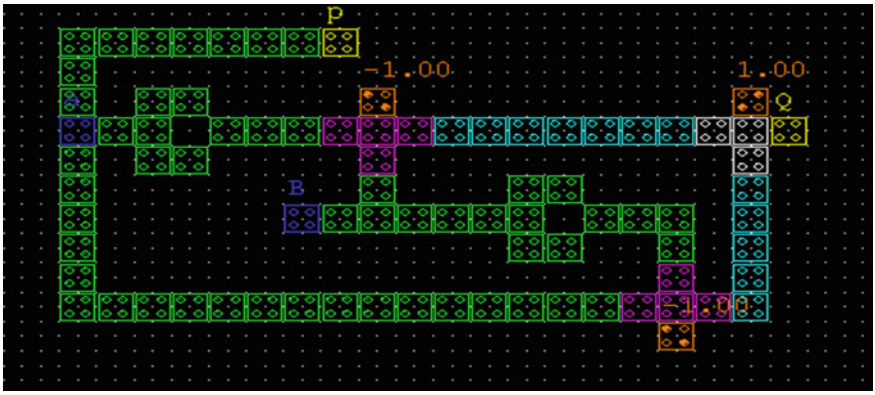

Fig. 10 QCA-based Feynman gate

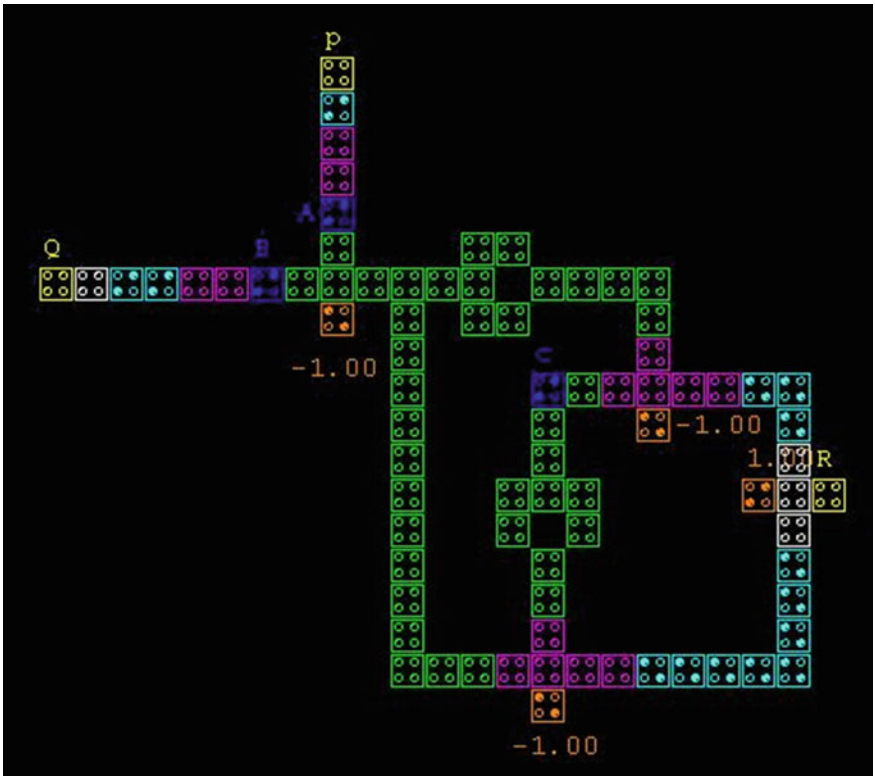

Fig. 11 QCA-based Toffoli gate

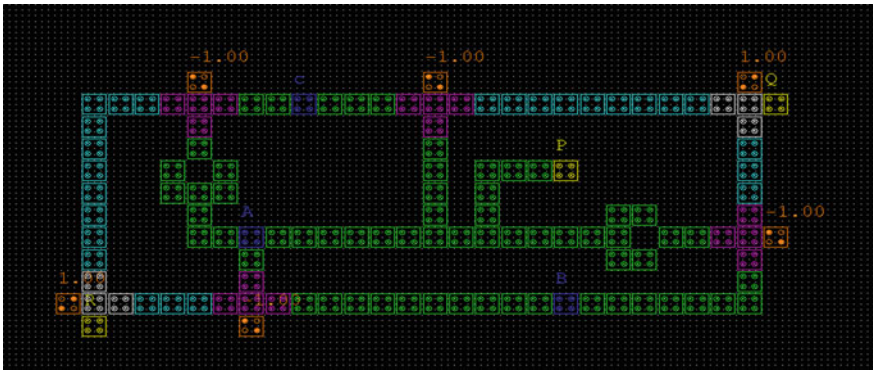

Fig. 12 QCA-based Fredkin gate

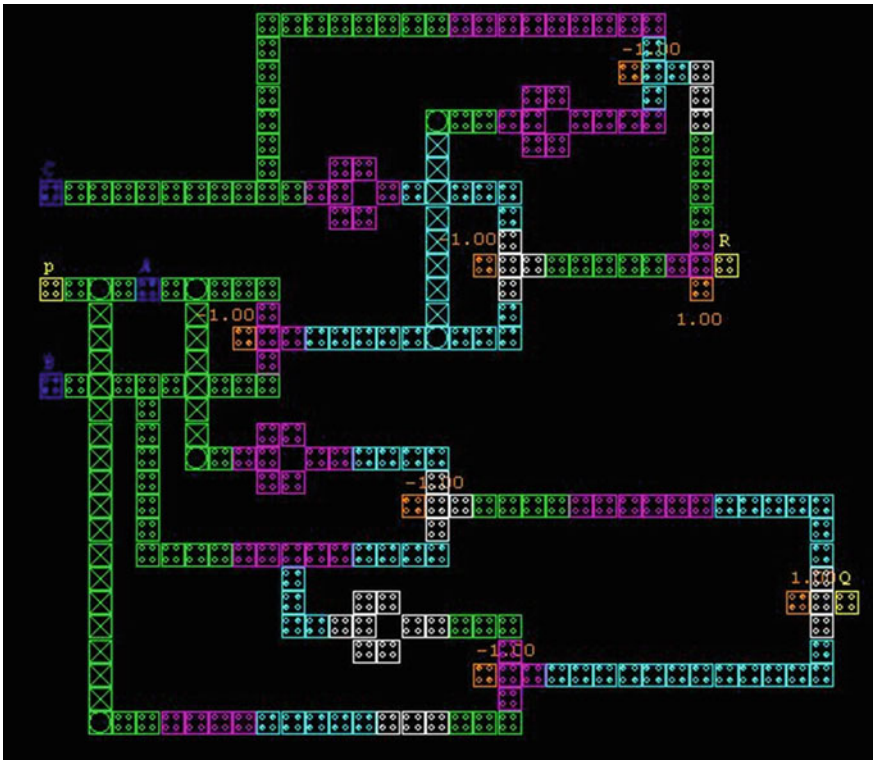

Fig. 13 QCA-based Peres gate

2. Toffoli Gate

The implemented Peres gate consists of two AND gates, two inverters, and one OR gates.

3. Fredkin Gate

The implemented Fredkin gate consists of four AND gates, two inverters, and two OR gates.

4. Peres Gate

The implemented Peres gate consists of five AND gates, four inverters, and two OR gates.

4 Output Waveforms

The results have been analyzed by summing up the graphical result attained from Cadence Virtuoso and QCADesigner V2.0.3 along with the truth table of the reversible logic gates.

4.1 Feynman Gate

See Fig. 14.

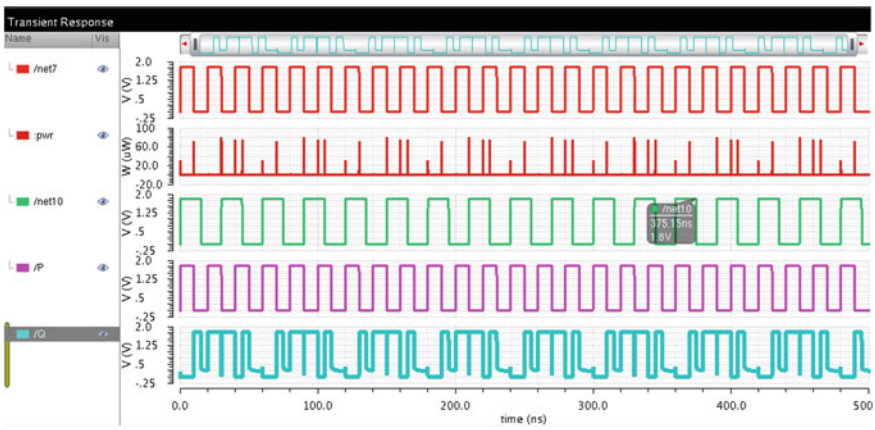

Fig. 14 CMOS output of Feynman gate

4.2 Toffoli Gate

See Fig. 15.

4.3 Fredkin Gate

See Fig. 16.

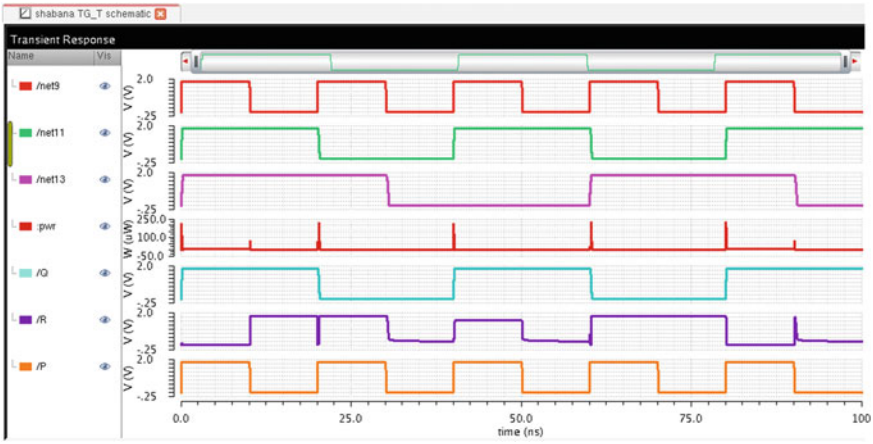

Fig. 15 CMOS output of Toffoli gate

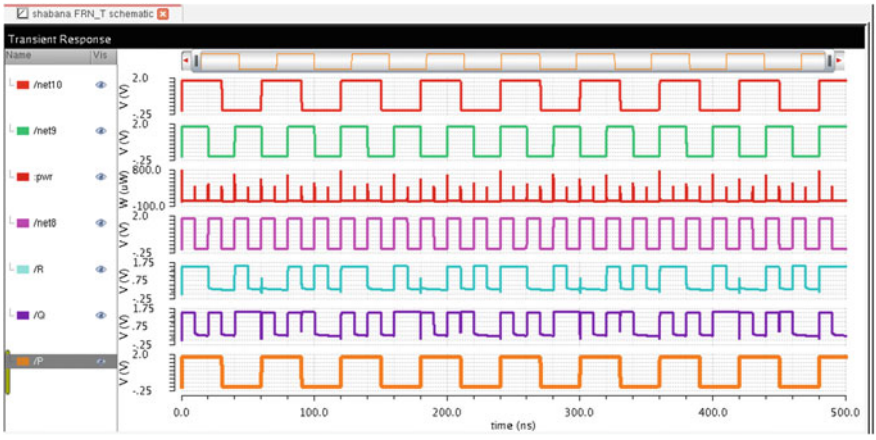

Fig. 16 CMOS output of Fredkin gate

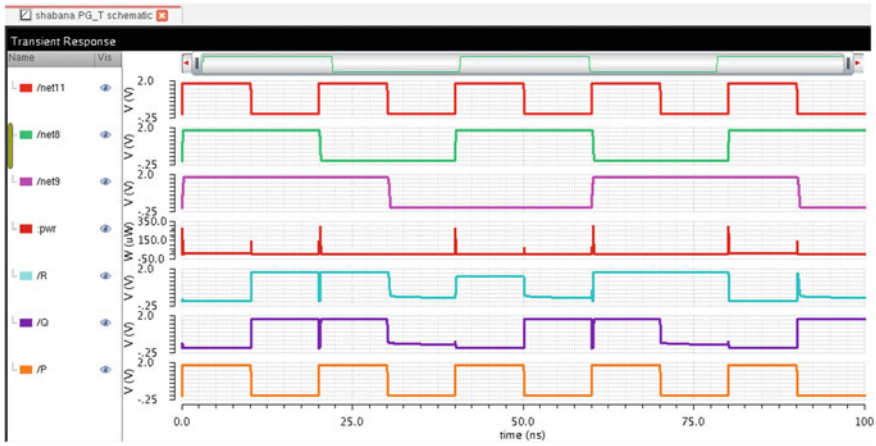

Fig. 17 CMOS output of Peres gate

4.4 Peres Gate

See Fig. 17).

5 Simulation

The four reversible logic gates are implemented and simulated using Cadence Virtuoso and QCADesigner version 2.0.3. The design specifications for reversible gates in QCADesigner for a coherence vector function having cell size must be 18 nm and remaining are as shown below.

6 Conclusion

This paper has explored the fundamental concepts of reversible logic and reversible gates. The simulations are carried using QCA tool and Cadence Virtuoso. Tables 1 and 2 gives design specifications of reversible gates. The regular reversible logic gates have been confirmed on both tools with minimum delay. Using these gates, in future we can design complex architectures as arithmetic logic unit and micro-processors, etc. The current QCA technology does not particularly set the possible operating frequency and definite latency, but it can be analyzed as an imperative parameter in forthcoming works.

Table 1 Design specifications in QCA

	Feynman gate	Toffoli gate	Fredkin gate	Peres gate
Complexity	83	81	121	284
Area	404 μm × 241 μm	458 μm × 426 μm	592 μm × 263 μm	678 μm × 598 μm
Delay (in clock pulse)	1/2	1/2	1/2	No
Clock zones	3	3	3	7

Table 2 Design specifications in 0.09 μm

	Feynman gate	Toffoli gate	Fredkin gate	Peres gate
No. of gates	XOR-1	AND-1 XOR-1	NOT-1 AND-4 XOR-1	AND-1 XOR-2
Power	516.4E-9	2.239E-6	23.13E-6	2.83E-6
Delay	15.17E-9	20.20E-9	10.13E-9	24.57E-12

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