Charge Pump with Improved High-Swing Cascode Current Source for Accurate Current Matching in DPLL

D.S. Rajeshwari, P.V. Rao and V. Rajesh

Abstract In loop dynamics of charge pump phase-locked loop, the charge pump current plays predominate role to loop bandwidth. Different charge pump architectures suffer from charge sharing, clock feed-through, channel charge injection, and current mismatch. Due to this, charge pump phase-locked loop can have more reference spur. Improved high-swing current source is proposed to obtain nearest current matching characteristics. 0.01 % of current mismatch is achieved with 3.3 V, 90 nm CMOS technology. The circuit is verified at process voltage temperature corners.

1 Introduction

Phase-locked loops are the implementations of clock generation for SOC processor. Charge pump-based phase-locked loop (CPPLL) is adequate because of its wide capture range and zero systematic phase offset. In CPPLL, the phase frequency detector (PFD) generates to output pulse UP and DOWN proportional to phase difference of two input pulses ω_{ref} (ω_{in}) and ω_{fb}. Charge pump either charges or discharges according to UP and DOWN. The charge pump current through loop filter generates VCO control output voltage V_{ctrl}. The loop stability ensures locking

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to input ω_{ref}. Thus charge pumps current proportional to vary the lock time and capture time. Any nonidealities in charge pump degrade performance of PLL.

Several single-ended common source charge pump architecture were proposed in the literature [1–2]. Charge sharing effect is greatly minimized using two switches NMOS-Mn and PMOS-Mp. Opamp restricts output range, need good stability by itself, and also the PSSR can reflect largely on PLL spur. Careful design of opamp, inverter delays match, and switch size are required in [1]. The implementation of switch using TG and folded cascode opamp makes careful design, but the TGs have to be scaled up to drive the current mirror, which results in larger Δt_{on} and worsens the reference spur level of CPPLL as charge pump proposed in [3]. Literature [4] exploits rail-to-rail operational amplifier and self-biased high-swing cascode current source to implement charge pump. Since the gain of rail-to-rail opamp varies for input voltage variation across full power supply makes less attraction for charge pump even though stability analysis is obliged. Literature [5] proposed that charge pump circuit uses opamp, cascode reference current source, and charge removal transistor. It backs with supporting any or zero current in cascode current mirror mean startup circuit, which may not turn ON to provide current through current mirror. Proposed charge pump in [2] as gate drain overlap capacitance of NMOSs is not equal to PMOSs, TGs do not avoid clock feed-through effectively. The current mismatch is avoided in literature [2] by deriving charging and discharging of current from the same current reference.

Section 2 covers PLL loop dynamics. Section 3 discusses conventional charge pump nonidealities. Section 4 shows proposed charge pump structure with results. Section 5 draws conclusion from this work.

2 CPPLL Loop Dynamics

CPPLL block diagram is shown in Fig. 1. PFD in loop increases the acquisition range and wide acquisition range. It is necessary because voltage-controlled oscillator (VCO) center frequency can vary considerably with process and temperature.

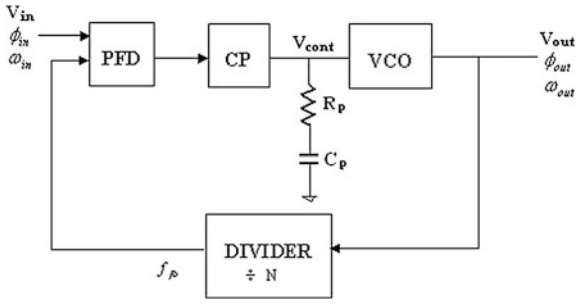


Fig. 1 CPPLL block diagram

The PLL open-loop transfer function [6] including the divider which is equal to

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}}(s)\big|_{\text{open}} = \frac{I_P}{2\pi}\left(R_P + \frac{1}{C_P s}\right).\frac{K_{\text{VCO}}}{s}.\frac{1}{N} \tag{1}$$

The closed-loop transfer function is compared with the standard response of second-order system.

$$H(s) = \frac{\frac{I_P K_{\text{VCO}}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi}\frac{K_{\text{VCO}} R_P s}{N} + \frac{I_P K_{\text{VCO}}}{2\pi C_P N}} = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{2}$$

Thus

$$\omega_n = \sqrt{\frac{I_P K_{\text{VCO}}}{2\pi C_P N}} \tag{3}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{\text{VCO}}}{2\pi N}} \tag{4}$$

ζ is proportional to charge pump current I_{P}, K_{VCO}, and $1/N$. The poles are at zero for $I_P = 0$. For $I_P K_{\text{VCO}} > 0$ which is small, the poles are complex. As $I_P K_{\text{VCO}-} > \infty$ system becomes more stable, the closed-loop system contains zero at $S_Z = -1/(R_P C_P)$. The settling time is inversely proportional to ζ. Thus the design challenges loop bandwidth with charge pump current, VCO gain, and divider factor. Manipulating (3) and (4), the loop filter values are

$$C_P = \sqrt{\frac{I_P K_{\text{VCO}}}{2\pi\omega_n N}} \tag{5}$$

$$R = \frac{2\varsigma}{\omega_n C_P} \tag{6}$$

Depending on the VCO output frequency to be locked, the divider factor is chosen and is given as

$$N = \frac{f_{\text{out}}}{f_{\text{ref}}} \tag{7}$$

The settling time [7] for 2 % tolerance as

$$t_s = \frac{3}{\varsigma\omega_n} \tag{8}$$

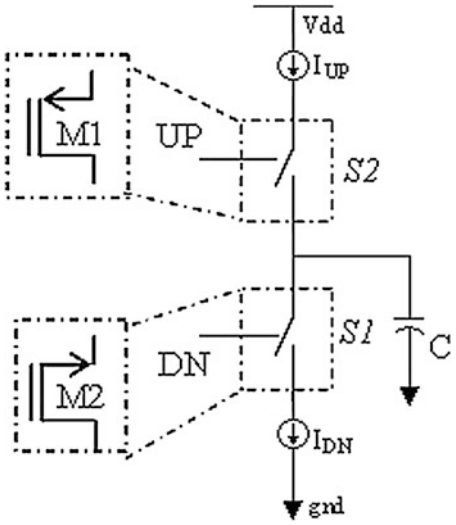


Fig. 2 Block diagram of charge pump

3 Basic Charge Pump Considerations and Its Nonidealities

Block diagram of charge pumps is as shown in Fig. 2. It consists of two switches and two current sources, correspondingly, for UP and DOWN. The switch can be placed at different terminals of current source. The switch S2 charges when switch UP is low, S1 discharges when switch DN is low and the mechanism ensures both switches are OFF as shown in Fig. 3. The MOS switch implementation favors error due to MOS transistor operation when the switch turns OFF/ON.

When MOS switch turns ON to OFF, the total charge in the inversion layer exits through the source and drain terminals. The charge injected on terminals introduces error in the voltage stored in the capacitor. The phenomenon is channel charge injection. Due to rise and fall transition, the output of PFD UP and DOWN pulse signals is coupled to output node via gate to source and gate to drain overlap capacitances. Resulting variation in capacitor voltage refers as clock feed-through. When the MOS switch is OFF, the output capacitor is floating. Later on MOS switch turns OFF to ON state, then charge shares among output capacitance and

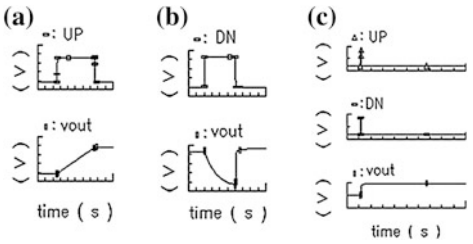
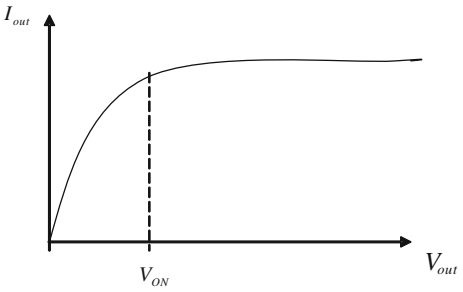


Fig. 3 States **a** Charging **b** Discharging **c** No change

Fig. 4 I_{out} across V_{out}



parasitic capacitance of switch causing deviation output capacitor voltage. Charge sharing, clock feed-through, and channel charge injection contributes gain error, dc offsets, and nonlinearity. The MOS switch errors and MOS implementation determine significant role in reference spur of PLL.

The current sources should be properly biased. The minimum voltage required to obtain constant current in V_{MIN} or V_{ON} is as shown in Fig. 4. The high output impedance minimizes the current variation for V_{DS} variation.

$$V_{\mathrm{DS}}(\mathrm{sat}) = V_{GS} - V_T = V_{\mathrm{ON}} \tag{9}$$

The constant current depends on the value of V_{ON} [6, 8]. Lesser the V_{ON} faster the constant current can be achieved. MOS switch and current source results phase offset due to leakage mismatch $\phi_{\varepsilon,\mathrm{leakage}}$, current mismatch $\phi_{\varepsilon,\mathrm{mismatch}}$, and timing mismatch $\phi_{\varepsilon,\mathrm{timing}}$. The total phase error due to these mismatches

$$\phi_{\varepsilon,\mathrm{tot}} = \phi_{\varepsilon,\mathrm{leakage}} + \phi_{\varepsilon,\mathrm{mismatch}} + \phi_{\varepsilon,\mathrm{timing}} \tag{10}$$

$$\phi_{\varepsilon,\mathrm{tot}} = \frac{2\pi I_{\mathrm{leak}}}{I_{CP}} + 2\pi \frac{\Delta t_{\mathrm{on}}}{T_{\mathrm{REF}}} \frac{\Delta I}{I_{CP}} + 2\pi \frac{\Delta t_{\mathrm{on}}}{T_{\mathrm{REF}}} \frac{\Delta t_d}{I_{CP}} \tag{11}$$

where Δt_{on}, Δt_d, T_{REF}, and ΔI are the turn on time of the PFD, the delay mismatch, the period of reference clock, and current mismatch of the charge pump, respectively.

4 Proposed Charge Pump

The charge pump proposed has an excellent current matching using improved cascode swing current source with a startup circuit. Charge sharing occurs when switch turns ON to OFF state. The charge stored during ON state is provided by definite path. Transistors MSUP2 and MSDN2 takes away stored Charge. These transistors are sized to turn ON fast. The charge pump has self-bias circuit with high output impedance and low turn on voltage to give constant bias voltage.

$$V_{G2} = 2V_{\mathrm{ON}} + V_{\mathrm{TH}}, \quad V_{G4} = V_{\mathrm{ON}} + V_{\mathrm{TH}} \tag{12}$$

$$V_{\mathrm{GS3}} = V_{\mathrm{ON}} + V_{\mathrm{TH}}, \quad V_{\mathrm{GS2}} = V_{\mathrm{ON}} + V_{\mathrm{TH}} \tag{13}$$

$$\begin{aligned} V_{\mathrm{DS5}} = V_{G2} - V_{\mathrm{GS3}} = V_{\mathrm{ON}}, \quad V_{\mathrm{DS3}} = V_{G4} - V_{\mathrm{DS5}} = V_{\mathrm{TH}}, \\ V_{\mathrm{DS4}} = V_{G2} - V_{\mathrm{GS2}} = V_{\mathrm{ON}} \end{aligned} \tag{14}$$

$$V_{\mathrm{DS5}} = V_{\mathrm{DS4}} \tag{15}$$

The size of MN1 and MP1 scaled to provide same V_{ON} as seen from V_X and V_Y correspondingly. The similar structure replicated on P side. The resistor deciding the current based on V_{GS4}–V_{GS5}. Because the cascode structure has high out resistance, the current remains constant for a wide operation range. The current source can provide any current in the circuit, and thus it is been provided by startup circuit that pull the nodes *pb1* and *nb1* toward GND and VDD. The startup circuit time should be less than the width of T_{ON} on locked condition. In a startup circuit, MSP2 will be turned off when *pb1* is equal to or greater than *nst*. Ensured the current source provided with wide operation range, high output resistance, constant current, and low *process voltage temperature* (PVT) sensitivity. The charging current IUP and discharging current IDN are derived from this improved wide swing current reference. The startup current reference and charge pump is shown in Fig. 5. The phase error due to current mismatch is reduced by 0.01 % with current 120 uA constant in tuning voltage 0.4–2.8 V. The charge sharing occurs due to load capacitance when switch turns OFF to ON. The CP structure has switch away from V_{cntrl}. Correspondingly, once the switches turns ON to OFF the switches MSUP2 and MSDN2 turns ON. The phase error due to timing mismatch is possible only with proper sizing of the inverters. The charge pump currents IUP and IDN over

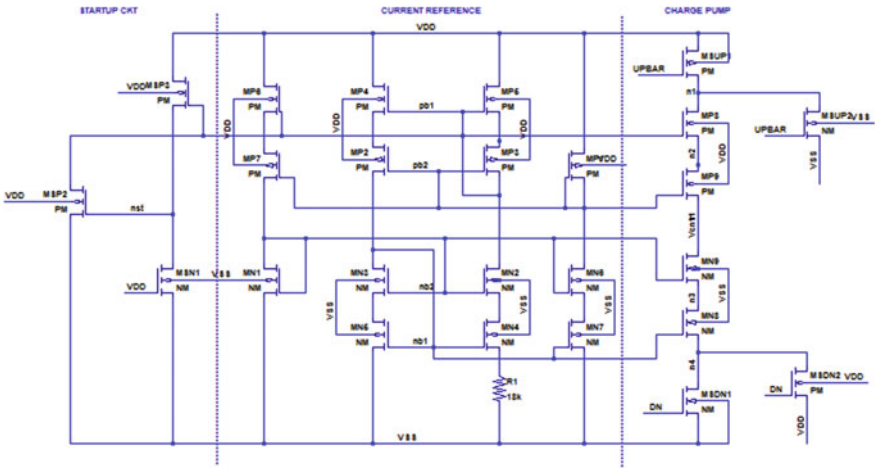


Fig. 5 Improved high-swing current reference-based charge pump with startup circuit

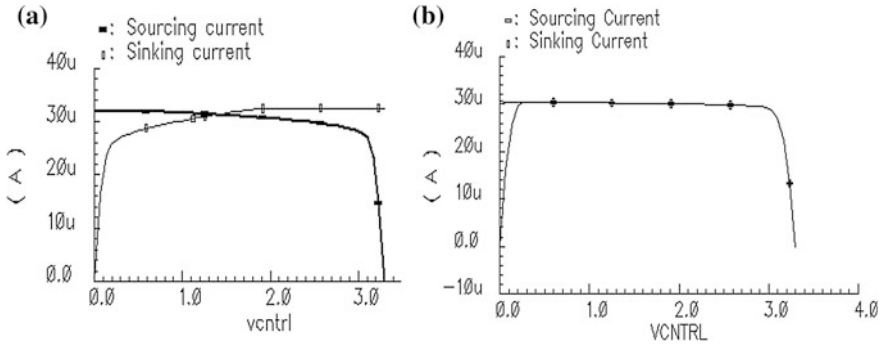


Fig. 6 Charge pump current matching characteristics A. V_{cntrl} versus Charge pump sourcing and sinking current B. current matching characteristics of proposed high-swing cascode CP

power supply 0–3.3 V are plotted comparing with conventional charge pump as shown in Fig. 6. From the proposed improved charge pump with improved high-swing cascode current source obtains nearest 0.01 % of current mismatch is achieved with 3.3 V, CMOS 90 nm *technology* [9, 10].

5 Layout Design and Simulation Results

CPLL consists of Digital blocks as PFD, Divider, and analog blocks as VCO. The placement is taken care to avoid ground bounce and supply bounce effects. The symmetry routing is provided in PFD so that it has minimum dead zone due to PFD and CP performance in loop. In layout of charge pump, symmetry affects the performance of CP. The proposed structure provides better matching in terms of layout performance. The entire transistors unit sized to the other on both N and P side. The structure makes routing very simple. The inter-digitization matching techniques are used to do current matching in cascode structure.

The output results of VCO are shown in Fig. 7. The VCO output signal ranges 1.65–3.1 V [11, 12]. The design is simulated for temperature range −40° to 125°.

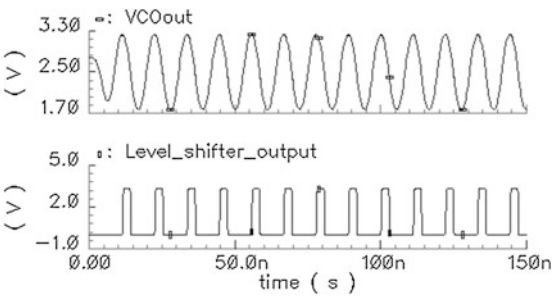


Fig. 7 VCO waveforms, before and after Level shifter (*V*ctrl = 1.65 V)

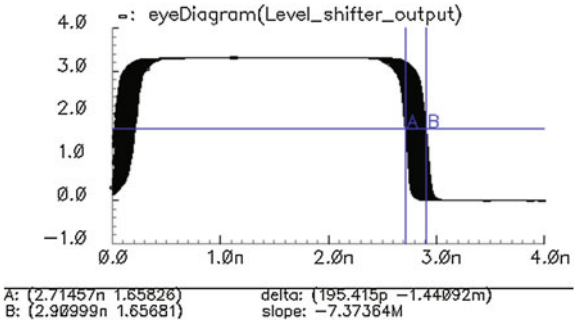


Fig. 8 VCO jitter calculation using "eye diagram" function in Cadence tool. Peak jitter = 195 ps at 85 MHz (Vctrl = 1.65 V)

The VCO output ranges to supply rails 0–3.3 V. The peak jitter is measured as shown in Fig. 8. The third-order CPPLL is simulated with proposed new architecture results as shown in Fig. 9. In Fig. 9, the waveform VCTR can be observed charging and discharging and settle down once it locks to reference input frequency. The loop parameters are modeled using octave to observe the stability. The V_{cntrl} (VCTR) plot can be observed to see verge of critically damped.

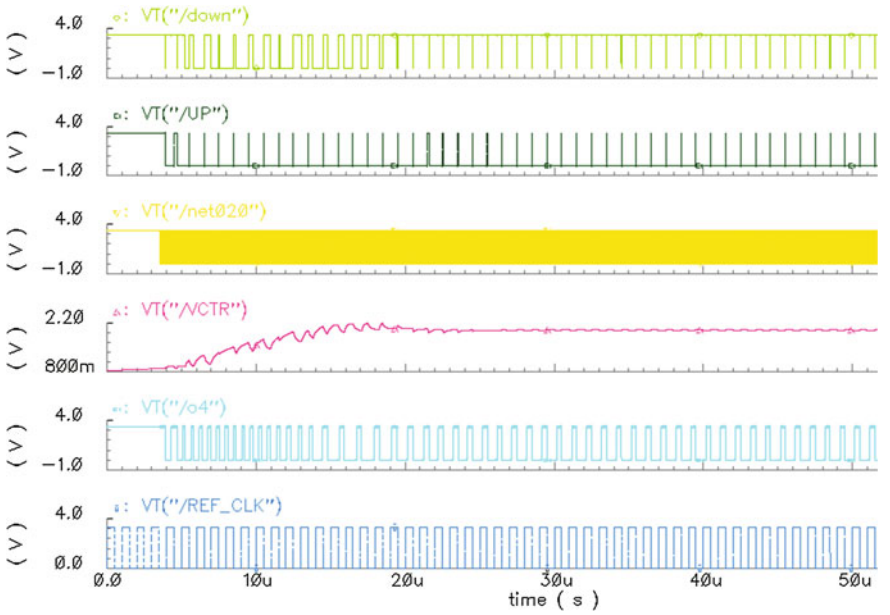


Fig. 9 Charge pump PLL Simulation results

6 Conclusion

The charge pump with improved high-swing cascode current source for accurate current matching is designed and analyzed using tsmc 90 nm technology. The proposed charge pump architecture provides 0.01 % current matching and provides stable current for voltage range 0–3.63. The dependence of ζ on loop parameters charge pump current I_{CP}, VCO Gain K_{VCO}, divider factor N, and it effects on settling time, lockin range, and loop bandwidth is discussed. Feature implementation can make programmable charge pump, so that the current source can be shutdown to avoid power consumption.

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