Chapter 3
Physical Mechanism of BTI Degradation—Direct Estimation of Trap Generation and Trapping

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Abstract In this chapter, direct characterization techniques have been used to access the trap generation and trapping subcomponents of BTI degradation in HKMG MOSFETs having different gate stack processes. Generation of new traps is estimated using DCIV for NBTI stress and both DCIV and SILC for PBTI stress respectively in p- and n-channel MOSFETs. Flicker noise is used to estimate the density of process related pre-existing gate insulator traps responsible for hole and electron trapping respectively during NBTI and PBTI stress. The spatial and energetic locations of generated traps for NBTI and PBTI stress are identified. The time, bias, and temperature dependencies of trap generation obtained using the DCIV technique are compared between NBTI and PBTI stress, while these parameters obtained using DCIV and SILC techniques are compared for PBTI stress. The relative dominance of trap generation and trapping on NBTI and PBTI threshold voltage degradation is estimated for different gate insulator processes.

3.1 Introduction

From a practical point of view of technology qualification, it is important to know the magnitude of Bias Temperature Instability (BTI) at end-of-life of devices and hence of circuits and products under normal use condition. Estimation of Negative BTI (NBTI) and Positive BTI (PBTI) respectively in p- and n-channel Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is usually done by stressing the devices at higher than normal gate bias ($V_G = V_{G\text{-STR}}$) and measuring the resulting device parametric degradation with minimal impact of recovery artifacts. Different "recovery-free" measurement techniques have been discussed in Chap. 2. As mentioned before, stress tests are usually performed for few hours or

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days in wafer level setup, although sometimes the test can go on for few months in package level setup. Measured data at short time and at accelerated aging condition are then extrapolated to end-of-life and normal operating condition by using suitable models. Proper understanding of BTI degradation mechanism is necessary to develop reliable extrapolation models. It also helps in understanding the impact of gate insulator processes on BTI, which in turn helps in process optimization for keeping BTI under acceptable limits for technology qualification.

The physical mechanism of BTI has remained as a topic of great debate. It was discussed in Chap. 1 that NBTI has emerged as a crucial p-MOSFET reliability issue since 90 nm technology node, when Silicon Oxynitride (SiON) replaced Silicon Dioxide (SiO_2) as the gate insulator [1, 2]. NBTI remains as an important issue even today for planar MOSFETs and FinFETs having state-of-the-art High-K Metal Gate (HKMG) gate stacks [3, 4]. Over the years, different physical mechanisms have been proposed to explain buildup of positive charges in the gate insulator during NBTI stress and were recently reviewed [5]. Figure 3.1 shows schematic of p- and n-channel HKMG MOSFETs having bi-layer gate insulator stack with SiO_2 or SiON Interlayer (IL) and Hafnium Oxide (HfO_2) High-K dielectrics. Positive charge buildup during NBTI stress can be due to either one or both of the two processes, i.e., generation of new traps at or near the interface between Silicon (Si) channel and SiO_2 (or SiON) IL and/or charging of pre-existing, as-processed traps in IL bulk. It is believed that HfO_2 High-K layer presumably acts primarily as a voltage divider.

Different characterization techniques have been discussed in Chap. 2 for accessing the density of process related and generated traps respectively before and after BTI stress. Note that direct characterization techniques such as Charge Pumping (CP) [6] and Gated Diode (or DCIV) [7] have been used in several reports to provide irrefutable proof of interface trap generation (ΔN_{IT}) for NBTI stress in SiON [5, 7–15] and HKMG [5, 16–18] p-MOSFETs. In spite of these experimental evidences, some reports have suggested hole trapping in pre-existing traps (ΔN_{HT}) as the only NBTI mechanism [19–23], which is definitely not correct. Similarly, reports suggesting ΔN_{IT} as the exclusive NBTI mechanism [10, 11] are also not correct, as they cannot explain ultra-fast threshold voltage shift (ΔV_T) measurements [20, 24, 25] and gate insulator process dependence of NBTI [13–15]. As of

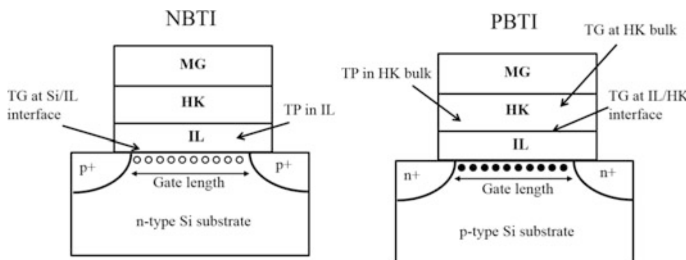

Fig. 3.1 Schematic of p- and n-channel HKMG MOSFETs showing different trap generation (TG) and trapping (TP) processes under NBTI and PBTI stress

today, the prevailing notion of NBTI mechanism involves contribution from both ΔN_{IT} and ΔN_{HT}; although some have suggested strong coupling or correlation between the two processes [26], most reports suggest that they are independent and mutually uncorrelated [5, 9, 13–18, 27–35]. Furthermore, trap generation (ΔN_{OT}) in bulk IL also contributes for situations involving high stress gate bias ($V_{G\text{-}STR}$). Mutually uncoupled ΔN_{IT} and ΔN_{HT} (and also ΔN_{OT} for certain situations) mechanisms can explain different gate insulator process dependent NBTI data [5, 33–35], and is discussed later in Chap. 4.

As discussed in Chap. 1, PBTI remained negligible for SiON n-MOSFETs and became important with the introduction of HKMG technology [36]. As mentioned before, NBTI in HKMG MOSFETs results in positive charge buildup in the SiO_2 or SiON IL due to trap generation at Si/IL interface and hole trapping in IL bulk [16, 17, 34]. In contrast, PBTI results in negative charge buildup in HfO_2 High-K layer as shown in Fig. 3.1 [36]. Note that initial HKMG MOSFETs had thick and not fully optimized HfO_2 High-K layer and showed very large PBTI degradation primarily due to significant electron trapping in pre-existing traps (ΔN_{ET}) [37, 38]. However, PBTI magnitude reduces with reduction in High-K layer thickness [36] and with optimization of HKMG process [39] as mentioned in Chap. 1. For well-optimized gate insulator stacks, various reports have suggested trap generation in the High-K layer measured directly using DCIV [16, 17, 40] and Stress Induced Leakage Current (SILC) [40, 41] methods. Moreover, a recent report has suggested two different and mutually uncoupled PBTI trap generation processes, presumably at the IL/High-K interface ($\Delta N_{IT\text{-}HK}$) and High-K bulk ($\Delta N_{OT\text{-}HK}$), respectively, probed by DCIV and SILC techniques [17]. In spite of such direct experimental evidences of trap generation, some report still suggests PBTI to be solely due to electron trapping in pre-existing process related traps in the High-K layer even for state-of-the-art technology nodes [42], which is obviously not correct. However, many reports have suggested mutually uncorrelated trap generation and trapping in High-K as the physical mechanism of PBTI [16, 17, 32, 40, 43]. PBTI model is discussed later in Chap. 4.

Furthermore, transconductance degradation (Δg_m) has been reported for NBTI stress in HKMG p-MOSFETs since generated IL charges are closer to the channel and results in mobility degradation due to Coulomb scattering. However, Δg_m is negligible for PBTI stress in well-optimized HKMG n-MOSFETs due to negligible IL degradation [39], refer to Chap. 1 for details. While the magnitude of PBTI degradation reduces with HfO_2 thickness scaling, it increases with reduction in IL thickness since generated High-K layer charges come closer to the channel, and also due to possible modification of the High-K layer quality introduced by the IL thickness scaling process [17, 32, 44, 45]. Therefore, NBTI and PBTI charges are shown to have very different physical location in the HKMG gate stack.

As mentioned in Chap. 1, the relative magnitude of NBTI and PBTI degradation respectively in p- and n-channel HKMG MOSFETs stressed under identical oxide field (E_{OX}) and temperature (T) depends on the gate insulator process and is industry specific [3, 4]. Although NBTI results in trap generation and trapping in the IL layer while PBTI degrades the High-K layer, they demonstrate very similar behavior listed

as follows, when measured by using Ultra-Fast Measure-Stress-Measure (UF-MSM) technique, refer to Chap. 1 for details:

(a) Time evolution of ΔV_T shows rapid increase at the beginning of stress and power-law time dependence with time exponent n for longer stress time. The longer time power-law dependence is observed for both DC and AC stress, refer to Figs. 1.25 and 1.30.
(b) The longer time power-law time exponent n is independent of stress E_{OX} and T when stress and measurements are performed without any extraneous artifacts, such as influence of recovery or stress saturation, and shows similar values for NBTI and PBTI stress. The exponent is also independent of AC pulse duty cycle (PDC) and frequency (f), although n for AC stress is higher compared to DC stress. Refer to Figs. 1.26 and 1.31.
(c) Measured ΔV_T increases with stress E_{OX} and T. The power-law E_{OX} acceleration factor (Γ_E) and Arrhenius T activation energy (E_A) extracted using ΔV_T measured at fixed stress time (t_{STR}) are found to be independent of stress T and E_{OX} respectively, when stress and measurements remain free from certain extraneous artifacts mentioned above, refer to Fig. 1.27.
(d) BTI recovery results in lower ΔV_T for AC when compared to DC stress. AC ΔV_T is independent of f, and shows a typical "S" shaped characteristic with variation in PDC, with a large "kink" or "jump" in ΔV_T observed between high PDC AC and DC stress, refer to Fig. 1.32.
(e) Although the magnitude of ΔV_T increases for NBTI but reduces for PBTI when Nitrogen (N) is incorporated in the gate insulator stack, the parameters n, E_A and Γ_E show a reduction for both NBTI and PBTI stress, refer to Fig. 1.34.
(f) Equivalent Oxide Thickness (EOT) scaling achieved either by reduction in IL thickness or post High-K nitridation results in higher ΔV_T but reduction in parameters n, E_A and Γ_E, refer to Fig. 1.35.

In this chapter, the underlying trap generation and trapping subcomponents of NBTI and PBTI degradation are independently assessed respectively in p- and n-channel HKMG MOSFETs. Devices having different HKMG gate insulator processes are used. The contribution of trap generation and trapping on ΔV_T measured using ultra-fast MSM method is also assessed to determine physical mechanism of BTI degradation. The concept developed in this chapter will be used in Chap. 4 to develop quantitative NBTI and PBTI models.

3.2 Description of HKMG Devices

Figure 3.2 shows the gate insulator process flow of different HKMG MOSFETs studied in this chapter. A Gate First integration scheme has been used.

The devices have different Rapid Thermal Process (RTP) based thermal IL layers [46] but identical HfO_2 High-K layer obtained using the Atomic Layer Deposition (ALD) method [47]. Different pre-clean surface treatments have been

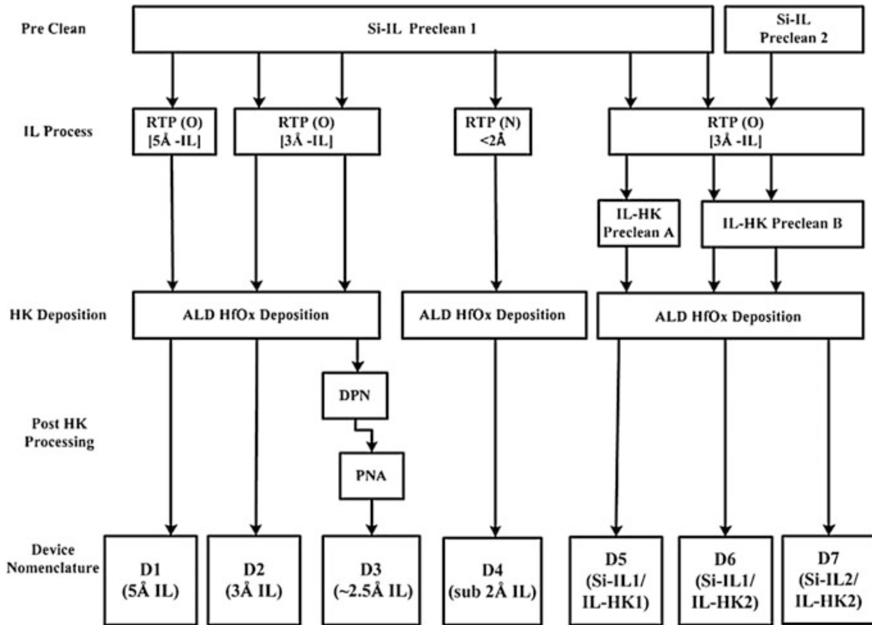

Fig. 3.2 Schematic process flow of different HKMG gate insulators studied in this chapter

used before thermal IL growth and before ALD High-K deposition. The Si/IL pre-clean is done before the IL growth and therefore affect the IL quality, and for thinner IL, it can also affect the High-K quality. The IL/HK pre-clean is done after IL growth but before High-K deposition, and impacts the High-K layer quality. EOT scaling has been achieved (a) by using RTP based thermal IL having thickness of 5 Å (D1) and 3 Å (D2), (b) by introducing Nitrogen (N) in the gate stack after High-K deposition, using Decoupled Plasma Nitridation (DPN) [48] with proper Post Nitridation Anneal (PNA) [49] (D3) and (c) by using N based surface passivation before RTP IL growth (D4). Devices D1 through D4 have identical Si/IL and IL/HK pre-clean processes, different IL but identical High-K thickness. Devices D5 through D7 have identical IL and High-K layer thickness, however, D5 and D6 have similar Si/IL but different IL/HK pre-clean processes, while D6 and D7 have different Si/IL but similar IL/HK pre-clean processes. All thicknesses are measured using X-ray Photoelectron Spectroscopy; refer to [32] for further details.

3.3 Trap Generation During NBTI

In this section, trap generation during NBTI stress in HKMG p-MOSFETs is studied using the Gated Diode or DCIV technique [7], which has been discussed in detail in Chap. 2. In this technique, the source and drain terminals of a MOSFET are

shorted together and forward biased below the junction cut-in voltage, the gate is swept from accumulation to inversion, and the current due to electron-hole recombination in traps at and near the Si channel and gate insulator interface is measured at the substrate. DCIV current (I_{DCIV}) is proportional to the density of these traps, and therefore, increase in I_{DCIV} after NBTI stress is a direct measure of generation of new traps. In HKMG MOSFETs, DCIV can measure trap generation at Si/IL interface, IL bulk, as well as at IL/High-K interface especially for gate stacks having thin IL layers, refer to Fig. 3.1. However, it is unlikely that DCIV would probe much deeper inside High-K bulk. Therefore, in addition to generated traps associated with NBTI, DCIV technique can also measure generated traps in the IL due to Time Dependent Dielectric Breakdown (TDDB) process as both mechanisms get triggered at identical stress conditions, refer to Chap. 1, Fig. 1.2. However, as discussed in Chaps. 2 and 4, TDDB has much larger V_G acceleration factor compared to NBTI [15], and for HKMG MOSFETs, the stress V_G gets divided between the IL and High-K layers. Therefore, for moderate values of stress V_G, trap generation in HKMG devices measured by DCIV can be largely associated to the NBTI process.

Furthermore, DCIV is a slow measurement technique and it takes approximately few seconds to perform the V_G sweep and measure I_{DCIV} using conventional instrumentation. Note that DCIV characterization is performed in MSM mode, where measurements are performed before and during logarithmically spaced intervals of NBTI stress. Since generated traps start to reduce when NBTI stress is stopped for measurement, measured DCIV data get corrupted by recovery artifacts and therefore needs to be corrected for measurement delay, as discussed in Chap. 2. Finally, note that DCIV scans trap generation located energetically in $\sim$0.3 eV around the Si band gap [7]. Since ΔV_T gets affected by trap generation in the entire band gap, measured DCIV data must also be corrected for such band gap difference before compared to ΔV_T obtained from *I–V* measurements. DCIV data in this and following sections are plotted after correction for measurement delay and band gap difference using the procedure discussed in Chap. 2 [17].

3.3.1 DCIV Measurements in DC Stress

Figure 3.3 plots time evolution of generated interface traps (ΔN_{IT}) in HKMG p-MOSFETs having (a) non-nitrided (D2) and (b) N surface passivated (D4) IL for NBTI stress at different $V_{G\text{-}STR}$ and T. As mentioned before, ΔN_{IT} is extracted from DCIV measurements after delay and band gap correction. Only longer time data are plotted, and ΔN_{IT} increases with increase in $V_{G\text{-}STR}$ and T as expected, and the nitrided device D4 shows slightly higher degradation compared to its non-nitrided counterpart due to larger stress E_{OX} and different IL quality. Note that E_{OX} is calculated using $(V_{G\text{-}STR} - V_{T0})$/EOT; where V_{T0} is pre-stress V_T and EOT is the SiO_2 equivalent gate insulator thickness. The time evolution of ΔN_{IT} shows power-law dependence with identical time exponent ($n \sim 1/6$) for both devices and

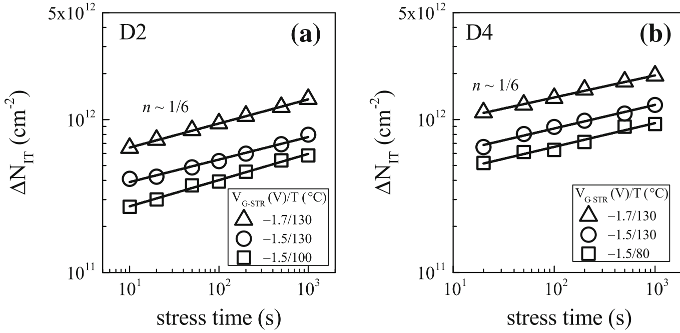

Fig. 3.3 DCIV measured time evolution of ΔN_{IT} for NBTI stress at different $V_{G\text{-}STR}$ and T in HKMG p-MOSFETs having different IL processes

for different $V_{G\text{-}STR}$ and T. The exponent n is extracted by linear regression of measured ΔN_{IT} time evolution data in t_{STR} range of 10 s to 1 Ks. Interestingly, the HKMG process dependence of time exponent n for ΔN_{IT} is different from that for ΔV_T shown earlier in Chap. 1, Figs. 1.25, 1.33 and 1.35. Note that although ΔV_T shows power-law time dependence with exponent n that is independent of $V_{G\text{-}STR}$ and T for a particular HKMG process, its value reduces for nitrided devices unlike that shown here for ΔN_{IT} data. Moreover, the value of n for ΔN_{IT} is always higher than that for ΔV_T when extracted in the same range of t_{STR} as shown.

As a further proof of the universality of power-law time exponent n, time evolution of ΔN_{IT} is measured using DCIV method in different HKMG devices shown in Fig. 3.2. Figure 3.4 plots extracted n versus (a) $V_{G\text{-}STR}$ and (b) T after correction for measurement delay. Note that within measurement error, a universal power-law time dependence with $n \sim 1/6$ is obtained for devices having different HKMG gate insulator processes and also across different $V_{G\text{-}STR}$ and T. Once again, while a universal exponent is obtained for time evolution of ΔN_{IT}, this is in contrast

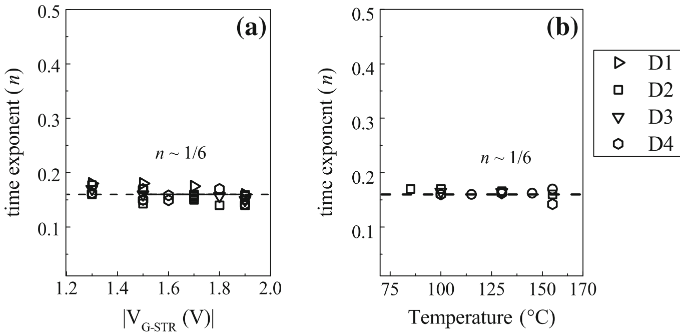

Fig. 3.4 Extracted long-time power-law time exponent n for different HKMG devices as a function of **a** stress V_G and **b** stress T, obtained using DCIV measurements during NBTI stress

to the exponent obtained for time evolution of ΔV_T from UF-MSM technique; the latter has strong gate insulator process dependence as discussed in Chap. 1, Sect. 1.6. This universality of ΔN_{IT} time evolution is a very significant result and underlines the robustness of physical mechanism governing interface trap generation, which will be discussed later in this book.

Figure 3.5 plots (a) stress E_{OX} and (b) stress T dependence of ΔN_{IT} at fixed t_{STR}, obtained from DCIV measurements after delay and band gap corrections. Experiments have been performed at three sets of stress T, and for each T, three different values of E_{OX} have been used. This facilitates extraction of power-law E_{OX} acceleration factor Γ_E and Arrhenius T activation energy E_A of ΔN_{IT} at different T and E_{OX}, respectively. Since ΔN_{IT} time evolution has power-law dependence with similar n for different stress E_{OX} and T as shown above, extracted Γ_E and E_A would be independent of t_{STR}. It is interesting to note that similar to E_{OX} and T dependence of ΔV_T shown in Chap. 1, Fig. 1.27, measured values of Γ_E and E_A from E_{OX} and T dependence of ΔN_{IT} are also independent of T and E_{OX}, respectively. Note that mutually independent E_{OX} and T dependencies are obtained when stress and measurement remain free from extraneous artifacts mentioned in Chap. 1, Sect. 1.3.

Figure 3.6 shows the impact of IL thickness on (a) power-law field acceleration factor Γ_E and (b) Arrhenius T activation energy E_A extracted from DCIV measured ΔN_{IT} data after delay and band gap correction, for NBTI stress in different HKMG devices shown in Fig. 3.2. As discussed before, IL thickness scaling is achieved by using different RTP based thermal IL (D1, D2), post High-K nitridation (D3), and RTP based IL on N passivated Si substrate (D4). Both Γ_E and E_A reduce with EOT scaling as shown, which is similar to EOT dependence of Γ_E and E_A for ΔV_T shown in Fig. 1.35. For a particular device, the magnitude of Γ_E for ΔN_{IT} is similar to that

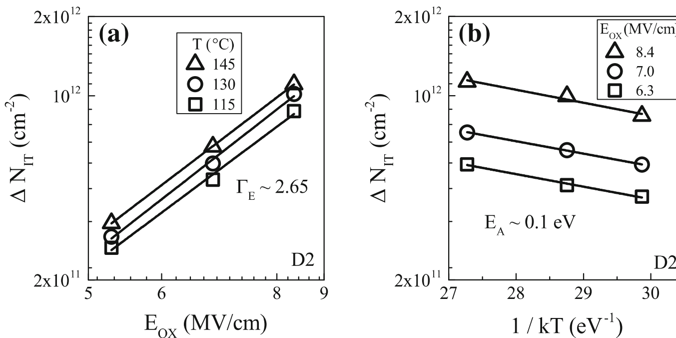

Fig. 3.5 Fixed time DCIV measured ΔN_{IT} versus **a** stress E_{OX} and **b** stress T for NBTI stress in HKMG p-MOSFETs. E_{OX} dependence is shown for different T and T dependence shown for different E_{OX}. E_{OX} dependence is plotted in a log–log scale and T dependence is plotted in a semi-log scale

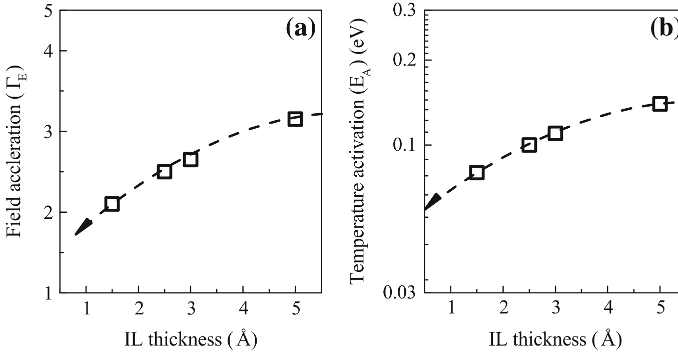

Fig. 3.6 Power-law field acceleration factor (Γ_E) and Arrhenius T activation energy (E_A) of DCIV measured ΔN_{IT} for NBTI stress, as a function of IL thickness of different HKMG stacks

for ΔV_T, while E_A for ΔN_{IT} is always higher compared to the corresponding value for ΔV_T. This aspect is discussed later in this chapter and also in Chap. 4.

3.3.2 DCIV Measurements in AC Stress

Similar to DC stress, DCIV assessment of trap generation during AC NBTI stress is also done in MSM mode, where measurements are performed before and during logarithmically spaced interruptions of stress. Figure 3.7 plots time evolution of ΔN_{IT} during AC stress at different (a) PDC and (b) f but identical stress E_{OX} and T, obtained from DCIV measurements after delay and band gap corrections.

Only the long t_{STR} data are plotted, and the corresponding DC data are also shown. Note that DC stress bias and AC stress pulses have been applied for identical t_{STR} duration, and therefore the actual duration of AC stress, i.e., the pulse on time would depend on PDC of the applied AC pulse. ΔN_{IT} time evolution shows power-law dependence at longer t_{STR} for both DC and AC stress, and the exponent n extracted in t_{STR} range of 10 s to 1 Ks is also plotted in Fig. 3.7 as a function of (c) PDC and (d) f of the gate pulse; DC value is shown as reference (100 % PDC). Identical n ($\sim$1/6) is observed for DC and AC stress at different PDC and f. Note that identical n of ΔN_{IT} time evolution for DC and AC stress is in contrast to that observed for time evolution of ΔV_T, measured using the UF-MSM technique and shown in Chap. 1, Fig. 1.31; ΔV_T shows lower n for DC compared to AC stress. Moreover when extracted in same t_{STR} range, ΔN_{IT} shows higher n compared to ΔV_T for DC stress, however, both ΔN_{IT} and ΔV_T show identical n ($\sim$1/6) for AC stress. Once again, the universality of $n \sim 1/6$ for ΔN_{IT} time evolution during DC and AC stress suggest the robustness of the underlying physical mechanism of interface trap generation and is discussed in Chap. 5.

Figure 3.7 also plots measured ΔN_{IT} at fixed t_{STR} for AC NBTI stress as a function of (e) PDC and (f) f, the PDC dependence is measured using AC pulses

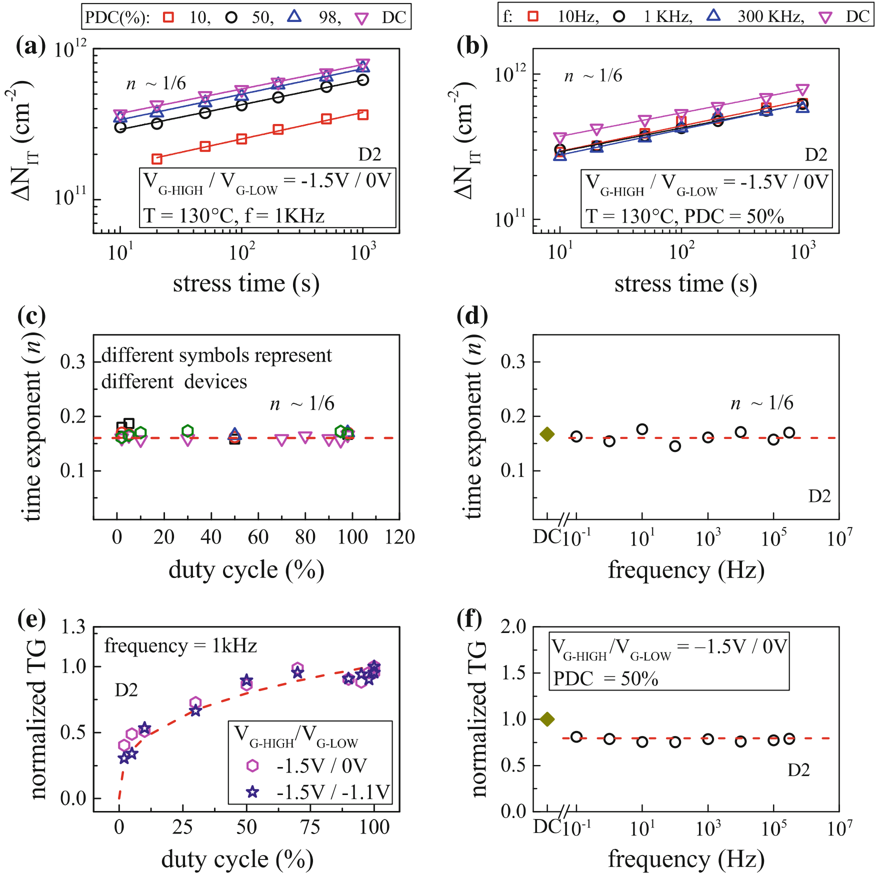

Fig. 3.7 DCIV measured time evolution of ΔN_{IT} for AC NBTI stress at different **a** PDC and **b** frequency; the PDC and f values used in panel **a** and **b** respectively are mentioned at the *top*. Measured long-time power-law time exponent n as a function of **c** PDC for different devices and **d** frequency. Fixed time measured ΔN_{IT} versus **e** PDC for different $V_{G\text{-}LOW}$ and **f** frequency

having identical pulse high but different pulse low values. AC data are normalized to the corresponding DC value at identical t_{STR}. Note that ΔN_{IT} magnitude increases with increase in PDC, but remains independent of the pulse low value and f. Although f independence of ΔN_{IT} is qualitatively similar to that observed for ΔV_T as shown in Chap. 1, Fig. 1.32, ΔN_{IT} and ΔV_T have very different AC to DC ratio. On the other hand, the PDC dependence of ΔN_{IT} is both qualitatively and quantitatively different from the PDC dependence of ΔV_T. Note, ΔN_{IT} does not show the “S” shaped PDC dependence as in ΔV_T, and moreover, no “kink” or “jump” is seen for ΔN_{IT} data between high PDC AC and DC stress. Furthermore, not only ΔN_{IT} has very different AC to DC ratio compared to ΔV_T as mentioned above, unlike ΔV_T, the AC to DC ratio for ΔN_{IT} does not depend on the pulse low value. Time evolution of ΔN_{IT} and ΔV_T for AC stress will be explained later in this book.

3.4 Hole Trapping During NBTI

As discussed earlier in this chapter, although interface trap generation plays a crucial role, it alone cannot explain UF-MSM measured ΔV_T during NBTI stress. As an evidence of additional contribution from the hole-trapping component, Fig. 3.8 plots time evolution of measured ΔV_T and ΔV_{IT} (=q/C_{OX} * ΔN_{IT}) obtained using UF-MSM and DCIV techniques, respectively. Experiments were performed on HKMG p-MOSFETs having (a) non-nitrided (D2) and (b) N surface passivated (D4) IL, refer to Fig. 3.2; C_{OX} is gate insulator capacitance and q is electronic charge. Identical stress E_{OX} and T have been used for both devices, and experimental DCIV data were corrected for measurement delay and band gap differences as mentioned earlier. Since ΔV_{IT} signifies the component of ΔV_T that is contributed by generated interface traps (ΔN_{IT}), the difference between ΔV_T and ΔV_{IT} signifies contribution due to hole trapping in pre-existing traps, ΔV_{HT} (=q/C_{OX} * ΔN_{HT}). Time evolution of ΔV_{HT} is also plotted in Fig. 3.8. Only longer t_{STR} data are shown.

Time evolution of ΔV_{IT} has power-law dependence with exponent $n \sim 1/6$ as discussed above, while ΔV_{HT} saturates at longer t_{STR} as shown. Therefore, time evolution of ΔV_T (=ΔV_{IT} + ΔV_{HT}) shows power-law dependence with lower n compared to that for ΔV_{IT}. This explains the reason behind lower time exponent n observed for ΔV_T compared to ΔN_{IT} data across different $V_{G\text{-}STR}$ and T as mentioned before. Although the ΔV_{IT} contribution increases slightly for the N containing device D4 compared to the non-nitrided device D2, a significantly large increase is observed for the ΔV_{HT} component. Therefore, ΔV_T magnitude increases while time exponent n reduces for the D4 device as shown. Figure 3.8 clearly indicates that the underlying ΔN_{IT} and ΔN_{HT} components of NBTI are uncorrelated; a relatively larger increase in ΔN_{HT} is observed for the D4 device having N in

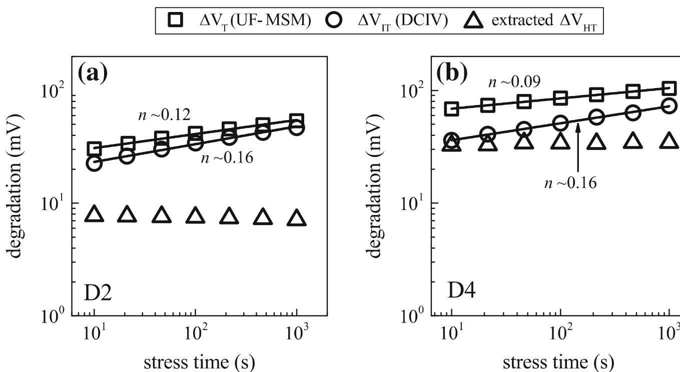

Fig. 3.8 Time evolution of UF-MSM measured ΔV_T and DCIV measured ΔN_{IT} contribution after measurement delay and band gap correction (ΔV_{IT}), for NBTI stress in HKMG p-MOSFETs having different IL processes. Extracted difference (ΔV_{HT}) is also shown

the gate stack, which can explain the measured reduction in the time exponent n. However, ΔV_{IT} component dominates ΔV_T for both devices as shown.

As a further proof, Fig. 3.9a shows the correlation of measured ΔV_T and ΔV_{IT} for HKMG devices D2 and D4. As mentioned before, ΔV_T is obtained using UF-MSM and ΔV_{IT} using DCIV after delay and band gap correction. The 1:1 correlation line is also shown, which signifies zero hole-trapping contribution. Note that for a particular ΔV_{IT}, D2 device shows slightly higher ΔV_T than the 1:1 correlation line, while a somewhat larger ΔV_T is observed for device D4, which is consistent with relatively larger ΔN_{HT} contribution for device D4 having N in the gate insulator stack. Larger magnitude of hole trapping during NBTI stress in gate insulators containing N is a well-known result and reported by various groups [13–15, 50].

Hole trapping occurs in pre-existing, process related gate insulator traps, and as mentioned in Chap. 2, flicker noise technique can be used to access the density of these traps. In flicker noise method, the gate of the MOSFET is biased in weak inversion and the power spectral density of drain current noise (S_{ID}) is measured using a spectrum analyzer. The inversion layer carrier density in the channel remains low in weak inversion, and drain current noise arises due to trapping and detrapping of carriers in gate insulator traps. Higher trap density results in larger S_{ID} and vice versa. Figure 3.9b shows measured pre-existing trap density in devices D2 and D4. Note that the nitrided device D4 shows higher trap density, which is consistent with higher ΔN_{HT} contribution shown in Figs. 3.8 and 3.9a. The impact of N on pre-existing hole traps has been studied in detail in SiON [50] and HKMG [51] p-MOSFETs and also verified by Density Functional Theory (DFT) calculations as discussed in detail in [17, 51].

Time evolution of ΔV_T and ΔN_{IT} during NBTI stress has been measured respectively using UF-MSM and DCIV methods for three sets of stress T, and for each T, three different E_{OX} values have been used for stress. The E_{OX} and T dependencies of ΔV_T at fixed t_{STR} are shown in Chap. 1, Fig. 1.27 and that for

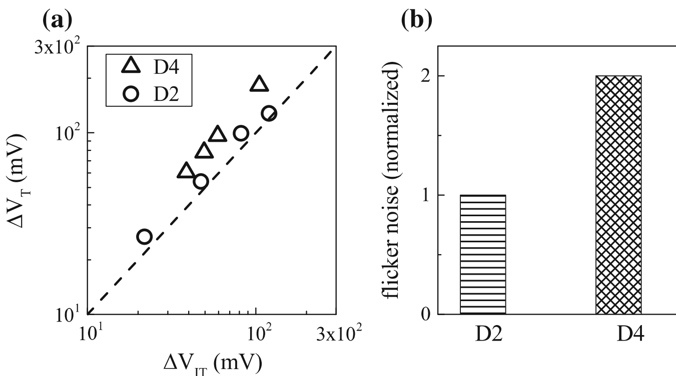

Fig. 3.9 **a** Correlation of UF-MSM measured ΔV_T and DCIV measured ΔV_{IT} for NBTI stress, and **b** pre-stress trap density measured by using flicker noise method, in HKMG p-MOSFETs having different HKMG gate insulator processes

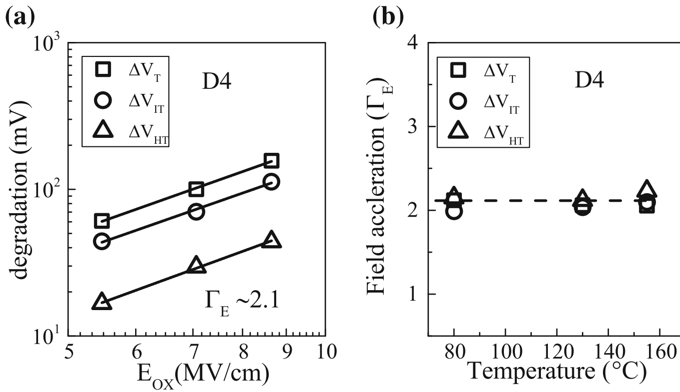

Fig. 3.10 **a** Fixed time UF-MSM measured ΔV_T, DCIV measured ΔV_{IT} and their difference (ΔV_{HT}) versus NBTI stress E_{OX} plotted in a log–log scale. **b** Extracted power-law field acceleration factor for ΔV_T, ΔV_{IT} and ΔV_{HT} versus stress T

ΔN_{IT} are shown before in Fig. 3.5. Measured ΔV_T and ΔV_{IT} as well as the extracted difference ΔV_{HT} obtained at a fixed t_{STR} for the HKMG device D4 are plotted in Fig. 3.10a versus stress E_{OX} for a particular stress T, and plotted in Fig. 3.11a versus stress T for a particular stress E_{OX}. Note that the ΔV_{IT} subcomponent dominates overall ΔV_T for all E_{OX} and T, even for D4 device having N in the gate insulator stack. Moreover, identical power-law E_{OX} dependence Γ_E is obtained for ΔV_T, ΔV_{IT} and therefore for ΔV_{HT}. However, extracted ΔV_{HT} has much lower Arrhenius T activation energy E_A compared to measured ΔV_{IT}, which explains lower E_A for ΔV_T when compared to E_A for ΔV_{IT} as shown.

As discussed before, ΔV_T and ΔN_{IT} have power-law time dependence with identical n across different E_{OX} and T, although n for ΔN_{IT} is higher than that for ΔV_T. Therefore, extracted Γ_E and E_A for ΔV_T, ΔV_{IT} and hence for ΔV_{HT} would be

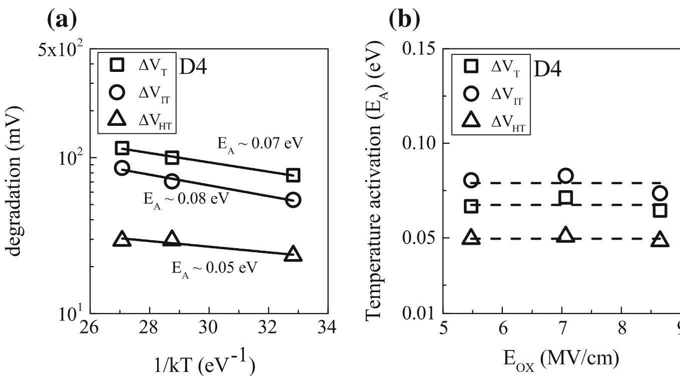

Fig. 3.11 **a** Fixed time UF-MSM measured ΔV_T, DCIV measured ΔV_{IT} and their difference (ΔV_{HT}) versus NBTI stress T plotted in a semi-log scale. **b** Extracted T activation energy for ΔV_T, ΔV_{IT} and ΔV_{HT} versus stress E_{OX}

independent of the value of t_{STR} used for extracting E_{OX} and T dependence, otherwise these terms would not have much meaning. Extracted Γ_E versus T for ΔV_T and its ΔV_{IT} and ΔV_{HT} subcomponents is shown in Fig. 3.10b, while the corresponding E_A versus E_{OX} relation is shown in Fig. 3.11b. Note that in the absence of different extraneous artifacts mentioned in Chap. 1, Sect. 1.3, Γ_E and E_A for both ΔV_T and ΔN_{IT} (or ΔV_{IT}) are independent of T and E_{OX} respectively as shown. Therefore, Γ_E and E_A of extracted ΔN_{HT} (or ΔV_{HT}) also has the same behavior as shown. Mutually uncoupled Γ_E and E_A is observed for other devices, not plotted here for brevity.

3.5 Trap Generation During PBTI

In this section, trap generation during PBTI stress in HKMG n-MOSFETs is studied using the DCIV [7] and SILC [41] techniques. DCIV scans trap generation located energetically in $\sim$0.3 eV around the Si band gap, and in HKMG MOSFETs, it can measure generated traps at Si/IL interface, IL bulk, as well as at IL/High-K interface especially for gate stacks having thin IL layers. As mentioned before, negligible g_m degradation during PBTI stress suggests negligible IL degradation and therefore, PBTI is believed to cause trap generation and trapping predominately in the HfO_2 High-K layer [36, 39]. DCIV measurements can probe trap generation during PBTI stress at and near the IL/High-K interface ($\Delta N_{IT\text{-}HK}$); refer to Fig. 1. As mentioned before, it is unlikely that DCIV method would probe much deeper into the High-K bulk.

As discussed in Chap. 2, SILC is estimated from measured gate current (I_G) before and during logarithmically spaced intervals of BTI stress. Increase in I_G after stress is due to trap assisted tunneling via newly generated traps, and therefore, the magnitude of increased gate current (ΔI_G) can be used to estimate density of generated traps during PBTI stress in HKMG n-MOSFETs [40]. Note that SILC has been used in the past to estimate gate insulator trap generation associated with the TDDB process [52–54], and also bulk trap generation during NBTI stress [55], in SiON MOSFETs. SILC is negligible during NBTI stress in HKMG p-MOSFETs due to band alignment issues mentioned in Chap. 2, while non-negligible SILC is observed in HKMG n-MOSFETs during PBTI stress [3, 16, 17, 40, 41]. Note that unlike DCIV that scans traps that are energetically aligned with Si mid gap, SILC scans traps close to the conduction band edge of the High-K layer [41]. However, there is a debate regarding the exact physical location of generated traps during PBTI stress in HKMG n-MOSFETs as probed by SILC; some report suggests it is at the IL/High-K interface [56], while other suggests it is deeper inside the High-K bulk [41]. Although the exact location of traps is an important aspect especially from the viewpoint of TDDB process, the type of generated traps probed by SILC has been found to have much smaller impact on PBTI degradation when compared to the impact of generated traps probed by the DCIV method [17], and will be discussed later in Chap. 4.

3.5.1 DCIV Measurements in DC Stress

Figure 3.12 plots the time evolution of generated interface traps ($\Delta N_{IT\text{-}HK}$) during PBTI stress at different $V_{G\text{-}STR}$ and stress T in HKMG n-MOSFETs with (a) non-nitrided (D2) and (b) N surface passivated (D4) IL. As mentioned before, $\Delta N_{IT\text{-}HK}$ is extracted from DCIV measurements after delay and band gap correction. The delay correction of DCIV is straightforward and the method used for NBTI can be used. However, the band gap correction is not obvious, as DCIV probes traps at or near the IL/High-K interface for PBTI stress, and the exact energetic extent of trap generation is yet unknown. For simplicity, a similar correction factor as used for NBTI stress is also assumed for PBTI stress in different HKMG devices.

Only longer time data are plotted, and measured $\Delta N_{IT\text{-}HK}$ increases with increase in $V_{G\text{-}STR}$ and T as expected. However unlike NBTI, the $\Delta N_{IT\text{-}HK}$ magnitude reduces significantly for the nitrided device D4 when compared to the non-nitrided device D2 at identical $V_{G\text{-}STR}$ and T. This happens in spite of higher E_{OX} for device D4 due to lower EOT, E_{OX} being calculated as $(V_{G\text{-}STR} - V_{T0})$/EOT, and hence is attributed to presence of N in the gate insulator stack. Similar to NBTI, time evolution of $\Delta N_{IT\text{-}HK}$ for PBTI stress shows power-law dependence with identical time exponent ($n \sim 1/6$) for both devices and for different $V_{G\text{-}STR}$ and T; the exponent n is extracted by linear regression of measured $\Delta N_{IT\text{-}HK}$ time evolution in t_{STR} range of 10 s to 1 Ks. Remarkably, identical n has been obtained for both NBTI and PBTI stress as shown. Note that similar to NBTI stress data shown earlier, the process dependence of $\Delta N_{IT\text{-}HK}$ time exponent for PBTI stress is in contrast with process dependence of ΔV_T time exponent shown in Chap. 1, Figs. 1.25 and 1.33. Although ΔV_T has power-law dependence for PBTI stress with time exponent n that is independent of stress E_{OX} and T for a particular HKMG process, the value of n reduces for nitrided devices, unlike that seen here for $\Delta N_{IT\text{-}HK}$ data. Moreover, similar to that observed for NBTI stress, the value of n for $\Delta N_{IT\text{-}HK}$ is always higher than n for ΔV_T for PBTI stress, when extracted in the same range of t_{STR} as shown.

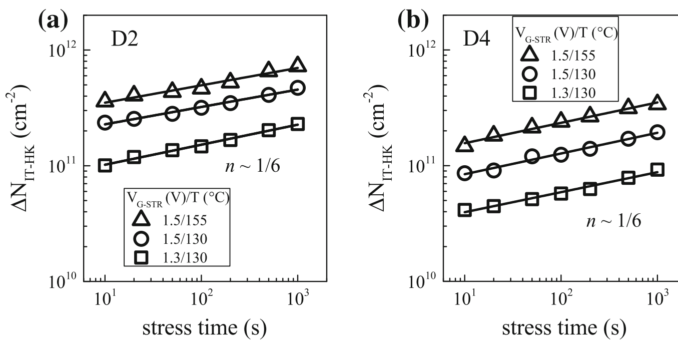

Fig. 3.12 DCIV measured time evolution of $\Delta N_{IT\text{-}HK}$ for PBTI stress at different $V_{G\text{-}STR}$ and T in HKMG n-MOSFETs having different IL processes

As a further proof of the universality of time exponent ($n \sim 1/6$) for PBTI stress, time evolution of $\Delta N_{IT\text{-}HK}$ is measured by using DCIV in different HKMG devices listed in Figs. 3.2, and 3.13 plots extracted n as a function of (a) $V_{G\text{-}STR}$ and (b) T after correction for measurement delay. Similar to NBTI, power-law time dependence with universal $n \sim 1/6$ is also obtained for $\Delta N_{IT\text{-}HK}$ during PBTI stress at different $V_{G\text{-}STR}$ and T in devices having different HKMG gate insulator processes. Once again, similar to NBTI results shown earlier, while a universal $n \sim 1/6$ exponent is obtained for time evolution of $\Delta N_{IT\text{-}HK}$ for PBTI stress in different HKMG devices, this is in contrast to the exponent obtained for time evolution of ΔV_T from UF-MSM technique; the latter shows strong gate insulator process dependence as discussed in Chap. 1, Sect. 1.6. The similarity of time evolution of ΔN_{IT} for NBTI and $\Delta N_{IT\text{-}HK}$ for PBTI stress is a very remarkable result and underlines the similarity of physical mechanism governing trap generation at Si/IL and IL/High-K interfaces, and will be discussed later in this book.

Similar to NBTI results shown earlier, $\Delta N_{IT\text{-}HK}$ time evolution for PBTI stress also has power-law dependence with similar n across different stress E_{OX} and T as shown. Therefore, the power-law E_{OX} acceleration factor Γ_E and Arrhenius T activation energy E_A for $\Delta N_{IT\text{-}HK}$ extracted at a fixed t_{STR} would remain independent of t_{STR}. PBTI experiments were done at three sets of stress T, and at each T, three different E_{OX} values have been used for stress. Figure 3.14 plots (a) stress E_{OX} and (b) stress T dependence of $\Delta N_{IT\text{-}HK}$ obtained from DCIV measurements after delay and band gap corrections. Measured values of Γ_E and E_A extracted from E_{OX} and T dependence of $\Delta N_{IT\text{-}HK}$ for PBTI stress are independent of T and E_{OX}, respectively. This behavior is similar to the E_{OX} and T dependent parameters of ΔV_T shown in Chap. 1, Fig. 1.27. Moreover, this observation is identical to the NBTI results discussed before in this chapter. As mentioned before, mutually independent E_{OX} and T dependencies are observed when stress and measurements remain free from artifacts mentioned earlier in Chap. 1, Sect. 1.3.

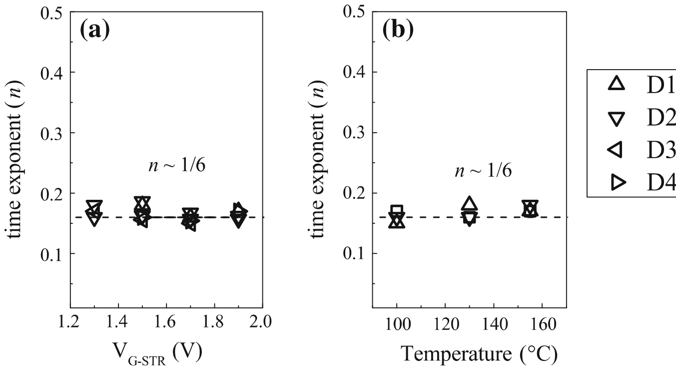

Fig. 3.13 Extracted long-time power-law time exponent n for different HKMG devices as a function of **a** stress V_G and **b** stress T, obtained using DCIV measurements during PBTI stress

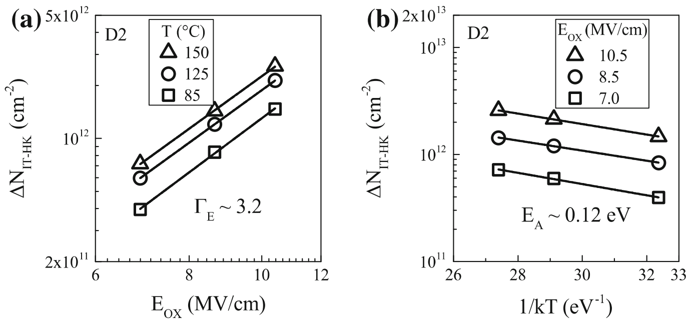

Fig. 3.14 Fixed time DCIV measured $\Delta N_{IT\text{-}HK}$ versus **a** stress E_{OX} and **b** stress T for PBTI stress in HKMG n-MOSFETs. E_{OX} dependence is shown for different T and T dependence shown for different E_{OX}. E_{OX} dependence is plotted in a log–log scale and T dependence is plotted in a semi-log scale

Figure 3.15 plots the impact of IL thickness on (a) power-law field acceleration factor Γ_E and (b) Arrhenius T activation energy E_A extracted from DCIV measured $\Delta N_{IT\text{-}HK}$ data after delay and band gap corrections, obtained for PBTI stress in different HKMG devices shown in Fig. 3.2. Reduction in IL thickness is achieved using different RTP based thermal IL (D1, D2), post High-K nitridation (D3), and RTP based IL on N passivated Si substrate (D4), refer to Fig. 3.2. Similar to NBTI, Γ_E for PBTI reduces with EOT scaling. However unlike NBTI, only negligible reduction in E_A has been observed with EOT scaling. Similar to NBTI results shown before, the magnitude of Γ_E for $\Delta N_{IT\text{-}HK}$ is similar to Γ_E for ΔV_T for a particular device also for PBTI stress, while E_A for $\Delta N_{IT\text{-}HK}$ is always higher compared to the corresponding value for ΔV_T; refer to Chap. 1, Fig. 1.35 for dependence of ΔV_T parameters on IL thickness. This aspect will be discussed later in this chapter.

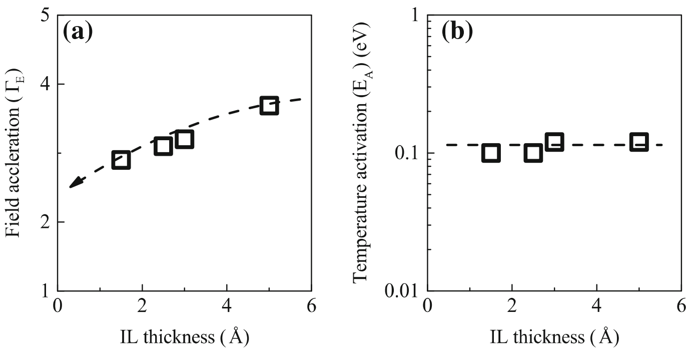

Fig. 3.15 Power-law field acceleration factor (Γ_E) and Arrhenius T activation energy (E_A) of DCIV measured $\Delta N_{IT\text{-}HK}$ for PBTI stress, as a function of IL thickness of different HKMG stacks

3.5.2 DCIV Measurements in AC Stress

DCIV assessment of trap generation during AC stress is done in MSM mode similar to DC stress, and measurements were performed before and during logarithmically spaced stress intervals. Figure 3.16 plots time evolution of $\Delta N_{IT\text{-}HK}$ during AC stress at different (a) PDC and (b) f but identical stress E_{OX} and T, obtained from DCIV measurements after delay and band gap corrections. Only long t_{STR} data are plotted, and the corresponding DC data are also shown. Similar to NBTI stress as discussed before, the DC stress bias and AC stress pulses for PBTI stress were applied for identical t_{STR} duration, and actual duration of AC stress depends on PDC of the applied AC pulse. Time evolution of $\Delta N_{IT\text{-}HK}$ shows power-law dependence at longer t_{STR}; the exponent n extracted in t_{STR} range of 10 s to 1 Ks is

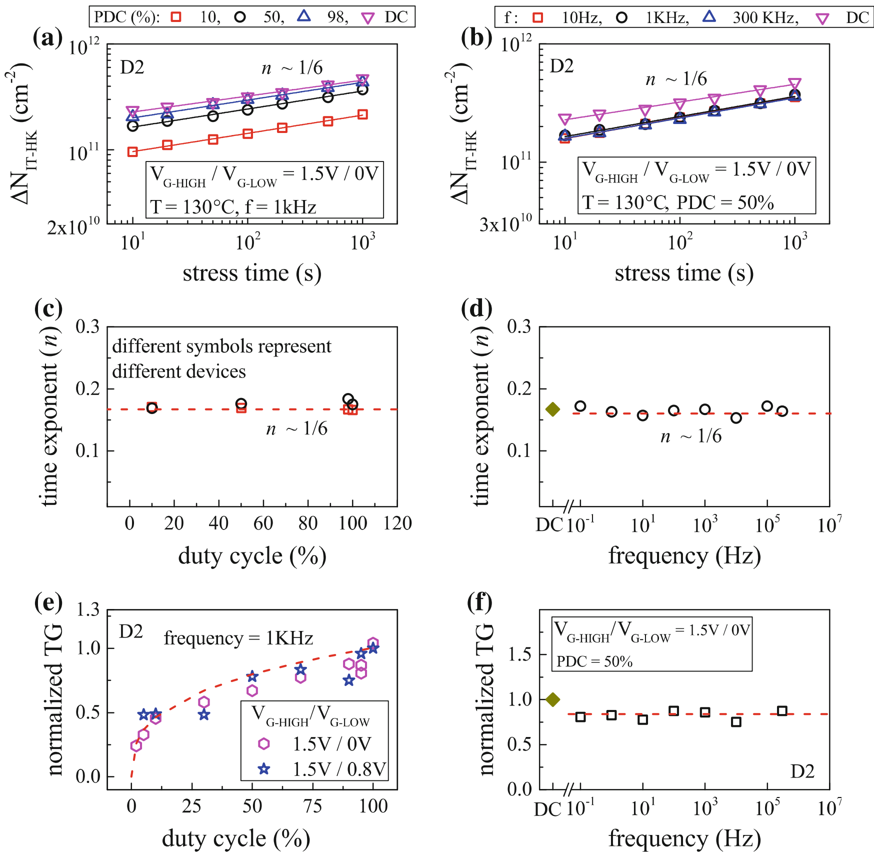

Fig. 3.16 DCIV measured time evolution of $\Delta N_{IT\text{-}HK}$ for AC PBTI stress at different **a** PDC and **b** frequency; the PDC and f values used in panel **a** and **b** respectively are mentioned at the *top*. Measured long-time power-law time exponent n as a function of **c** PDC for different devices and **d** frequency. Fixed time measured $\Delta N_{IT\text{-}HK}$ versus **e** PDC for different $V_{G\text{-}LOW}$ and **f** frequency

also plotted in Fig. 3.16 as a function of (c) PDC and (d) f of the gate pulse. The DC value is shown as reference.

Similar to NBTI stress results shown earlier, identical n (~1/6) is observed for DC and AC PBTI stress at different PDC and f. Once again, similar to NBTI, identical n of $\Delta N_{IT\text{-}HK}$ time evolution for DC and AC PBTI stress is in contrast to the observed time evolution of ΔV_T measured using UF-MSM technique and shown in Chap. 1, Fig. 1.31; ΔV_T time evolution has lower n for DC compared to AC stress. Moreover when extracted in the same t_{STR} range, $\Delta N_{IT\text{-}HK}$ shows higher n compared to ΔV_T for DC stress, but both $\Delta N_{IT\text{-}HK}$ and ΔV_T show identical n (~1/6) for AC stress also for PBTI stress, which is again similar to NBTI stress results shown before. Once again, the universality of n ~ 1/6 for $\Delta N_{IT\text{-}HK}$ time evolution during DC and AC PBTI stress suggest the robustness of the underlying physical mechanism of interface trap generation and will be discussed later in the book.

Figure 3.16 also plots the measured $\Delta N_{IT\text{-}HK}$ at fixed t_{STR} for AC PBTI stress as a function of (e) PDC and (f) f of the gate pulse. Once again, AC pulses having identical pulse high but different pulse low values were used to study the PDC dependence. AC data are normalized to the corresponding DC value at identical t_{STR}. Similar to that shown earlier for NBTI, the magnitude of $\Delta N_{IT\text{-}HK}$ for PBTI stress increases with increase in PDC but remains independent of the pulse low value and f of the gate pulse. Remarkably similar AC to DC ratio and PDC dependent shape has been observed for NBTI and PBTI stress. Moreover, although the f independence of $\Delta N_{IT\text{-}HK}$ for PBTI stress is qualitatively similar to that observed for ΔV_T shown in Chap. 1, Fig. 1.32, $\Delta N_{IT\text{-}HK}$ and ΔV_T show very different AC to DC ratio. This observation is similar to that reported for NBTI stress. Once again, similar to NBTI, the PDC dependence of $\Delta N_{IT\text{-}HK}$ for PBTI stress is both qualitatively and quantitatively different from the PDC dependence of ΔV_T shown in Chap. 1. Similar to NBTI results, $\Delta N_{IT\text{-}HK}$ for PBTI also does not have the "S" shaped PDC dependence as observed for ΔV_T, and unlike ΔV_T, no "kink" or "jump" is observed for $\Delta N_{IT\text{-}HK}$ data between high PDC AC and DC stress. Moreover as mentioned earlier, $\Delta N_{IT\text{-}HK}$ has very different AC to DC ratio compared to ΔV_T, and unlike ΔV_T, the AC to DC ratio for $\Delta N_{IT\text{-}HK}$ does not depend on the pulse low value. The PDC and f dependencies of $\Delta N_{IT\text{-}HK}$ and ΔV_T for AC PBTI stress have been found to be remarkably similar to AC NBTI stress as shown earlier in this chapter and also in Chap. 1.

3.5.3 SILC Measurements in DC Stress

As mentioned before, increase in gate leakage current (I_G) after stress is also used to calculate trap generation during PBTI stress [40, 41]. While DCIV scans generated traps aligned energetically with the Si [7] mid gap, SILC scans traps closer to the conduction band edge of High-K layer, although the exact physical location of these traps are debated [41, 56]. I_G versus V_G sweeps were taken before and during

logarithmic intervals of stress, and generated trap density ($\Delta N_{OT\text{-}HK}$) is calculated as discussed in Chap. 2 [40].

Figure 3.17 plots the time evolution of $\Delta N_{OT\text{-}HK}$ calculated from SILC for different $V_{G\text{-}STR}$ and T in (a) D2 and (b) D4 HKMG n-MOSFETs; refer to Fig. 3.2 for device details. Note that SILC in HKMG devices recovers after removal of stress, and therefore, measured data must be corrected for measurement delay following the methodology shown in Chap. 2. Only long t_{STR} data are plotted; magnitude of $\Delta N_{OT\text{-}HK}$ increases with $V_{G\text{-}STR}$ and T as expected, but reduces drastically for the device D4 having N in the gate stack. Note that D4 device have thinner EOT and would have higher E_{OX} compared to device D2 for a given $V_{G\text{-}STR}$. Therefore, the reduction can be attributed to the presence of N in the gate insulator stack. It is interesting to remark that both DCIV and SILC measurements show reduced trap generation in nitrided devices during PBTI stress. Although the time evolution of $\Delta N_{OT\text{-}HK}$ from SILC shows power-law dependence, the time exponent n is much larger when compared to that for DCIV measured $\Delta N_{IT\text{-}HK}$ and UF-MSM measured ΔV_T time evolution data shown earlier in the book.

As a further proof, Fig. 3.18 plots extracted time exponent n from $\Delta N_{OT\text{-}HK}$ time evolution measured using SILC after delay correction, versus (a) $V_{G\text{-}STR}$ and (b) T. As done earlier, the exponent n is extracted by linear regression of measured time evolution of $\Delta N_{OT\text{-}HK}$ data in t_{STR} range of 10 s to 1 Ks. Data from different HKMG devices shown in Fig. 3.2 are plotted, and the trend line corresponding to DCIV data is also shown as a reference.

Note that SILC data show similar n ($\sim$1/3) for different $V_{G\text{-}STR}$ and T and for different devices, which signifies the robustness of the underlying physical mechanism. However, the magnitude of time exponent n from SILC is considerably higher than n ($\sim$1/6) obtained from DCIV, which unequivocally suggests different physical mechanism of generated traps that are probed by these methods. On the other hand, a remarkable similarity of extracted n has been observed during NBTI and PBTI stress

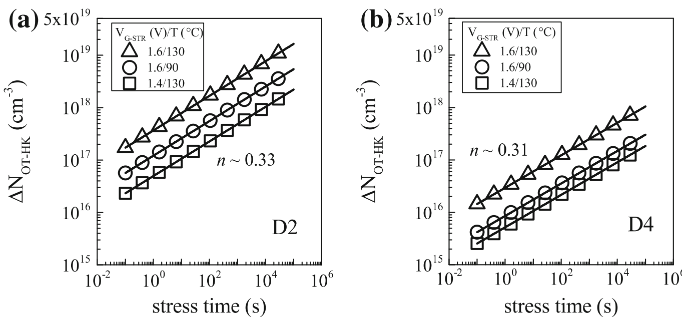

Fig. 3.17 SILC measured time evolution of $\Delta N_{OT\text{-}HK}$ for PBTI stress at different $V_{G\text{-}STR}$ and T in HKMG n-MOSFETs having different IL processes

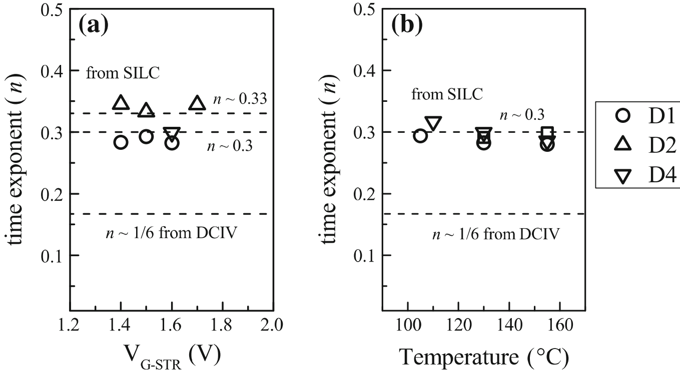

Fig. 3.18 Extracted long-time power-law time exponent *n* for different HKMG devices as a function of **a** stress V_G and **b** stress *T* using SILC measurements during PBTI stress. The reference line for DCIV measurement is also shown

for DCIV measurements, refer to Figs. 3.4 and 3.13, which suggests similar generation mechanism for these traps. This will be discussed later in this book.

Figure 3.19 plots measured $\Delta N_{OT\text{-}HK}$ at fixed t_{STR} from delay corrected SILC data versus (a) stress E_{OX} and (b) stress T, for D2 and D4 HKMG n-MOSFETs. The magnitude of $\Delta N_{OT\text{-}HK}$ reduces for the nitrided device D4, although the power-law E_{OX} acceleration factor Γ_E and Arrhenius T activation energy E_A remain independent of HKMG processes. As $\Delta N_{OT\text{-}HK}$ shows power-law time dependence and identical n across stress E_{OX} and T, extracted Γ_E and E_A would be independent of t_{STR}. Note that Γ_E and E_A for $\Delta N_{OT\text{-}HK}$ obtained from SILC has much larger value when compared to $\Delta N_{IT\text{-}HK}$ from DCIV and ΔV_T from UF-MSM measurements

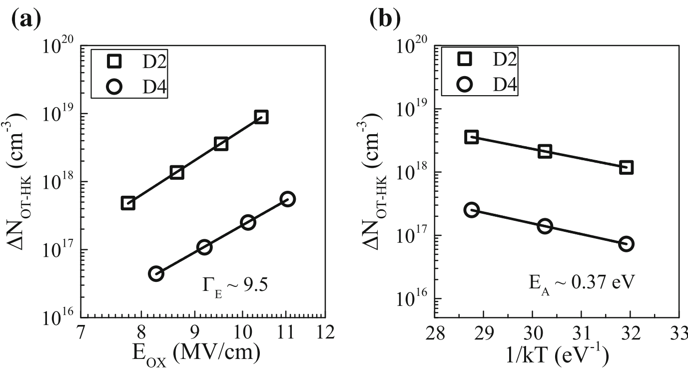

Fig. 3.19 Fixed time SILC measured $\Delta N_{OT\text{-}HK}$ versus **a** stress E_{OX} and **b** stress *T* for PBTI stress in HKMG n-MOSFETs. E_{OX} dependence is plotted in a log–log scale and *T* dependence is plotted in a semi-log scale

shown earlier in the book. Different Γ_E and E_A also suggest different physical mechanism of generated traps as probed by DCIV and SILC techniques during PBTI stress.

To understand the relative importance of different trap generation processes on PBTI degradation, Fig. 3.20 compares extracted (a) n, (b) Γ_E and (c) E_A for DCIV, SILC and UF-MSM measurements, as a function of IL thickness for D1 through D4 HKMG devices shown in Fig. 3.2. Note that $\Delta N_{OT\text{-}HK}$ parameters obtained from SILC measurements remain almost constant across IL thickness and show significantly higher values when compared to the ΔV_T and $\Delta N_{IT\text{-}HK}$ parameters obtained respectively from UF-MSM and DCIV measurements. Between DCIV and UF-MSM measurements, power-law time exponent n is somewhat higher for $\Delta N_{IT\text{-}HK}$ compared to ΔV_T for all devices and n reduces with IL scaling for both ΔV_T and $\Delta N_{IT\text{-}HK}$; however, much larger reduction is observed for ΔV_T for deeply scaled IL. The power-law E_{OX} acceleration Γ_E shows similar values for ΔV_T and $\Delta N_{IT\text{-}HK}$ and reduces slightly with IL scaling. Arrhenius T activation energy E_A for $\Delta N_{OT\text{-}HK}$ remains almost constant with IL, but that for ΔV_T and $\Delta N_{IT\text{-}HK}$ reduces slightly with IL scaling. It will be shown in Chap. 4 that the voltage shift corresponding to generated bulk traps from SILC is negligible compared to that for generated interface traps from DCIV, and it is the later that dominates PBTI degradation. Therefore, the parameters n, Γ_E and E_A for ΔV_T are closer to the parameters for $\Delta N_{IT\text{-}HK}$ rather than that for $\Delta N_{OT\text{-}HK}$. Of course, additional contribution from electron trapping in High-K bulk must be considered to compute ΔV_T, as discussed in the following section.

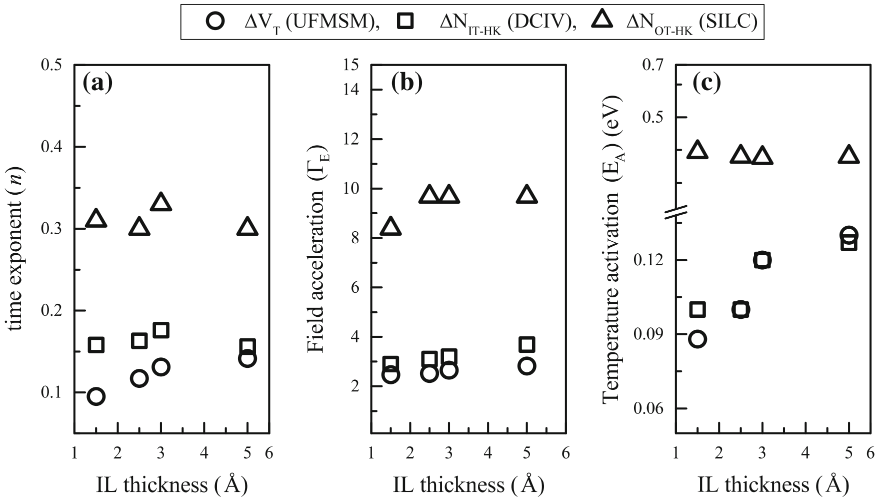

Fig. 3.20 **a** Power-law time dependence n, **b** power-law field acceleration factor Γ_E and **c** Arrhenius T activation energy E_A obtained using UF-MSM, DCIV and SILC methods for PBTI stress, versus IL thickness of different HKMG stacks

3.6 Electron Trapping During PBTI

Although trap generation in the IL is negligible for PBTI stress and the generated traps at or near the IL/High-K interface ($\Delta N_{IT\text{-}HK}$) plays a crucial role, it alone cannot explain ΔV_T measured using UF-MSM method. As an evidence of additional contribution from electron trapping in pre-existing, process related High-K bulk traps (ΔN_{ET}), Fig. 3.21 plots time evolution of ΔV_T and $\Delta V_{IT\text{-}HK}$ (=q/C_{OX} * $\Delta N_{IT\text{-}HK}$) respectively measured using UF-MSM and DCIV techniques. Experiments were performed in HKMG n-MOSFETs having (a) non-nitrided (D2) and (b) N surface passivated (D4) IL, refer to Fig. 3.2; C_{OX} is gate insulator capacitance and q is the electronic charge. Identical $V_{G\text{-}STR}$ and T have been used for both devices, and experimental DCIV data were corrected for measurement delay and band gap differences as discussed before. Since $\Delta V_{IT\text{-}HK}$ signifies the component of ΔV_T contributed by generated interface traps at IL/High-K interface, the difference between ΔV_T and $\Delta V_{IT\text{-}HK}$ signifies the contribution due to electron trapping in pre-existing traps, ΔV_{ET} (=q/C_{OX} * ΔN_{ET}). Time evolution of ΔV_{ET} is also plotted in Fig. 3.21. Only longer t_{STR} data are plotted, and contribution from $\Delta V_{IT\text{-}HK}$ dominates ΔV_T for both devices as shown.

Similar to NBTI data, time evolution of $\Delta V_{IT\text{-}HK}$ for PBTI stress shows power-law dependence with exponent $n \sim 1/6$ and ΔV_{ET} saturates at longer t_{STR}. Therefore, time evolution of ΔV_T (=$\Delta V_{IT\text{-}HK} + \Delta V_{ET}$) shows power-law dependence with lower n compared to that for $\Delta V_{IT\text{-}HK}$. However contrary to NBTI, the $\Delta V_{IT\text{-}HK}$ component of ΔV_T reduces drastically for the N containing device D4 compared to the non-nitrided device D2, while an increase is observed for the ΔV_{ET} component. Note that device D4 has lower EOT and therefore higher E_{OX} when compared to device D2 at identical $V_{G\text{-}STR}$. As $\Delta V_{IT\text{-}HK}$ dominates overall ΔV_T for both D2 and D4 devices, the magnitude of ΔV_T and its power-law time exponent n reduce for

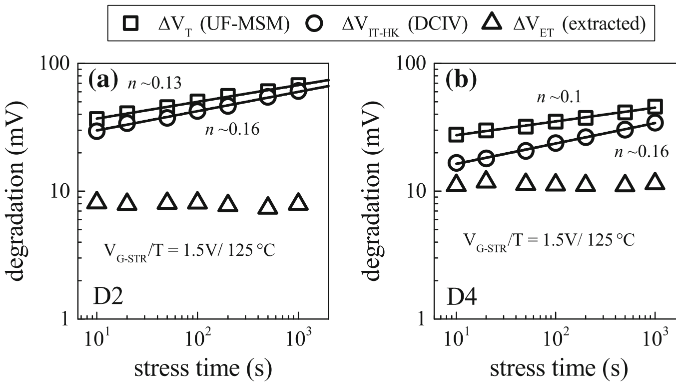

Fig. 3.21 Time evolution of UF-MSM measured ΔV_T and DCIV measured $\Delta N_{IT\text{-}HK}$ contribution after measurement delay and band gap correction ($\Delta V_{IT\text{-}HK}$), for PBTI stress in HKMG n-MOSFETs having different IL processes. Extracted difference (ΔV_{ET}) is also shown

device D4 as shown. Therefore, Fig. 3.21 clearly shows that underlying $\Delta N_{IT\text{-}HK}$ and ΔN_{ET} components of PBTI are clearly uncorrelated; i.e., while $\Delta N_{IT\text{-}HK}$ reduces, ΔN_{ET} increases for the D4 device, which can explain the measured reduction in ΔV_T and n. This aspect is further discussed in detail in Chap. 4.

As an additional proof, Fig. 3.22a plots the correlation of measured ΔV_T and $\Delta V_{IT\text{-}HK}$ for HKMG devices D2 and D4. As mentioned before, ΔV_T is obtained using UF-MSM method and $\Delta V_{IT\text{-}HK}$ using DCIV method after delay and band gap corrections. The 1:1 correlation line corresponding to zero electron trapping contribution is also plotted. Note that for a particular $\Delta V_{IT\text{-}HK}$, D2 device shows slightly higher ΔV_T than the 1:1 correlation line. However, much larger ΔV_T is observed for device D4, which is consistent with relatively larger ΔN_{ET} contribution for device D4 having N in the gate insulator stack. Larger magnitude of electron trapping during NBTI stress in gate insulators containing N has been analyzed using DFT simulations; refer to [17] for additional details.

Similar to hole trapping in NBTI, electron trapping during PBTI also occurs in pre-existing, process related gate insulator traps; while the hole traps are located in IL, electron traps are located in the High-K layer. As done in p-MOSFETs, flicker noise method can also be used to access the density of High-K electron traps in n-MOSFETs. Figure 3.22b shows measured pre-existing trap density in devices D2 and D4. Note that the nitrided device D4 shows higher trap density, which is consistent with higher ΔN_{ET} contribution shown in Figs. 3.21 and 3.22a, and is also consistent with DFT simulation results [17].

Similar to NBTI stress, time evolution of ΔV_T and $\Delta N_{IT\text{-}HK}$ during PBTI stress has been measured respectively using UF-MSM and DCIV methods for three sets of stress T, and for each T, three different stress E_{OX} have been used. The E_{OX} and T dependencies of ΔV_T at fixed t_{STR} are shown in Chap. 1, Fig. 1.27, and the same for ΔN_{IT} are shown earlier in Fig. 3.13. Measured ΔV_T, $\Delta V_{IT\text{-}HK}$ and their difference ΔV_{ET} at a particular t_{STR} for the HKMG device D4 is plotted versus stress E_{OX} at a

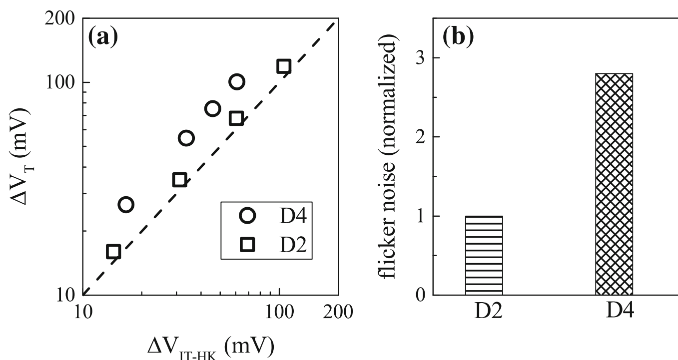

Fig. 3.22 **a** Correlation of UF-MSM measured ΔV_T and DCIV measured $\Delta V_{IT\text{-}HK}$ for PBTI stress, and **b** pre-stress trap density measured by using flicker noise method, in HKMG n-MOSFETs having different HKMG gate insulator processes

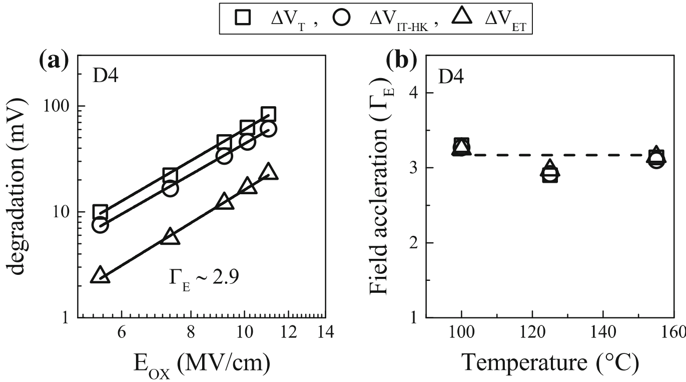

Fig. 3.23 **a** Fixed time UF-MSM measured ΔV_T, DCIV measured $\Delta V_{IT\text{-}HK}$ and their difference (ΔV_{ET}) versus PBTI stress E_{OX} plotted in a log–log scale. **b** Extracted power-law field acceleration factor for ΔV_T, ΔV_{IT} and ΔV_{ET} as a function of stress T

particular stress T in Fig. 3.23a, and also plotted versus stress T for a fixed stress E_{OX} in Fig. 3.24a. Note that $\Delta V_{IT\text{-}HK}$ subcomponent dominates overall ΔV_T for all E_{OX} and T, even for this particular device having N in the gate insulator stack. Moreover, identical power-law E_{OX} dependence Γ_E is obtained for ΔV_T, $\Delta V_{IT\text{-}HK}$ and therefore for ΔV_{ET}. However, ΔV_{ET} shows much lower Arrhenius T activation energy E_A compared to ΔV_T and $\Delta V_{IT\text{-}HK}$. Note that the relative values of Γ_E and E_A for ΔV_T, $\Delta V_{IT\text{-}HK}$ and ΔV_{ET} for PBTI stress are similar to that observed for NBTI stress data shown earlier in this chapter.

As shown before, ΔV_T and $\Delta N_{IT\text{-}HK}$ have power-law time dependence with identical n across different E_{OX} and T, although higher n has been observed for

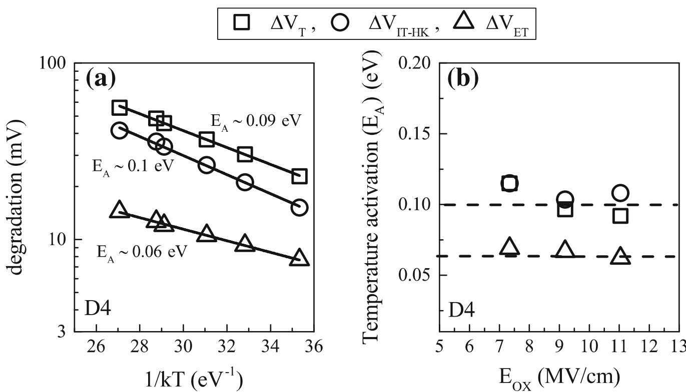

Fig. 3.24 **a** Fixed time UF-MSM measured ΔV_T, DCIV measured $\Delta V_{IT\text{-}HK}$ and their difference (ΔV_{ET}) versus PBTI stress T plotted in a semi-log scale. **b** Extracted T activation energy for ΔV_T, ΔV_{IT} and ΔV_{ET} as a function of stress E_{OX}

$\Delta N_{IT\text{-}HK}$ compared to ΔV_T data. Therefore, extracted Γ_E and E_A for ΔV_T, $\Delta V_{IT\text{-}HK}$ and therefore for ΔV_{ET} would be independent of the value of t_{STR} used for extracting E_{OX} and T dependence. Extracted Γ_E for ΔV_T and underlying $\Delta V_{IT\text{-}HK}$ and ΔV_{ET} subcomponents are plotted versus T in Fig. 3.23b, while their corresponding E_A values are plotted versus E_{OX} in Fig. 3.24b. Note that in the absence of different extraneous artifacts mentioned in Chap. 1, Sect. 1.3, Γ_E and E_A for ΔV_T and $\Delta N_{IT\text{-}HK}$ (or $\Delta V_{IT\text{-}HK}$) are shown to be independent of T and E_{OX}, respectively. Therefore, Γ_E and E_A of extracted ΔN_{ET} (or ΔV_{ET}) also show the same behavior as shown. These features of PBTI stress are exactly identical to NBTI, and similar mutually uncoupled Γ_E and E_A has been observed for other devices, not plotted here for brevity.

3.7 Location of Generated Traps (DCIV Measurements)

As discussed earlier in this chapter, although hole and electron trapping cannot be ignored respectively for NBTI and PBTI stress, trap generation plays the dominant role. DCIV technique has been used to access trap generation during BTI stress, and the resulting data show very similar time, bias and temperature dependence for NBTI and PBTI stress in different HKMG devices. This suggests very similar underlying physical mechanism of DCIV accessed trap generation for NBTI and PBTI. SILC is not observed for NBTI due to band alignment issues but is present for PBTI stress; although the magnitude of generated bulk traps that are responsible for SILC has been found to be smaller compared to that probed by DCIV, refer to Chap. 4 for details. DCIV accessed trap generation during NBTI and PBTI has been attributed to Si/IL and IL/High-K interfaces respectively by noting the presence or absence of degradation in g_m. Trap generation in the IL in any significant quantity is ruled out for PBTI stress due to the absence of Δg_m, while the presence of Δg_m suggests trap generation in IL for NBTI stress. The similarities of DCIV measured trap generation during NBTI and PBTI stress have been shown before, which suggests similarity of underlying physical mechanism. In this section, experimental proof is provided to bring out their differences, which will ascertain the difference in physical location. All DCIV data shown in this section are corrected for delay and band gap using the procedure described in Chap. 2.

Figure 3.25 plots the E_{OX} dependence of generated traps obtained at fixed t_{STR} for (a) NBTI and (b) PBTI stress in HKMG devices having relatively thicker (D1) and thinner (D2) IL, refer to Fig. 3.2. IL thickness has no impact for NBTI stress since generated traps are at the Si/IL interface. However, magnitude of generated traps increases for thinner IL device for PBTI stress. As discussed in Chap. 5, trap generation for NBTI stress in p-MOSFETs is caused due to tunneling of inversion layer holes into the Si–H bonds at Si/IL interface, and therefore, the magnitude is independent of IL thickness. However, trap generation at or near the IL/High-K interface for PBTI stress in n-MOSFETs occurs due to tunneling of inversion layer electrons, which increases with reduction in IL thickness, and therefore causes higher trap generation magnitude for thinner IL devices as shown.

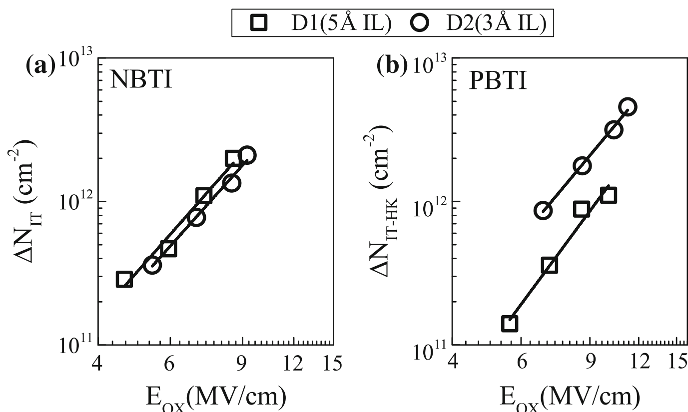

Fig. 3.25 DCIV measured trap generation versus E_{OX} for **a** NBTI and **b** PBTI stress in HKMG MOSFETs having different IL thickness

Figure 3.26 plots the E_{OX} dependence of generated traps obtained at fixed t_{STR} for (a) NBTI and (b) PBTI stress in HKMG devices without (D2) and with (D3) post High-K nitridation using the DPN process, refer to Fig. 3.2. Nitridation impact is negligible for NBTI stress, but trap generation reduces significantly for device D3 for PBTI stress. Since N incorporation is done after High-K deposition, higher N density is expected in the High-K compared to the IL layer, especially for denser thermal IL used in this study that show much lower N penetration, refer to [51] for additional evidence from Angle Resolved X-ray Photoelectron Spectroscopy measurements. Therefore, post High-K nitridation has larger impact on generated

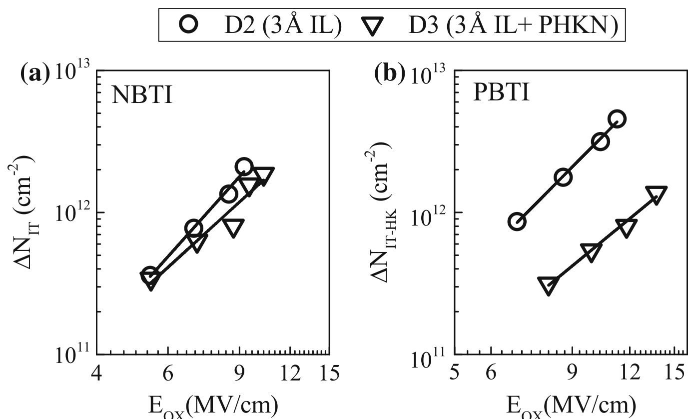

Fig. 3.26 DCIV measured trap generation versus E_{OX} for **a** NBTI and **b** PBTI stress in HKMG MOSFETs without and with nitridation after High-K deposition

traps at or near the IL/High-K interface for PBTI stress compared to that at Si/IL interface for NBTI stress. The exact physical mechanism responsible for reduction in trap generation for nitrided gate stacks is not known and need further study.

Figure 3.27 plots the E_{OX} dependence of generated traps obtained at fixed t_{STR} for (a) NBTI and (b) PBTI stress in HKMG devices D5 through D7 having different pre-cleans before IL growth and High-K deposition, refer to Fig. 3.2. Devices D5 and D6 have similar pre-clean before IL but different pre-clean before High-K and hence similar IL but different High-K quality. On the other hand, devices D6 and D7 have different pre-clean before IL but similar pre-clean before High-K and hence different IL but similar High-K quality. Therefore, trap generation at Si/IL interface for NBTI stress in p-MOSFETs is similar for D5 and D6 but different for D6 and D7 devices, while trap generation at or near the IL/High-K interface for PBTI stress in n-MOSFETs is different for D5 and D6 and similar for D6 and D7 devices as shown.

Although DCIV assessed generated traps for NBTI and PBTI have similar time dynamics and E_{OX} and T dependence, they have very different HKMG process dependence as shown in Figs. 3.25, 3.26 and 3.27 that clearly verifies the difference in physical location of these generated traps. As a further evidence, Fig. 3.28 correlates g_m degradation to generated trap density measured using DCIV for NBTI and PBTI stress. Note that NBTI shows higher Δg_m for a particular trap density when compared to PBTI stress. Since Δg_m is due to mobility degradation resulting from Coulomb scattering by BTI charges and as trap generation dominates both NBTI and PBTI degradation, higher Δg_m is caused by trap generation at Si/IL interface for NBTI than that at IL/High-K interface for PBTI.

Therefore, although DCIV measured traps during NBTI and PBTI stress respectively in p- and n-channel HKMG MOSFETs show very similar kinetics, they have very different physical location as discussed above.

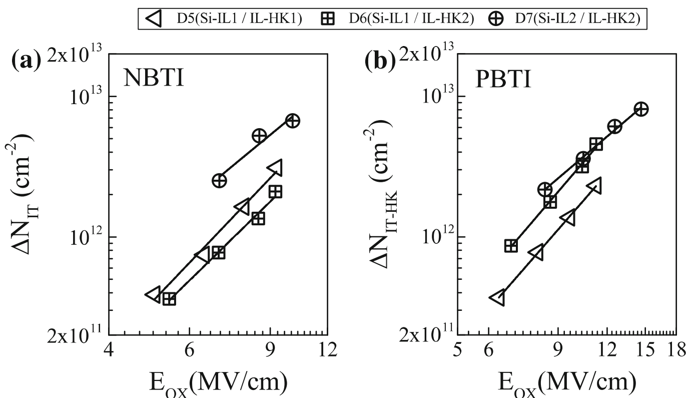

Fig. 3.27 DCIV measured trap generation versus E_{OX} for **a** NBTI and **b** PBTI stress in HKMG MOSFETs having different pre-clean processes before IL growth and High-K deposition. Refer to Fig. 3.2 for details

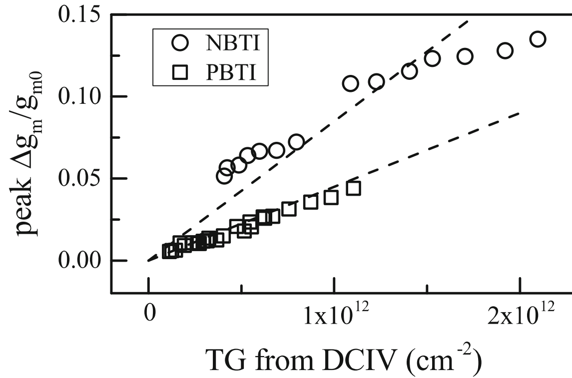

Fig. 3.28 Correlation of peak transconductance degradation to DCIV measured generation of traps for NBTI and PBTI stress

3.8 Summary

To summarize, the underlying subcomponents of NBTI and PBTI degradation in p- and n-channel HKMG MOSFETs respectively have been analyzed using different direct characterization techniques. MOSFETs having different HKMG gate insulator processes have been studied. Process related pre-existing hole and electron traps respectively in the IL and High-K layers is accessed using flicker noise. The generation of traps during NBTI is studied using DCIV method, while that during PBTI stress using DCIV and SILC methods. The relative contribution of trapping and trap generation on BTI degradation has been accessed. Although hole trapping in IL for NBTI and electron trapping in High-K for PBTI contribute, it is observed that trap generation dominates NBTI and PBTI degradation for different HKMG gate insulator processes.

DCIV measures trap generation at Si/IL interface during NBTI and at or near IL/High-K interface during PBTI, refer to Fig. 3.1. Energetically, these traps are aligned to ~0.3 eV around the Si band gap as shown in Chap. 2. Although locations of DCIV accessed generated traps are different, at Si/IL interface for NBTI and at or near IL/High-K interface for PBTI, they show very similar time, bias, temperature, AC duty cycle, and frequency dependence between NBTI and PBTI stress, suggesting strong universality of the underlying physical process. SILC measures trap generation energetically located closer to the HfO_2 conduction band, however, the exact physical location of these traps are still debated. Nevertheless for PBTI stress, SILC accessed generated traps show very different time, temperature, and bias dependence compared to that measured by DCIV and suggests very different underlying physical mechanism. SILC accessed traps have been found to have negligible role in PBTI degradation.

The following observations can be made between trap generation measured using DCIV, hole or electron trapping, and UF-MSM measured threshold voltage degradation for both NBTI and PBTI stress:

(a) Contribution from generated interface traps, ΔV_{IT} for NBTI or $\Delta V_{IT\text{-}HK}$ for PBTI, shows power-law time dependence at long stress time and universal exponent $n \sim 1/6$ for DC stress at different E_{OX} and T, for AC stress at different f and PDC, and for different HKMG processes. Since the trapping component, ΔV_{HT} for NBTI or ΔV_{ET} for PBTI, saturates at long time ($n \sim 0$), the relative magnitude of trap generation and trapping determines the time exponent ($n < 1/6$) of overall ΔV_T. Trap generation and trapping are completely uncorrelated to each other.

(b) Incorporation of N in the gate insulator has minimal impact on ΔV_{IT} for NBTI but significantly reduces $\Delta V_{IT\text{-}HK}$ for PBTI stress, while N increases both ΔV_{HT} and ΔV_{ET} for NBTI and PBTI stress, respectively. This unequivocally indicates that the trap generation and trapping subcomponents are mutually uncorrelated. Although ΔV_{IT} and $\Delta V_{IT\text{-}HK}$ dominate NBTI and PBTI respectively, a relatively larger ΔV_{HT} or ΔV_{ET} contribution results in reduction in n for overall ΔV_T in HKMG devices containing N in the gate stack.

(c) The power-law E_{OX} acceleration factor Γ_E has been found to be identical for ΔV_{IT} and ΔV_{HT} (or for $\Delta V_{IT\text{-}HK}$ and ΔV_{ET}) and therefore for ΔV_T for all HKMG processes, although Γ_E reduces for devices containing N in the gate stack or with reduction in IL thickness.

(d) The Arrhenius T activation energy E_A is larger for ΔV_{IT} (or $\Delta V_{IT\text{-}HK}$) compared to ΔV_{HT} (or ΔV_{ET}). Therefore, the relative magnitude of trap generation and trapping determines E_A for overall ΔV_T. HKMG processes having relatively larger trapping subcomponent show lower E_A for ΔV_T and vice versa.

(e) For AC stress, ΔV_{IT} (or $\Delta V_{IT\text{-}HK}$) remains independent of f but increases with increase in PDC of the gate pulse. However, the AC/DC ratio and PDC dependent shape for ΔV_{IT} (or $\Delta V_{IT\text{-}HK}$) is very different from that for ΔV_T, and will be explained later in the book.

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