Chapter 33
Comparison of 6T and 8T SRAM Cell with Parameters at 45 nm Technology

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Abstract Static random access memory (SRAM) plays a most significant role in the microprocessor world, but as the technology is scaled down in nanometers, leakage current, leakage power and delay are the most common problems for SRAM cell which is basically designed in low power application. In this paper we compares the performance, working and simulation results of two different SRAM cell methods i.e. Conventional six transistor SRAM cell and proposed eight transistor SRAM cell Designing of 8T SRAM cell is done due to high speed operation. By simulating and performing operations we confirmed that our proposed conventional 8T SRAM cell has amend their parameters. During write operation of 8T SRAM cell gives leakage current is 69 pA, leakage power is 7.581 nW and delay is 20.55 ns and for read operation of leakage current is 53.90 pA, leakage power is 1.709 μW and delay is 21.44 ns and SNM of 8T SRAM Cell has greater stability by 29 % as compared to 6T SRAM.

33.1 Introduction

Static random access memory (SRAM) has its own applications mainly in the various types of portable devices. As the size is reduced the effect of leakage current, leakage power is increased in the circuit [1]. As we know that the number of transistor is maximum so that leakage current of an SRAM cell is high as it dominates in stand-by mode which is in direct relation to the number of transistor [2]. Due to scaling perform on devices a different design challenge arises for the nanometer design of SRAM memory [3]. 6T SRAM cells results to a low memory density compared with the DRAM cells design. Hence in conventional SRAM cell which uses 6T SRAM cell faces problems to meet the demand of large memory area in mobile application [4].

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33.1.1 6T SRAM Cell

In this case, we have minimizing the loading effect through PMOS transistor. In this SRAM cell design, we have used two inverter pair resulting two NMOS and 2 PMOS transistor are called active transistor and plus two additional NMOS transistor are connected in the row line. This architecture is known as 6T SRAM cell. This additional two transistor are used to retrieve data on bit lines i.e. BL (bit line) and BLB (bit line bar). Both bit line and word line (WL) are used for write and read operation. The main drawback of 6T SRAM cell is its huge size (Fig. 33.1).

33.1.1.1 Write Operation/Read Operation

When we performing a write operation, both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL = 1 and BLB = 0 or BL = 0 and BLB = 1). When WL enables transistors M5 and M6 then data writes on the output nodes Vout and Vout1 of back to back connected inverter. When we perform the read operation which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high. Since one of the output nodes (Vout and Vout1) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read.

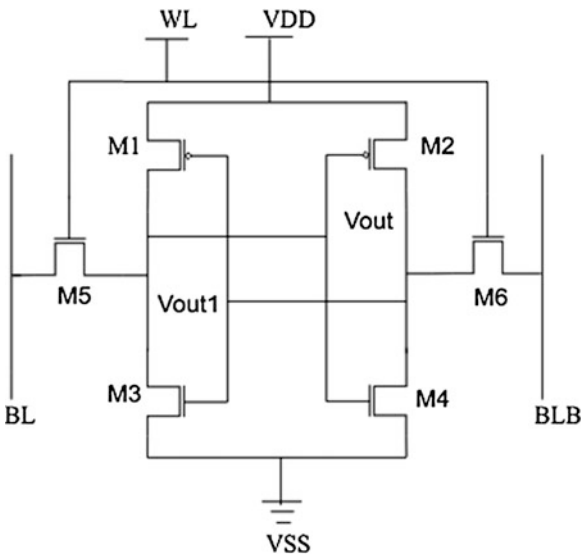

Fig. 33.1 Conventional 6T SRAM cell

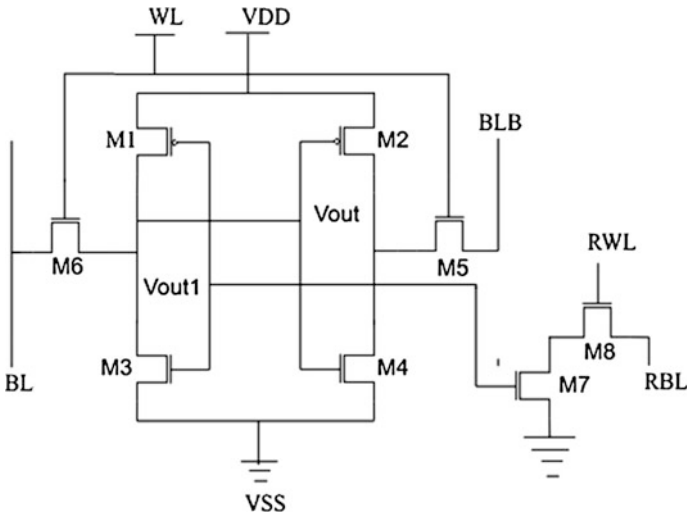

Fig. 33.2 Conventional 8T SRAM cell

33.1.2 8T SRAM Cell

When we designed the 6T SRAM cell so many problems are occurring due to continuous scaling of the technology. We add two more transistors for the low power design in 6T SRAM cell. In this cell we add two more transistor in 6T SRAM cell to access read bit line (RBL). Two transistors M7 and M8 are implemented to reduce leakage current.

Figure 33.2 shows the design of the 8T SRAM cell in which individual read word line (RWL) and RBL are used.

33.2 Perfomance Analysis and Simulation Result

For SRAM cell, the leakage current is the main basis of standby power consumption whose major components are the sub-threshold leakage, the reverse biased band-to-band tunneling junction leakage and the gate direct tunneling leakage in nano-scale devices. To define leakage power, whenever the CMOS inverter is in stable mode, it has its PMOS and NMOS transistor shot off (Table 33.1).

33.2.1 Static Noise Margin

To flip from one state to another in an SRAM cell Static Noise Margin may be defined as the minimum DC noise voltage by the cell. The Stability of the Cell is

Table 33.1 The comparison of different parameters of both 6T and 8T SRAM at 45 nm technology in cadence virtuoso tool

Parameters	Conventional 6T SRAM		Conventional 8T SRAM	
	Write	Read	Write	Read
Leakage current	69.22×10^{-12} A	54.88×10^{-12} A	69.00×10^{-12} A	53.90×10^{-12} A
Leakage power	7.346 nW	1.710×10^{-6} W	7.561 nW	1.709×10^{-6} W
Delay	20.57 ns	21.70 ns	20.55 ns	21.44 ns

Table 33.2 The comparison of SNM of both 6T and 8T SRAM at 45 nm technology

S. no.	SRAM	6T SRAM Cell	8T SRAM Cell
1.	RSNM	V_{OH} = 299 mV, V_{IH} = 392 mV	V_{OH} = 330 mV, V_{IH} = 375 mV
2.	WSNM	V_{IL} = 385 mV, V_{OL} = 315 mV	V_{IL} = 320 mV, V_{OL} = 390 mV
3.	Overall SNM	83.21 mV	117 mV

measured generally by the SNM. SNM of the SRAM cell depends on the supply voltage, pull up ratio (PR) and cell ratio (CR). CR is considered as the ratio of the driven transistor to the access transistor sizes. Pull-up ratio is defined as the ratio between sizes of the access transistor to the load transistor during write operation (Table 33.2).

This illustrates that SNM of 8T SRAM Cell is less than the 6T SRAM Cell. Therefore, 8T SRAM Cell is more stable than 6T SRAM cell.

33.3 Conclusion

For a high density and low leakage current, we propose a conventional 8T SRAM cell in which we perform both read and write operation and compare the result of both write and read operation with the 6T SRAM cell operation. By comparing we can say that, 8T SRAM cell possess low leakage current as compare to 6T SRAM cell and delay is also reduced in both read and write operation, but leakage power is increased in 8T SRAM cell than 6T SRAM cell. These designs also improve the read and write stability.

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