CMOS Amplifier Design Using Simplified g_m/I_D Technique

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Abstract This paper demonstrates design of analog circuits using g_m/I_D method. It explains the effectiveness of $g_m - I_D$ approach and then generates required plots using any simulator. Other than complex method of generating $g_m - I_D$ plots, which requires advanced simulators, it is shown that a plot of I_D/g_m can be easily generated directly using simulator or through a simple program capable to manipulate device current–voltage data. The success of g_m/I_D technique lies on the fact that it employs a simple rule of scaling device dimension (w) and scales the current as well as transconductance (g_m) equally, when other parameters are constant. Therefore, when a reference device with required g_m and I_D is found, it can be scaled up to generate desired g_m at the given bias current (power) I_D. Proposed method is not only technology independent, it is also free from complex mathematical expressions associated with the device as it employs data generated from simulators. As it is not based on analytical methods or models, its accuracy (independent of BSIM or ACM; and their parameter values) is much better specially for analog design. Most importantly incorporating simulator in the design process, analysis of the designed circuit, using the same simulator, is expected to match the desired performance closely. Using this simple approach, design time becomes shorter and a workable design can be made very quickly. Two basic amplifier circuits are designed using the proposed method, and simulation results are discussed.

Keywords Amplifier design · MOS sizing · g_m/I_D · Analog CMOS

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1 Introduction

Analog designs are carried out traditionally by analytical methods [1, 2] and then fine-tuned using a simulator to reach the final design. It is often observed that final design variables (device dimensions) differ largely from the estimated values obtained analytically. The difference in the predicted and the final design values can be reduced if complex models like BSIM are used while carrying out the design analytically. The designer often seeks for the help of another simulator, optimizer or programming method to reach the specifications [3, 4]. Whatever may be the approach, the net time to design any analog block increases, specially for designs using short-channel devices. Moreover, such methods increase the design complexity and make the task difficult for beginners designing analog circuits in submicron CMOS.

To overcome this challenge, a technology-independent approach is proposed by Kaspers [5–7] where g_m/I_D ratio is used to as key design parameter. It is found that this ratio-based technique can be applied to all kind of devices, both long and short channel [8]. Being free from complex analytical models, even novice designers can design analog blocks with desired performance within a short span of time with fewer iteration.

In the following sections, the principle of g_m/I_D approach is explained and the method is tested by designing amplifiers using 180 nm CMOS.

2 Basic Principles

Typically, analog designers first design any analog circuit with pen and paper using some device model whose equations can be manipulated with hand calculations (SPICE level 1 or 2). Usually, these models are based on long-channel devices. Once this design is complete, the designer implements the schematic using the device sizes projected analytically on a simulator. State-of-the-art simulators, however, use extremely complex and accurate deep submicron device models like BSIM3,4 to analyse the designed circuit. Consequently, simulation results do not match with the mathematical expectations. It may be mentioned that this error is primarily due to the modelling of short-channel devices with long-channel equations. The designer now adopts an ad hoc approach, adjusts the device dimensions, bias and attempts to meet the desired response from the circuit. In CMOS technology, keeping all the transistors in saturation is one of the most challenging tasks, specially in cascaded structures.

This work investigates the use of g_m/I_D model in the design of analog circuits through simulator. Simplified circuit technique is used to generate I_D/g_m plots, so that any basic SPICE like simulator can be employed. Plot of device output impedance versus length is also generated to estimate minimum geometry of the

required transistor. Finally, simple programming-based design is discussed to make an optimized design with improved accuracy. The design process comprises of the following steps.

2.1 Theory

The current–voltage relationship of a MOS can be written as:

$$I_D = k' \cdot \frac{w}{l} f(V_{\mathrm{GS}}, V_{\mathrm{DS}}, \ldots, V_T) \tag{1}$$

Above equation has two important characteristics. One, drain current I_D can be scaled by scaling the device width (w) if other parameters remain constant and it is independent of technology node. This simply means, maintaining bias and other parameters constant, and connecting devices in parallel will simply add their drain currents. Second, transconductance of the device ($g_m = \delta I_D/\delta V_{\mathrm{GS}}$) is found to be:

$$g_m = k' \cdot \frac{w}{l} f'(V_{\mathrm{GS}}, V_{\mathrm{DS}}, \ldots, V_T) \tag{2}$$

which is gain found to be scalable, provided other parameters are constant. In other words, if we connect N devices with identical bias condition but of different width w_i in parallel, overall g_m of the composite device can be written as

$$g_m = g_{m1} + g_{m2} + \cdots = \sum g_{mi} \tag{3}$$

Above two points can be summarized as follows. When multiple devices of identical gate length are connected in parallel, both current and transconductance scale up (down) equally. Dividing (1) by (2) we get,

$$\frac{I_D}{g_m} = \frac{f(V_{\mathrm{GS}}, V_{\mathrm{DS}}, \ldots, V_T)}{f'(V_{\mathrm{GS}}, V_{\mathrm{DS}}, \ldots, V_T)} \tag{4}$$

And it is independent of device size and becomes function of bias voltages applied across different terminals. In other words,

$$\left.\frac{I_D}{g_m}\right|_{w1} = \left.\frac{I_D}{g_m}\right|_{w2} = \left.\frac{I_D}{g_m}\right|_{wN} = \phi(V) \tag{5}$$

To elaborate this issue, we have calculated g_m/I_D using α power model [9–11], where drain current is expressed as

$$I_D = k' \frac{w}{l} (V_{GS} - V_T)^{\alpha} \quad [\alpha = 1.3 - 2] \tag{6}$$

Therefore, $g_m/I_D = \alpha/(V_{GS} - V_T)$, clearly depends only on V_{GS}, where α, V_T could be treated as constant.

To understand its implication, consider the I_D–V_{GS} plot of a reference device shown in Fig. 1. We are required to find the relative width of a device which will operate at a bias current of $I_D(\max) = I_{D2}$ and offer a $g_m = g_{m2}$ which could provide desired amplification. Therefore, we are required to find out the operating point of the reference device where it will have an $I_D = I_{D1}$ with $g_m = g_{m1}$ such that when device is scaled by k, the scaled device ($w2 = kw1$) will operate at $I_D(\max) = I_{D2} = kI_{D1}$ and offer $g_{m2} = kg_{m1}$.

Let us summarize the steps to be followed to design an amplifier of gain A_v. From the given specifications, we need to find out (i) maximum drain current permissible (from P_D, SR, or UGF, etc.) (ii) the required load impedance R_L (from output DC bias point, output swing, etc.) then (iii) g_m required to achieve desired gain A_v and lastly calculate the ratio of drain current to required transconductance (I_D/g_m). We now take a reference device and plot its I_D/g_m ratio under varying bias. In this plot, we have to locate the bias point (I_D or V_{GS}) where desired I_D g_m ratio is available. Scaling this device by k, where

$$k = \frac{I_D(\max)}{I_{D1}} \tag{7}$$

will give the dimension of the amplifying device. When I_D/g_m (or g_m/I_D) is plotted with respect to V_{GS}, we need to measure its I_{D1} at the same V_{GS} and use (7) to find the required device.

In case the ratio k is found abnormally large, which could happen if I_{D1} is small or V_{GS1} is close to V_T, designed amplifier will operate near subthreshold which may not return a reliable design. In such case, it is suggested to lower the g_m requirement and increase R_L (if permissible). Alternatively, one may use other I_D/g_m reference plots of devices of higher gate length l.

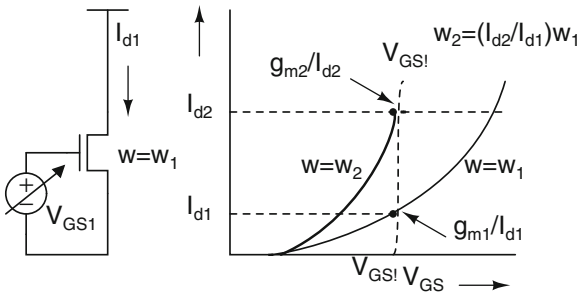

Fig. 1 Generation of (i) $I_D - V_{GS}$ data (ii) at V_{GS1}, $g_{m1}/I_{D1} = g_{m2}/I_{D2}$

3 Generation of I_D/g_m Plots

This section describes how to generate I_D/g_m plots using simulator. Plenty of literature on this matter is available on web, and plotting technique exploits waveform manipulation tools generally available from advanced simulators like cadence. However, basic SPICE like freely downloadable simulators do not support such manipulation of plots and it becomes quite difficult to generate where I_D has to be divided by g_m under varying bias conditions.

Most preferred approach to calculate I_D/g_m ratio would be with the help of simple computer program (or SCILAB/MATLAB) which can manipulate $I_D - V_{GS}$ data easily. In this technique, simulator is required to generate a datafile where I_D as function of V_{GS} is stored by sweeping V_{GS}. Once the table of data is available, g_m can be calculated as

$$g_m = \frac{I_D(i+1) - I_D(i)}{V_{GS}(i+1) - V_{GS}(i)} \quad \text{and} \quad \frac{I_D}{g_m} = \frac{I_D(i)[V_{GS}(i+1) - V_{GS}(i)]}{I_D(i+1) - I_D(i)} \tag{8}$$

MATLAB/SCILAB can easily manipulate *I–V* data of reference device and plot I_D/g_m as a function of either I_D or V_{GS} based on (8). Alternatively, if we wish to plot it directly in simulator, we must compute (8) while running DC sweep. To carry out the computation, we have separated 3 factors in (8). We propose to compute third factor assuming other two terms (or their ratio) are known. To appreciate this, let us rewrite (8) as follows.

$$\frac{I_D}{g_m} = \frac{(I_{D2} + I_{D1})}{2} \frac{[V_{GS2} - V_{GS1}]}{[I_{D2} - I_{D1}]} \tag{9}$$

Let us assume we can vary I_D in a manner such $I_{D1} = (1-\delta)\cdot I$ and $I_{D2} = (1+\delta)\cdot I$ so that $(I_{D2} + I_{D1})/(I_{D2} - I_{D1}) = 1/\delta$. Under this condition, I_D/g_m can be written as

$$\frac{I_D}{g_m} = \frac{1}{2\delta}(V_{GS2} - V_{GS1}) \tag{10}$$

If $\delta = 0.005$, I_D/g_m becomes 100 times difference between two gate–source voltages driven by current having small differential drain current. A schematic to plot I_D/g_m is shown in Fig. 2 where two controlled sources are used to drive two NMOS. Estimation of I_D/g_m could be done from differential gate–source voltages $(V_{GS1} - V_{GS2})$. One may use current ramps $(I(t) = mt \pm \delta t)$ in place of controlled sources to achieve similar plot.

A better way of computing g_m/I_D is to use a *logarithmic* amplifier. In this approach, drain current (I_D) of the reference device is applied to a log amplifier and then output current is differentiated in time domain using a simple RC differentiator. Mathematically stated,

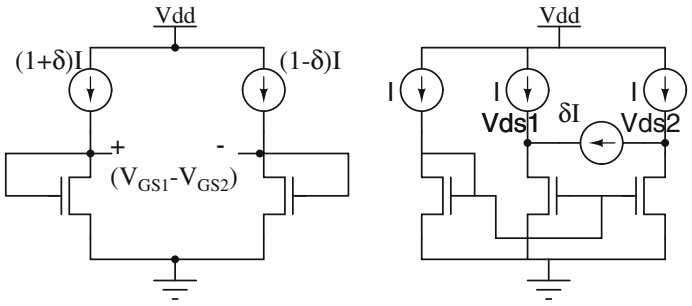

Fig. 2 Generation of (i) I_D/g_m plot (ii) g_{ds} plot for amplifier design

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\delta I_D}{\delta V_{GS}} = \frac{\delta(\ln I_D)}{\delta V_{GS}} \tag{11}$$

4 Amplifier Design

In this section, we explain the design procedure of a CS amplifier with specifications given as follows: DC gain $A_v = 10$, UGF = 1 MHz, power dissipation = 1 mW, $C_L = 5$ pF, $V_{DD} = 1.8$ V, etc. Following basic steps [2], one can find out the DC bias current and load resistance which meet the gain and other requirements. Let us assume that the required value of DC bias current is (I_D = 20 µA) and $R_L = 45$ K. Ignoring g_{ds}, we get required $g_m = A_v/R_L = 222$ µA/V. From the I_D/g_m plot (Fig. 3) of a reference device of w/l = 240/180 nm, we find desired I_D/g_m at V_{GS1} = 428 mV, at I_{D1} = 4.42 µA. Thus, amplifying device needs to be scaled by 4.5x (=20/4.42) to have desired g_m at drain current of 20. Finally, when amplifier is simulated using the projected device, a voltage gain of 7.8 is measured.

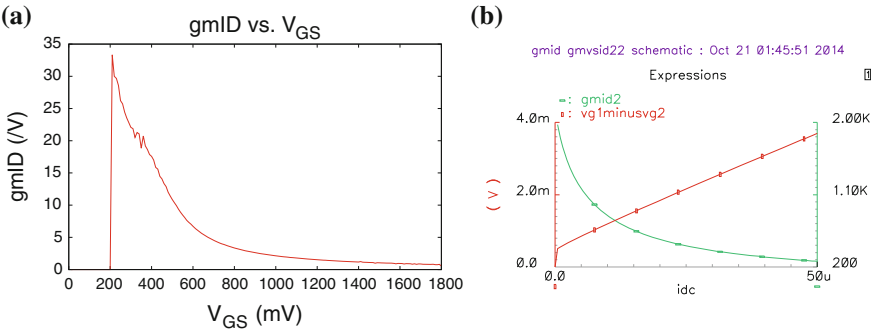

Fig. 3 **a** g_m/I_D plot using program. **b** I_D/g_m measurement using schematic

The deviation from the expected value is due to the fact that we had neglected the effects of r_o in gain calculation ($A_v \propto R_L \parallel r_o$) and approximations involved in I_D/g_m measurement. The ratio plotted using the schematic is actually $I_D/(g_m + g_{ds})$. More investigation on this is under process.

4.1 CS Amplifier with Current Source Load

Now, we turn our attention to the design of a CS amplifier with a PMOS current source load. The procedure is simple when we employ a simulator to measure the output impedance accurately. To measure g_{ds} or r_o, we use a setup where two identical devices with same gate bias are driven by $V_D = (0.5V_{DD} \pm 50\,\text{mV})$ and their differential I_D (ΔI_D) is measured. Thus, $g_{ds} = 10 \times \Delta I_D$. Such plots are generated for different lengths. To find out the desired length of the load to achieve desired r_o, required length of the device is adjusted using $r_{o1}/l_1 = r_{o2}/l_2$. If r_o measured from simulation is less than the desired R_L, we need to scale up the length of the device proportionately. On the other hand, if the device r_o is higher, we expect more gain from the designed amplifier. However, one may redesign the circuit with lower current and obtain a low-power design solution. Same approach may be used if load device r_o is smaller than desired by scaling down current, provided it satisfies other specifications like slew rate.

5 Conclusion

In this paper, an extremely simple design methodology for analog circuits is discussed. Besides being technology independent, it is also free from complex mathematical expressions. Analog designers with less experience can also design opamps in a short time using the proposed approach. Being directly based on the simulator, which uses state-of-the-the-art MOSFET models like BSIM, the results obtained from this method are highly accurate. In this work, design of simple amplifiers for a given specification is described to validate the method. All the design formulations have been tested in UMC 180 nm CMOS process.

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