A 2 Dot 1 Electron Quantum Cellular Automata Based Parallel Memory

Mili Ghosh, Debarka Mukhopadhyay and Paramartha Dutta

Abstract In the present scope, a new design methodology of parallel memory is offered. It is designed using 2 dot 1 electron Quantum-Dot Cellular Automata (QCA) paradigm. This methodology ensures better efficiency and high degree of compactness. One bit design methodology can be extended to design multiple bit parallel memory. Here we present 2 bit memory using 2 dot 1 electron QCA.

Keywords Parallel memory · 2 dot 1 electron QCA · Loop · n bit memory

1 Introduction

High speed and integrated circuitry are treated as the major requirement of digital industry. CMOS technology provides all these features with some added benefits. Thus it rules the digital industry from a past few decades. But the recent advancement in the digital industry due to the emergence of nanotechnology and nano scale devices threatens the existence of CMOS technology in the world of nano scale devices. CMOS technology is going to achieve its scaling limits in the near future. CMOS technology possesses some limitations in nano scale designs. Some of these limitations are off state leakage current, dimensional restriction, degraded switching performance etc. This leads to an urge of highly efficient nanotechnology offering cost optimum designs. QCA is one of the most promising

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alternative to the CMOS technology. The design methodology of the memory unit is based on the design proposed in [1]. This paper supplements implementation of the design proposed in it. But in the present scope we implemented this using 2 Dot 1 electron QCA. The rest of the paper is organized in the following manner. Section 2 presents the basics of 2 Dot 1 electron QCA. Section 3 proposes the advantages of 2 Dot 1 electron QCA designs. In Sect. 4, the previous reportings in this domain has been briefly discussed. Section 5 presents the 2 Dot 1 electron QCA implementation of the design and Sect. 6 determines the output states of the proposed design. In Sect. 7 the stability and compactness of the proposed design have been analysed. The design methodology of the memory is then compared with the existing designs in Sect. 8. Conclusion is drawn in Sect. 9.

2 Basics of 2 Dot 1 Electron QCA

QCA concept is based on the concepts of cells and quantum dots. Quantum dots are capable of containing free electrons which can tunnel between the quantum dots. The cell configuration is used to represent the binary information. The most common form of QCA is 4 Dot 2 electron QCA and it has been well explored in [2, 3]. 2 Dot QCA cells can align either vertically or horizontally as shown in Fig. 1. The basic constructs of 2 Dot 1 electron QCA consists of binary wire, inverter, majority voter gate and planar wire crossing as shown in Figs. 1c, d, 2 and 4 respectively (Fig. 3).

2.1 Clocking Mechanism

The QCA clocking is a bit different from conventional CMOS clocking. It is basically a quasi adiabatic four phase clocking mechanism. This type of clock is used in QCA to control the movement of channel electron and to supply energy to weak input signals. QCA clock consists of four phases: switch, hold, release and relax [4, 5]. At the beginning of switch phase the electrons are latched into dots with minimum energy. During the switch phase electrons gain extra energy from applied clock. During hold phase electrons obtain enough energy to surpass the capacitive barrier. During release phase electrons dissipate energy to the environment and at the end of this phase the electrons will latch at the other dots. During relax phase electrons will be confined into the dots with minimum energy. So, during this relax phase the cells in a clock zone will act as input for the next zone cells. Each and every QCA architecture is in general divided into four clocking zones and each clocking zone is $\pi/2$ out of phase with its previous zone as shown in Fig. 5a.

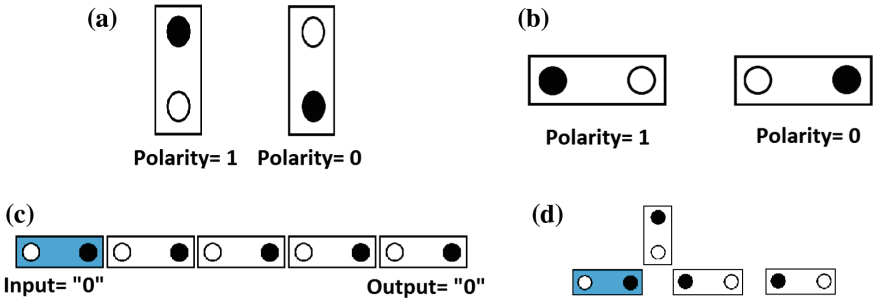


Fig. 1 Binary encoding in 2 dot QCA cell **a** with vertical alignment and **b** with horizontal alignment and **c** 2 Dot 1 electron QCA wire and **d** inversion by oppositely aligned cell

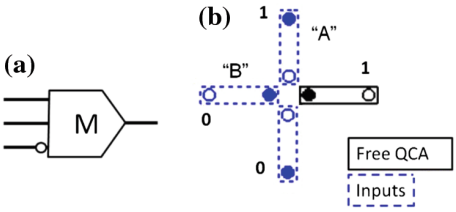
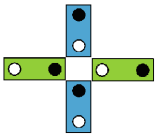


Fig. 2 Majority voter gate **a** schematic representation and **b** QCA implementation

(i) Inverting (ii) Non-inverting (iii) Non-inverting (iv) Inverting

Fig. 3 Inversion by corner cell placement

Fig. 4 Planar crossing of wires



3 Advantages of 2 Dot 1 Electron QCA

2 Dot 1 electron QCA provides all the benefits of QCA structures over conventional CMOS technology along with advantages over the 4 Dot 2 electron QCA counterpart. The advantages of 2 Dot 1 electron QCA over the 4 Dot 2 electron QCA are enlisted as following:

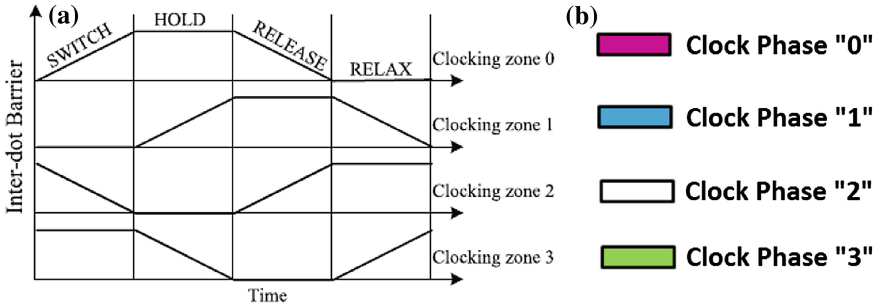


Fig. 5 **a** 2 dot QCA clocking and **b** colour code of different clock phases

1. The 4 Dot 2 electron QCA consists of 4 quantum dots and 2 electrons. Thus there are six possible configurations among which four are ambiguous [6]. But as the name suggests, 2 Dot 1 electron QCA cell consists of 2 quantum dots and 1 free electron. Thus there are exactly two cell configurations both being valid.
2. For any logic circuitry the number of quantum dots and free electron in 2 Dot 1 electron QCA is halved from that of the 4 Dot 2 electron QCA.

4 Previous Reportings in this Domain

This domain has been vastly explored using 4 Dot 2 electron QCA. Design of memory unit using 4 Dot 2 electron has been reported in [7–10]. H-memory structure, line based memory, loop based memory and parallel memory units have reported. But all of the said reportings are done in the field of 4 Dot 2 electron QCA. Here we will discuss one of the previous work reported in [10] which is the base of our present work.

In [10], a parallel memory unit design along with 1 bit and 2 bit serial memory designs. Our prime focus is on the parallel memory unit. As shown in Fig. 6a the design consists of two AND gates and one 2 × 1 multiplexer. The major signals used by the memory unit are *RowSelect*, $\overline{Rd}/Wt$, *Input*. The *Rowselect* input behaves as a memory chip selector and the $\overline{Rd}/Wt$ is used to signify whether the memory unit will be used for either *Read* or *Write* operation. If the desired operation is a read operation then the previous data is retained using a feedback loop and if the desired operation is a write operation then the new data input is stored in the memory unit. It is well defined using Fig. 6a.

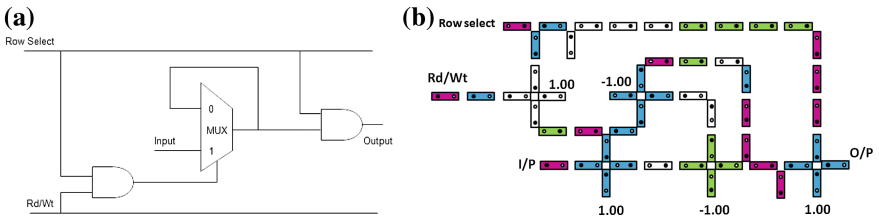


Fig. 6 **a** Schematic diagram of the parallel memory unit and **b** parallel memory implementation in 2 dot 1 electron QCA

5 Proposed Design

The proposed design is based on the block diagram as indicated in Fig. 6a. The design has been implemented using 2 Dot 1 electron QCA. 2 Dot 1 electron QCA has some basic advantages over the 4 Dot 2 electron QCA as discussed in Sect. 3. The design consists of two AND gates and one 2 × 1 MUX. The AND gates are implemented in 2 Dot 1 electron QCA architecture using two majority voter gates and the MUX is implemented using three majority voter gates. At first a one bit parallel memory design has been implemented using 2 Dot 1 electron QCA as shown in Fig. 6b. The memory unit design shown in Fig. 6b can be used to design higher order parallel memory in 2 Dot 1 electron QCA architecture. To design *n*-bit parallel memory in 2 Dot 1 electron QCA, we need to use *n* such parallel memory unit as shown in Fig. 6b. The *RowSelect* and $\overline{Rd}/Wt$ must be common for all the *n* units. In Fig. 7 a 2-bit parallel memory unit design using the said principle is shown.

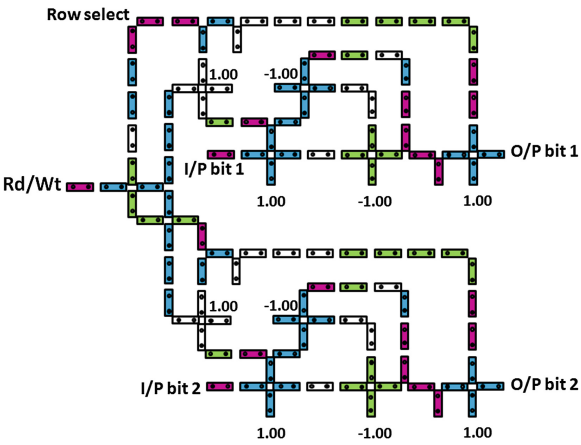


Fig. 7 2-bit parallel memory implementation in 2 dot 1 electron QCA

6 Determination of Output State of the Proposed Design

The field of 2 Dot 1 electron QCA is emerging comparatively with a slow speed as there is no open source simulator of 2 Dot 1 electron QCA available such as QCA Designer [11] of 4 Dot 2 electron QCA. Thus, the proposed design in 2 Dot 1 electron QCA is verified using potential energy calculations as available in [3]. The potential energy between two point charges is

$$U = Kq_1q_2/r \tag{1}$$

$$Kq_1q_2 = 9 \times 10^{-9} \times (1.6)^2 \times 10^{-20} \tag{2}$$

$$U_T = \sum_{t=1}^{n} U_t \tag{3}$$

where U is the potential energy, q_1, q_2 are the point charges, K is the Boltzman constant and r is the distance between the two point charges. U_T is the total potential energy for a particular electron position for all of its neighbour electrons. Quantum dots contains induced positive charge. Electrons always latch at a position with minimum potential energy. Thus potential energy at each possible electron position is evaluated. Figure 8 presents the cell numbering of the proposed parallel memory design with 2 Dot 1 electron QCA. The potential energy calculations are shown in Table 1. In Fig. 9, it is shown that the 2-bit parallel memory consists of two parallel memory units as justified in Table 1. Both the units can be justified in the similar manner. The polarity of the long array of likely oriented cells are determined by the property of binary wire.

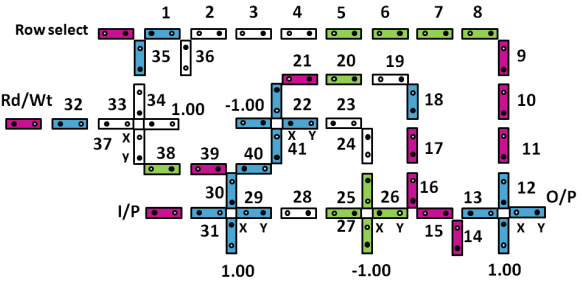


Fig. 8 A parallel memory unit design with cell positions

Table 1 Output state of parallel memory unit design

Cell	Electron position	Total potential energy	Comments
1	–	–	Input cell with polarity *RowSelect*
35, 34	–	–	Attains the polarity of cell input *RowSelect* according to corner placement shown in Fig. 3(iii)
36	–	–	Attains the inverse polarity of cell 1
32, 33	–	–	Attains the inverse polarity of cell Rd/Wt
2	–	–	Attains the inverse polarity of cell 36
3, 4, 5, 6, 7, 8	–	–	Attains the polarity of cell 2
9, 10, 11, 12	–	–	Attains the polarity of cell 8 according to corner placement shown in Fig. 3(iii)
37 37	x y	3.33×10^{-20} J 0.54×10^{-20} J	Electron will latch at position y due to less energy
38, 39, 30	–	–	Attains the polarity of cell 37
29 29	x y	6.75×10^{-20} J 0.3×10^{-20} J	Electron will latch at position y due to less energy
28, 27	–	–	Attains the polarity of cell 29
22 22	x y	-13.41×10^{-20} J -1.38×10^{-20} J	Electron will latch at position x due to less energy
23	–	–	Attains the polarity of cell 22
24, 25	–	–	Attains the polarity of cell 23 according to corner placement shown in Fig. 3(iii)
26 26	x y	-13.41×10^{-20} J -1.38×10^{-20} J	Electron will latch at position x due to less energy
16, 17, 18	–	–	Attains the inverse polarity of cell 26 according to corner placement shown in Fig. 3(i)
19, 20, 21	–	–	Attains the polarity of cell 18 according to corner placement shown in Fig. 3(iii)
15	–	–	Attains the polarity of cell 16 according to corner placement shown in Fig. 3(ii)
14	–	–	Attains the polarity of cell 15 according to corner placement shown in Fig. 3(iii)
13	–	–	Attains the inverse polarity of cell 14 according to corner placement shown in Fig. 3(iv)
O/P O/P	x y	6.75×10^{-20} J 0.3×10^{-20} J	Electron will latch at position y due to less energy

7 Analysis of Proposed Design

Two important measures of any design in 2 Dot 1 electron QCA are the effective area of the design and the stability of the design.

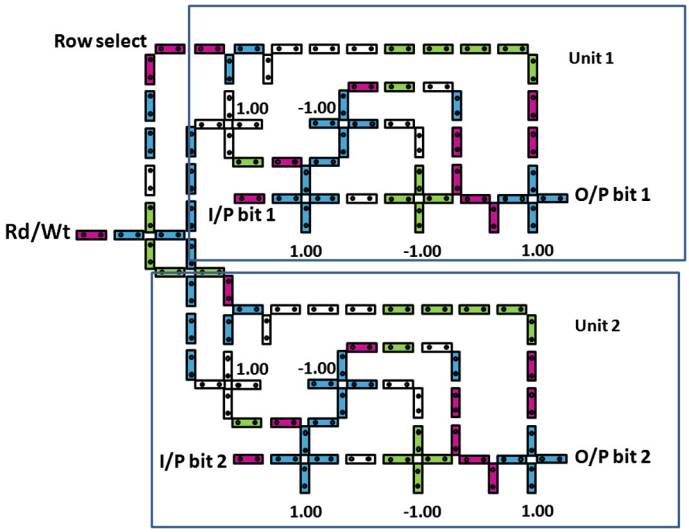


Fig. 9 2-bit parallel memory design with cell positions

7.1 Effective Area

The 2 Dot 1 electron QCA cells are rectangular in shape. Let us say the size of a 2 Dot 1 electron QCA is of size $a \times b$. As shown in Fig. 6b the parallel memory unit in 2 Dot 1 electron QCA is constructed using 48 such cells. So, the effective area of the design is $48ab$ and the area covered by the design is $60ab$. So, the area utilization ratio of the design is 4:5. Similarly the effective area ratio of the 2-bit parallel memory design is 113:156.

7.2 Stability Measure

Stability of any design has a significant contribution in judging the acceptance of that particular design. The stability of any design in 2 Dot 1 electron QCA can be ensured if the following conditions are met:

1. Each and every input signal of a majority voter gate must reach the gate at the same time with same strength.
2. The output of a majority voter gate must be taken off at the same clock phase or at the next clock phase.
3. Every cell of a majority voter gate must be at the same clock.

As we can see in Fig. 6b, the design satisfies all the constraints and hence ensures stability.

Table 2 Comparison of existing parallel memory unit design in 4 dot QCA with the proposed design in 2 dot QCA

	Parallel memory unit design in [10]	Proposed parallel memory unit design
Number of cells	104	48
Compactness of design (%)	34	80
Energy required to run	Relatively higher amount of energy needed as there are 208 number of electrons	Lesser amount of energy required as there are 96 number of electrons

8 Comparative Study

This section will give a comparative analysis of the proposed design in 2 Dot 1 electron QCA with the existing 4 Dot 2 electron QCA design as proposed in [10]. As seen in Sect. 3, the 2 Dot 1 electron QCA exhibits some beneficiary properties which minimizes the energy requirement as well as the energy dissipation of a logic construct. The comparative study is explained in Table 2.

9 Conclusion

In this article, a design methodology of parallel memory has been proposed using 2 Dot 1 electron QCA. Further, it is shown that how this memory unit can be used to construct *n*-bit parallel memory and an implementation of 2-bit parallel memory is given. Each of the designs are justified using potential energy calculations. Here, also we gave a brief analysis of the proposed design with respect to stability and effective area.

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