A Novel Hardware/Software Partitioning Technique for System-on-Chip in Dynamic Partial Reconfiguration Using Genetic Algorithm

Janakiraman N. and Nirmal Kumar P.

Abstract Hardware/software partitioning is a common method used to reduce the design complexity of a reconfigurable system. Also, it is a major critical issue in hardware/software co-design flow and high influence on the system performance. This paper presents a novel method to solve the hardware/software partitioning problems in dynamic partial reconfiguration of system-on-chip (SoC) and observes the common traits of the superior contributions using genetic algorithm (GA). This method is stochastic in nature and has been successfully applied to solve many non-trivial polynomial hard problems. It is based on the appropriate formulation of a general system model, being therefore independent of either the particular co-design problem or the specific partitioning procedure. These algorithms can perform decomposition and scheduling of the target application among available computational resources at runtime. The former have been entirely proposed by the authors in previous works, while the later have been properly extended to deal with system-level issues. The performance of all approaches is compared using benchmark data provided by MCNC standard cell placement benchmark netlists. This paper has shown the solution methodology in the basis of quality and convergence rate. Consequently, it is extremely important to choose the most suitable technique for the particular co-design problem that is being confronted.

Keywords Hardware/software partitioning · Genetic algorithm · Dynamic partial reconfiguration · System-on-chip

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1 Introduction

Hardware/software partitioning is a method of dividing a complex heterogeneous system into hardware co-processor functions and its compatible software programs. It is a prominent practice that can realize results greater than the software-only or hardware-only solutions in system-on-chip (SoC) design. This technique can improve the system performance [1] and reduce the total energy consumption [2]. The proposed partial dynamic reconfiguration method does not depend on any tool. It uses a set of algorithms to detect crucial code regions, compilation/synthesize of hardware/software modules, and updating of communication logic. Hence, it could tune up the system to give full efficiency without disruption of other SoC-related operations. Here, the genetic algorithm (GA) is used for optimization process. This is essential in system-level design, since decision-making process affects the total performance of system. This paper presents a novel system partitioning technique with in-depth analysis. The paper is organized as follows. Section 2 briefs about the previous works in this field. Section 3 presents the proposed system model for partitioning problem. Section 4 gives the results and its analysis. Section 5 concludes the paper and discusses about the future work. Last section provides the list of references.

2 Related Works

When compared to dynamic partitioning using standard software, the run-time (or) partial dynamic reconfigurable systems had attained superior performance with manually specified predetermined hardware regions. Multiple choices of preplanned reconfigurations were rapidly executed in a run-time reconfigurable system using PipeRench architecture [3] and dynamically programmable gate arrays (DPGA) [4]. The binary-level partitioning technique [5] was provided a good solution compared to source-level partitioning methods due to the functionality of any high-level language and software compiler. Since the satisfaction of performance was not considered for the cost function of this system, it may be failed to find out local minima. A mapping technique for nodes and hardware/software components was developed in [6] called GCLP algorithm. The hardware cost was minimized by the incorporation of hill-climbing heuristic algorithm with the hardware/software partitioning algorithm [7].

3 System Model for Partitioning

The problem resolution requires the system model definition to represent the important issues in the hardware/software co-design for a specific problem [8]. The system partitioning problem model is represented by the task graph (TG) flow diagram. TG is a model of directed and acyclic graph (DAG) flow with weight vectors. Formally,

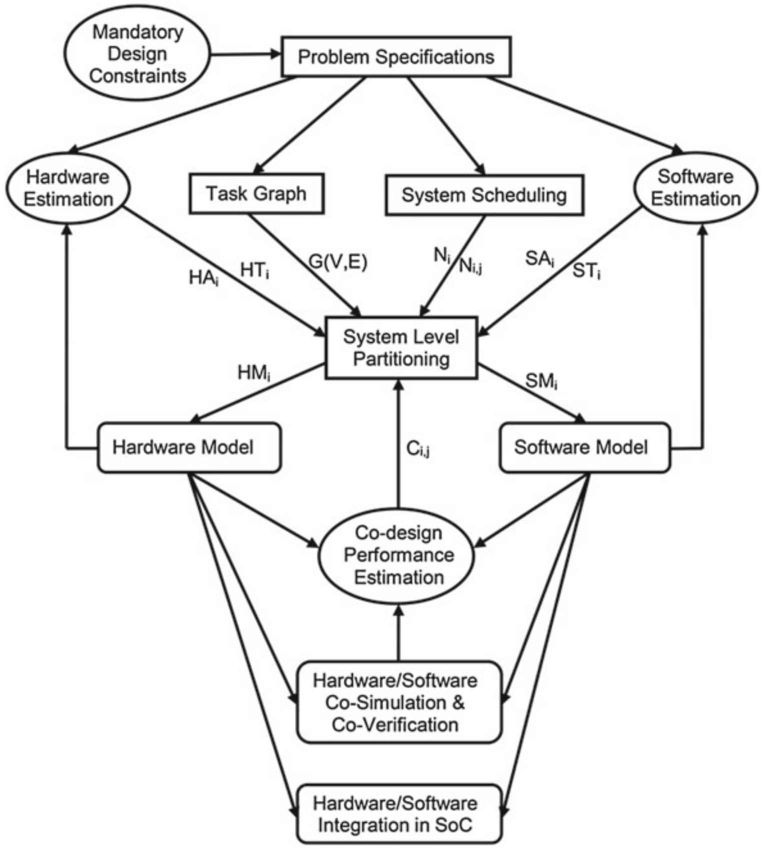
Mandatory Design Constraints
Problem Specifications
Hardware Estimation
Task Graph
System Scheduling
Software Estimation
HA_i
HT_i
G(V,E)
N_i
N_i,j
SA_i
ST_i
System Level Partitioning
HM_i
SM_i
Hardware Model
C_i,j
Software Model
Co-design Performance Estimation
Hardware/Software Co-Simulation & Co-Verification
Hardware/Software Integration in SoC

Fig. 1 System model for partitioning

it is defined as $G = (V, E)$, where 'V' represents the nodes and 'E' represents the edges. The flow direction is represented by each edge. Due to reducing the complexity of TG, it can be modified as one starting node and one ending node. Figure 1 represents the overview of the partitioning procedure. Design constraints and design specifications are given as the input to the partitioning process as a high-level specification language. The nodes can act as giant pieces of information like tasks and processes of coarse granularity or tiny types like instructions and operations of fine granularity approach.

After the system space estimation, every node is tagged with some attributes. Giant pieces of data for a node ($V_{\mathrm{i,j}}$) are represented by 5 attributes as follows:

(1) Hardware area ($\mathrm{HA}_{\mathrm{i,j}}$).
(2) Hardware implementation time ($\mathrm{HT}_{\mathrm{i,j}}$).
(3) Software memory size ($\mathrm{SS}_{\mathrm{i,j}}$).
(4) Software execution time ($\mathrm{ST}_{\mathrm{i,j}}$).

(5) The average execution time in numbers $(N_{\mathrm{i,j}})$.

Shortly,

$$\text{Hardware module }\left(\mathrm{HM}_{\mathrm{i,j}}\right) = \left(\mathrm{HA}_{\mathrm{i,j}}\right) + \left(\mathrm{HT}_{\mathrm{i,j}}\right) + (N_{\mathrm{i,j}})$$
$$\text{Software module }\left(\mathrm{SM}_{\mathrm{i,j}}\right) = \left(\mathrm{SS}_{\mathrm{i,j}}\right) + \left(\mathrm{ST}_{\mathrm{i,j}}\right) + (N_{\mathrm{i,j}})$$

Communication values $(C_{\mathrm{i,j}})$ of every node are represented by three components as follows:

(1) Transfer time $(\mathrm{TT}_{\mathrm{i,j}})$
(2) Synchronization time $(\mathrm{SynT}_{\mathrm{i,j}})$
(3) The average communication time in numbers $(M_{\mathrm{i,j}})$

Shortly,
$$\text{Communication value of node }\left(C_{\mathrm{i,j}}\right) = \left(\mathrm{TT}_{\mathrm{i,j}}\right) + \left(\mathrm{SynT}_{\mathrm{i,j}}\right) + (M_{\mathrm{i,j}})$$

$$C_{\mathrm{i,j}} = \frac{(N_i * \Delta\mathrm{TT}_i) + \left(N_j * \Delta\mathrm{TT}_j\right) + (\mathrm{SynT}_{\mathrm{i,j}})}{(\mathrm{HT}_i) + (\mathrm{HT}_j)}$$

where $(\Delta\mathrm{TT}_i) = (\mathrm{ST}_i) - (\mathrm{HT}_i)$ and $(\Delta\mathrm{TT}_j) = \left(\mathrm{ST}_j\right) - \left(\mathrm{HT}_j\right)$.

Efficiency of the hardware/software system partitioning process is based on the target architecture and its mapping technique. Hence, this work considers the 'Dynamically Reconfigurable Architecture for Mobile Systems' (DReAM) as target architecture. Execution of hardware and software processes should be concurrently in the standard processor and the application-specific co-processor. This partitioning process concludes the assignment of modules to implement the hardware and software stages, implementation schedule (timing), and the communication interface between software and hardware modules. In general, this partitioning solution can be validated by the measurement of eminent attributes like performance and cost parameters. Hence, this paper used as three quality attributes related to design elements as follows:

(1) The estimated hardware area is A_E, and the maximum available area is A.
(2) The estimated design latency is T_E, and the maximum allowed latency is T.
(3) The estimated software (or) memory space is M_E, and the maximum available space is M.

Static-list scheduling method is used for the scheduling process [9]. It is a subtype of resource-constrained scheduling algorithm. This scheduler considers the timing estimation of every vertex and its interconnections. This scheduler unit provides the design latency (T_E) and the cost of communication for hardware–software co-design. Based on the hardware and software implementations, another four parameters are considered for co-design realization.

When the entire system is implemented in hardware,

(1) The minimum design latency is MinT.
(2) The maximum hardware area is MaxA.

When the entire system is implemented in software,

(1) The maximum design latency is MaxT.
(2) The maximum memory space is MaxM.

These parameters are used to create the bounding constraints for the design space. $0 \leq A \leq \text{MaxA}$; $0 \leq M \leq \text{MaxM}$; $\text{MinT} \leq T \leq \text{MaxT}$.

3.1 System Operations

The design specifications are given in the format of ISPD98 benchmark suite [10] circuit netlist. This partitioning process has three stages.

In first stage, the processing of design specifications is divided into three subtasks. The first subtask is the separation of hardware (HA_i and HT_i) and software (SS_i and ST_i) estimations from the design specifications. The second subtask is to translate the design specifications into a hypergraph-based control data flow graph (CDFG) representation $G = (V, E)$. The third subtask is scheduling (N_i and $N_{\text{i,j}}$) of each operations in the CDFG with satisfaction of the design constraints and the priority of operations.

In second stage, the outputs of these three tasks are given into the system-level partitioning module through the registers. It has three functionalities. The operational-level analysis is the first process, used to classify the tasks whether it is suitable for hardware realization or software execution. Next, the allocation process is used to allocate the required supporting entities like functional units, interconnections, and storage elements for the scheduled hardware and software systems. This allocation is based on the speed constraint (i.e., parallel processing) and the area constraint (i.e., dynamic partial reconfiguration). Finally, an absolute data path is generated by integrating components in the basis of hardware and software partitions. Then, the partitioning data are given to the specific hardware (HM_i) and software (SM_i) models.

In third stage, the hardware and software models are executed separately and the outcomes are compared with their estimated values (i.e., first stage). If any controversy arises, the feedbacks are given to the second-stage process. This looping process is continued till the satisfaction of all criterions.

Next, the performance ($C_{\text{i,j}}$) of hardware–software co-design is estimated and compared with target performance metrics. If any misalignment arises, the feedback is indicated to the system-level partitioning stage. Then, the entire second and third stages are recompiled, till the achievement of target performance measures. Finally, the hardware/software co-simulation and co-verification is performed, and then, the SoC is realized.

3.2 Hardware/Software Estimation

The CDFG file is given to the input of both hardware and software estimations with the settings of target technology files and processor specifications. The hardware execution is a parallel process since the specifications are modeled in VHDL library. The software execution is a sequential process since the specifications are modeled in C code. The GA technique is used to optimize these parallel and sequential processes.

Hardware estimation is based on the high-level synthesizable components, to share the control and data path between hardware and software processes. GA is used to optimize this resource sharing process [11]. The quality measures are closely associated with performance metrics like execution, implementation, transfer, and synchronization times commonly called reaction time. This reaction time is associated with each node in each execution of local DFG. For convenient, the CDFG is split into several small DFGs called local DFGs.

The response times for

Routine statements, $T_{\mathrm{RS}} = T_{\mathrm{DFG}}$

Conditional statements, $T_{\mathrm{CS}} = \sum_n P_n T_{\mathrm{DFGn}}$;

n—Number of iterations

P_n—Probabilities of iterations of outcomes

Looping statements, $T_{\mathrm{LS}} = nT_{\mathrm{DFG}}$;

$$\begin{aligned} T_{\mathrm{CDFG}} &= F(T_{\mathrm{DFG1}}, F_{\mathrm{DFG1}}, \ldots, T_{\mathrm{DFGi}}, F_{\mathrm{DFGi}}) \\ &\quad + F(T_{\mathrm{DFG1}}, F_{\mathrm{DFG1}}, \ldots, T_{\mathrm{DFGj}}, F_{\mathrm{DFGj}}) \end{aligned}$$

$$\mathrm{MinT} = \alpha[(\mathrm{MaxA} * C_{\mathrm{i,j}}) + \sum_i T_i N_{\mathrm{i,j}}]$$

T_i—Time delay for each node

α—Co-estimation factor

$$\mathrm{MaxT} = \mathrm{MinT} + \beta \sum_i [T_i \sum_{j=1}^{R_i} N_{\mathrm{i,j}}]$$

R_i—Required components of each node 'i'

β—Constant, since MaxT is a higher-order term

F_i—Number of fixed components for each node 'i'

$$T_{\mathrm{CDFG}} = \mathrm{MinT} + \beta \sum_i [\frac{T_i}{F_i} \sum_{j=F_i+1}^{R_i} N_{\mathrm{i,j}}]$$

Register Estimation: [12]

Many input multiplexers = (i*MUXs)

State machine-based control logic is used to control lines, $\log_2 i$

ROM size, $(\mathrm{STA}^*[(1+\log_2 i)\left(\mathrm{REG}+\sum_i F_i\right)+\log_2 S])$bits

STA—Number of states
REG—Number of registers

Software estimation is based on the calculation of memory space occupied by instruction set and user-defined data types and data structures. The average queuing time for each memory access can be modeled as T_q, and the number of access is represented by N_{mem}. This calculation is necessary to estimate $(\mathrm{TT}_{\mathrm{i,j}})$ and $\left(\mathrm{SynT}_{\mathrm{i,j}}\right)$.

Hardware estimation $(T_{\mathrm{HM}}) = (T_{(\mathrm{CDFG,HM})}) + \alpha T_q (N_{\mathrm{mem,HM}})$

Software estimation $(T_{\mathrm{SM}}) = (T_{(\mathrm{CDFG,SM})}) + T_q (N_{(\mathrm{mem,SM})})$

Co-estimation $(T_{\mathrm{HM/SM}}) = \sigma(T_q) + \varphi(\frac{N_{\mathrm{mem}}}{T_q})$; where σ and φ are complex structures.

4 Analyses of Results

All the hardware/software partitioning algorithms have been experimented in a set of benchmark suites provided by ISPD’98, whose characterization is shown in Table 1. Size and values of the system graph should bound within the design space. All these examples are illustrated in the form of directed and acyclic graphs to specify the certain coarse–grain tasks. Every example has been tested in different constraints, but it always within the specified boundary conditions. The results are summarized in Table 2. These results will be analyzed from both qualitative and quantitative perspectives. The qualitative aspects will be mainly represented by the resulting cost of the solutions obtained from each method, under different constraints. The quantitative issues will be shown by means of the computation time resulting from each technique.

Table 1 Design characteristics for ISPD’98 benchmark suite

Circuit	# Cells	# Pads	# Modules	# Nets	# Pins
ibm01	12,506	246	12,752	14,111	50,566
ibm02	19,342	259	19,601	19,584	81,199
ibm03	22,853	283	23,136	27,401	93,573
ibm04	27,220	287	27,507	31,970	105,859
Ibm05	28,146	1,201	29,347	28,446	126,308

Table 2 Results acquired with the ISPD'98 examples

Example	Constraints			Genetic algorithm			
	Area (CLBs)	Time (ns)	Memory (Bytes)	A_E	T_E	M_E	**Fitness**
ibm01	121,800	10,200	52,670	118,146	9,384	46,350	0.9233
	103,080	8,670	44,770	101,637	8,020	41,189	0.9437
ibm02	154,700	12,600	55,980	140,170	11,230	49,823	1.0000
	193,375	15,750	48,980	172,104	15,435	51,429	0.9733
ibm03	171,200	14,200	48,090	154,896	12,040	38,953	1.0000
	111,280	9,230	57,708	103,521	8,769	54,823	1.0000
ibm04	182,200	15,900	56,460	173,090	14,469	62,106	0.9866
	258,724	19,239	50,814	234,597	16,546	46,749	0.9600
ibm05	198,300	16,800	62,210	180,453	13,776	58,478	0.8900
	97,167	12,432	81,495	92,309	10,940	84,755	0.9566

5 Conclusion and Future Work

In this paper, the commonly used biologically inspired optimization algorithm, which addresses the hardware/software partitioning problem for SOC designs, is implemented using clustering approach as well as their performance is evaluated. This evaluation process does not have any constraints on the cluster size and the number of clusters. Hence, this evaluation approach is quiet suitable to be used in reducing the design complexity of systems. This paper had shown how this problem can be solved by means of very different partitioning techniques at runtime of the system (dynamic partial reconfiguration). The problem resolution has been based on the definition of a common system model that allows the comparison of different procedures. These extensions have improved previous implementations, because they include some issues previously not considered. The constraints of these algorithms have been integrated into the cost function in a general and efficient way. This genetic algorithm-based dynamic partitioning technique has produced an average of 16.19 % accuracy in hardware/software partitioning compared to [13] and [14].

A future study could extend the system model to encompass other quality attributes, like power consumption, influence of communications, and the degree of parallelism. Also, the hybrid algorithms of these biologically inspired algorithms and their compilation are currently under study.

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