Analysis and Simulation of Full Adder Design using MTCMOS Technique

Richa Saraswat[1], Shyam Akashe[2], Shyam Babu[3]

[1] ECED ,ITM University Gwalior, India

[2] ECED ,ITM University Gwalior, India

[3] ECED ,ITM University Gwalior, India

richasaraswat44@gmail.com; shyam.akashe@itmuniversity.ac.in,itm.shyam @gmail.com}

Abstract. The intention of this paper is to reduce leakage power and leakage current of 1-bit Full Adder while maintaining the competitive performance with few transistors are used (transistors count 10). A new high performance 1-bit Full Adder based on new logic approach is presented in this paper. MTCMOS technique which decreases the process variation on 1-bit Full Adder, the key of MTCMOS technique is applied on 1-bit Full Adder is to reduce the operating power, leakage power and leakage current. We investigate the use Multi-threshold CMOS (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low Vth transistors for logic cells and low leakage, high Vth of transistor and show that it is particularly effective in sub threshold circuits and can eliminate performance variations with Low power. A 20ns access time and frequency 0.05GHz provide 45nm CMOS process technology with 0.7V power supply is employed to carry out 1-bit Full Adder.

Keywords: 1-bit Full Adder; MTCMOS; CMOS; Leakage Power; Leakage Current; Frequency.

1 Introduction

Adder is one of the most vital components of a CPU (central processing unit), Arithmetic logic unit (ALU), floating point unit and address generation like cache or memory access unit. On the other hand, increasing demand for portable equipments such as cellular phones, personal digital assistant (PDA), and notebook personal computer, arise the need of using area and Power efficient VLSI circuits. Low-power and high-speed adder cells are used in battery-operation based devices. As a result, design of a high-performance full-adder is very useful and vital [1]

J. C. Bansal et al. (eds.), *Proceedings of Seventh International Conference on Bio-Inspired Computing: Theories and Applications (BIC-TA 2012),* Advances in Intelligent Systems and Computing 202, DOI: 10.1007/978-81-322-1041-2_16,

One of the most well known full adders is the standard CMOS full adder that uses 28 transistors as shown in Fig.1. In this paper, we present a 1-bit full-adder circuit, which uses 10 transistor count with suitable power consumption, delay performance. The basic advantage of 10 transistors full adders are-low area compared to higher gate count full adders [2], lower power consumption, and lower operating voltage. It becomes more and more difficult and even outmoded to keep full voltage move backward and forward operation as the designs with fewer transistor count and lower power consumption are pursued [3]. In pass transistor logic, the output voltage move backward and forward may be de-graded due to the threshold loss problem Thus, attractive its presentation is significant for enhancing the overall module performance [4]-[5]. To implement probabilistic Boolean logic[6], a probabilistic gate produces a preferred value as an output that is 0 or 1 with probability p, and, hence, can produce the wrong output value with a probability (1 - p) [7]. It is supposed that probabilistic computing has potential for multimedia applications [8]. The basic disadvantage of the 10 transistors full adders are suffering from the threshold- voltage loss of the pass transistors. They all have double threshold losses in full adder output terminals [9]

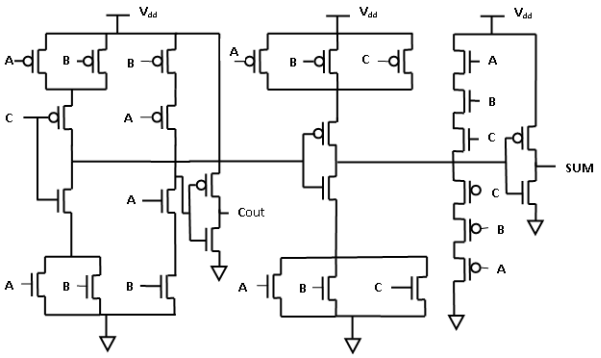

Fig.1. Schematic of conventional full adder

Multi-threshold CMOS (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low Vth transistors for logic cells and low leakage, high Vth devices as sleep transistors. To reduce the leakage in sleep mode, sleep transistors disconnect logic cells from the power supply and/or. In this technology, also called power gating, wake up latency and power plane integrity are key concerns. The schematic of power gating technique using MTCMOS is shown in Fig. 2.The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation [10].

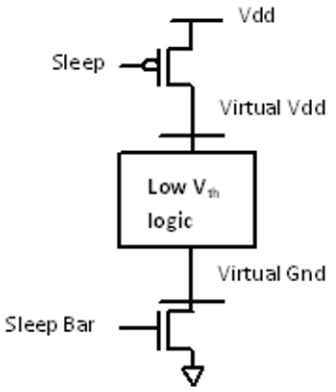

Fig.2. Power gating using MTCMOS technique

To determine the overall performance of the integrated circuits, the interconnect delay becomes the dominant factor. Since the delay of an interconnect is quadratic in its length, repeater insertion has been widely used to reduce the delay. As shown in [11] the repeaters can be optimally sized and divided to minimize the interconnect delay. The size of an optimal repeater is typically much larger than a minimum-sized repeater. To drive global interconnects, since millions of repeaters will be inserted, significant power will be consumed by these repeaters, predominantly if delay-optimal repeaters are used [12]. Several works used the extra acceptable delay for power saving in interconnects. Authors are provided investigative methods to calculate unit length power optimal repeater sizes and distances [13]. The power investigation should consider switching, leakage and short circuit correctly. This in turn increases the capacitive coupling noise on the interconnection lines, as the technology scales down wires are laid out closer to each other. This will have an effect on both delay and power consumption in interconnects. In addition to switching power on the coupling capacitances, the authors of [14] showed that the short circuit power consumption is increased indicate cantly in the being there of crosstalk noise. Therefore, one should also consider this effect in the design of power optimal repeaters. Moreover, the technology scaling has resulted in large increase in leakage current. Leakage power has grown exponentially to become a important fraction of the total chip power consumption [15]. Authors in [16] studied the applicability of MTCMOS to repeater design for leakage power saving, however they did not provide a mathematical explanation for the instantaneous optimal sizing of the sleep transistors and repeaters and the insertion length. In addition the effect of crosstalk on delay and power has not been taken into description for the optimal design.

2 1-Bit Full Adder

In this paper, we present a 1-bit full-adder circuit, with suitable power consumption, delay performance. We have simulated a 1-bit Full-adders circuit along with various 10 transistors and compared the Power dissipation, propagation delay, and other parameters. The basic advantage of 10 transistors full adders are-low area compared to higher gate count full adders, lower power consumption, and lower operating voltage. It becomes more and more difficult and even obsolete to keep full voltage move backward and forward operation as the designs with fewer transistor count and lower power consumption are pursued. In pass transistor logic the output voltage swing may be de-graded due to the threshold loss problem. That is, the output high (or low) voltage is deviated from the VDD (or ground) by a multiple of threshold voltage Vth. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. At low VDD operation, the degraded output may even cause malfunction of circuit [17]. Therefore, for designs using reduced voltage swing, special consideration must be paid to stability the power consumption and the speed. [18]. For the implementation of various 10 transistors full adder circuits we required either 4 transistors XOR circuit or 4 transistor XNOR circuit and 2-to-1 multiplexer. The schematic of 1- bit Full Adder is shown in figure 4, the output waveform is shown in figure 5.
This uses a total of 10 transistors for the implementation of following logic expressions.
Consider a 1-bit full adder. This circuit has two operands, A and B, and an input carry, Cin. It generates the sum

$$S = A \oplus B \oplus Cin \qquad (1)$$

and the output carry

$$Cout = AB + BC + AC \qquad (2)$$

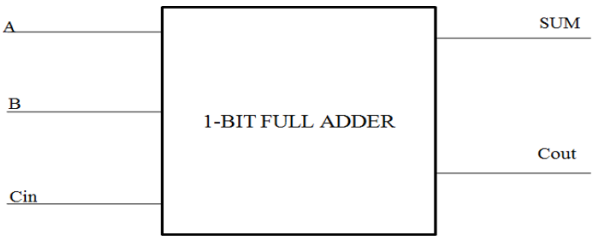

Fig.3. Symbol Diagram of 1Bit full adder

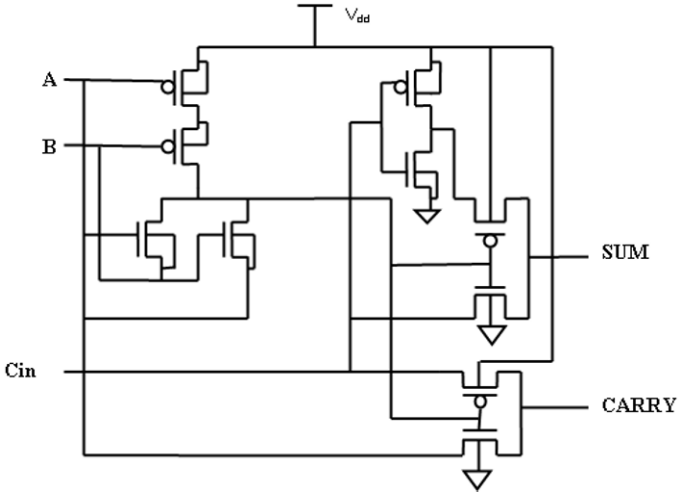

Fig.4. Schematic of 1-bit Full Adder

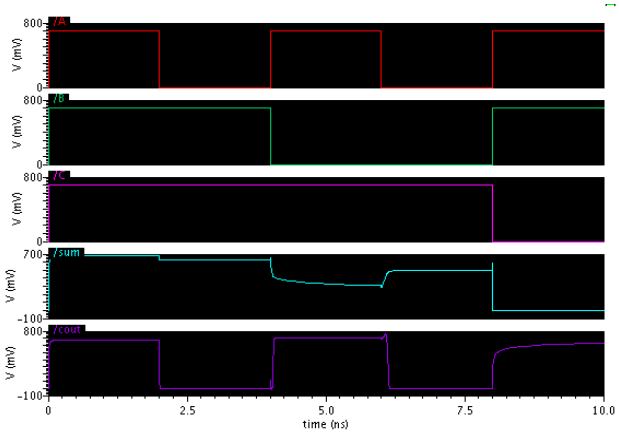

Fig.5. Output Waveform of 1-bit Full Adder

3 MTCMOS Technique Applied On 1-bit Full Adder

MTCMOS technique is applied on 1-bit Full Adder in which we uses a high Vth PMOS connected to the Vdc terminal of 1-bit Full Adder and a high Vth NMOS is connected to the ground terminal of 1-bit Full Adder. The schematic of MTCMOS applied on 1-bit Full Adder is shown in figure 5. MTCMOS is a variation of CMOS chip technology which has transistors with multiple threshold voltage (Vth) in order to optimize delay or power. The Vth of a MOSFET is the gate voltage where an inversion layer forms at interface between insulating layer (oxide) and the substrate (body) of the transistor. Low Vth devices switch faster, and are therefore useful on critical delay paths to minimize clock period. The penalty is that low Vth devices have substantially higher static leakage power. High Vth devices are used on non-critical path to reduce static leakage power without incurring the delay penalty. Typical high Vth devices reduce the static noise by 10 times compared with low Vth devices [19].The output waveform of 1-bit Full Adder using MTCMOS technique is shown in figure 6, the output waveform is shown in figure 7 ,and operating current waveform is shown in figure 8.

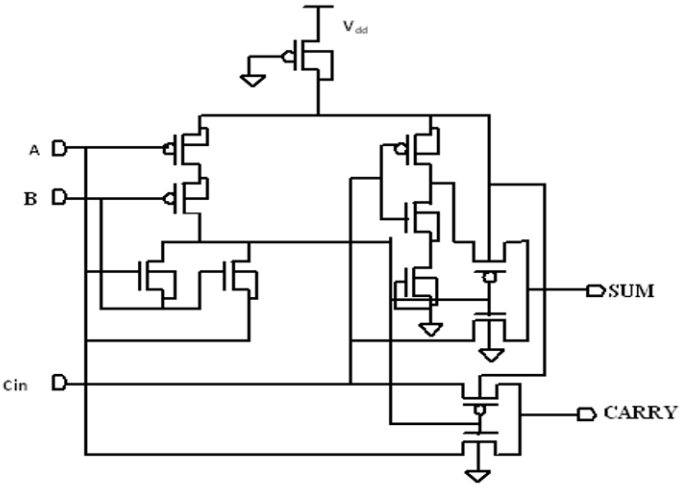

Fig.6. Schematic of 1-bit Full Adder using MTCMOS technique

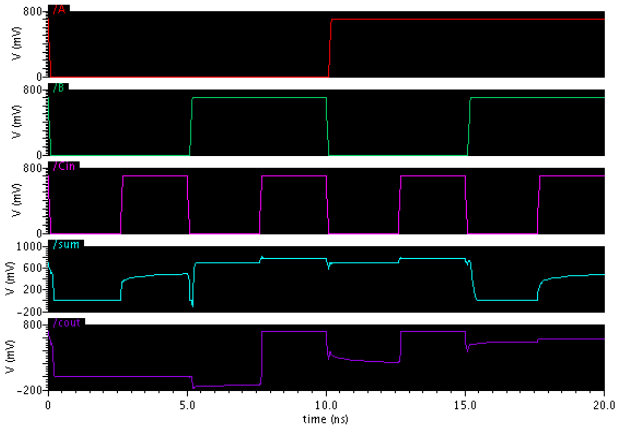

Fig.7. Output Waveform of 1-bit Full Adder with MTCMOS technique

Digital CMOS circuit may have three major sources of power dissipation namely dynamic, short and leakage power. Hence the total power consumed by every Full Adder can be evaluated using the equation 3.

$$P_{tot} = P_{dyn} + P_{sc} + P_{leak}$$

$$= CLV_{dd}Vf_{clk} + I_{SC}V_{dd} + I_{leak}V_{dd} \qquad (3)$$

Thus for low-power design the important task is to minimize CL V_{dd} V f_{Clk} while retaining required functionality. The first term P_{dyn} represents the switching component of power, the next component *Psc* is the short circuit power and P_{leak} is the leakage power. Where, CL is the loading capacitance, fClk is the clock frequency which is actually the probability of logic 0 to 1 transition occurs (the activity factor). Vdd is the supply voltage, V is the output voltage swing which is equal to Vdd; but, in some logic circuits the voltage swing on some internal nodes may be slightly less. The current I_{SC} in the second term is due to the direct path short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current I_{leak}, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. Duty cycle is also calculated in this paper for single bit full adder cell .In a periodic event, duty cycle is the ratio of the duration of the event to the total period of signal [20].

Duty Cycle (D) = τ / T

Where τ is the duration that functions is active. And T is the period of the function.

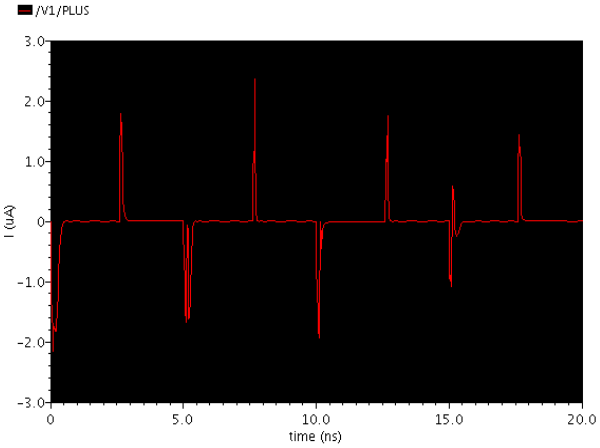

Fig.8. Operating current waveform of 1-bit Full Adder with MTCMOS

4 Simulation Result

A 1-Bit Full Adder based on MTCMOS technique have been proposed. The analysis of the simulated results confirms the feasibility of the MTCMOS technique in full adder design and shows that there is reduction of 40 to 43 percent in the value of power dissipation parameter as compared to CMOS technique at supply voltage of 0.7V. MTCMOS adders have a marginal increase in area compared to the CMOS adders; overall, we achieved the lowest power dissipation. Simulation result is measured by CANDENCE VIRTUOSO Tool .The Simulation result is summarized in TABLE 1.

Table 1. Simulated Result summary

Parameters	1-bit Full Adder	MTCMOS
Technology Used	45nm	45nm
Supply Voltage	0.7V	0.7V
Frequency Used	0.05GHz	0.05GHz
Access Time	20ns	20ns

Delay	3.94ns	2.05ns
Duty cycle	52.3 %	68.08 %
Leakage Power	1.594pW	0. 4pW
Leakage Current	652.4nA	230pA
Optimum Current	4.84 µA	73.3 nA
Optimum Power	0.53nW	2.3mW
Dynamic Current	18.02µA	1.52µA
Dynamic Power	2.086pW	1.766pW
Operating Power	51.63nW	20.03nW
Operating Current	1.804µA	2.35µA

5 Conclusion

In our investigation the 1-bit Full Adder and full adder using MTCMOS technique, we have estimated the design parameters such as operating current, operating power, leakage current, leakage power, optimum current, optimum power, dynamic current, dynamic power, delay and Efficiencies with the help of cadence virtuoso at 45nm technology. The advantage of having the same functionality with very few transistors will be beneficial in 1-bit Full Adder realization. Low Vth devices switch faster and are therefore useful on critical delay paths to minimize clock period. The penalty is that low Vth devices have substantially higher static leakage power. High Vth devices are used on non-critical path to reduce static leakage power without incurring the delay penalty. Typical high Vth devices reduce the static power by 10 times compared with low Vth devices.

References

[1] Rabaey J. M., A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, A Design Perspective, 2nd 2002, Prentice Hall, Englewood Cliffs, NJ.

[2] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan, Zhangming Zhu, Yintang Yang, "Novel Low Power Full Adder Cells in 180nm CMOS Technology", 4th IEEE Conference on Industrial Electronics and Applications, ICIEA 2009, pp 430-433.
[3] Lu Junming; Shu Yan; Lin Zhenghui; Wang Ling," A Novel 10-transistor Low-power High-speed Full adder cell", Proceedings of 6th International Conference on Solid-State and Integrated-Circuit Technology, vol-2, pp. 1155-1158,2001.
[4] Adarsh Kumar Agrawal, Shivshankar Mishra, and R. K. Nagaria, "Proposing a Novel Low-Power High-Speed Mixed GDI Full Adder Topology", accepted in Proceeding of IEEE International Conference on Power, Control and Embedded System (ICPCES), 28 Nov.-1Dec. 2010.
[5] N. M. Chore, and R. N. Mandavgane, "A Survey of Low Power High Speed 1 Bit Full Adder", Proceeding of the 12th International Conference on Networking, VLSI and Signal Processing, pp. 302-307,2010.
[6] A. Bhanu. M. S. K. Lau, K. V. Ling, V. l Mooneylll, and A. Singh, "A more precise model of noise based CMOS errors," Proceedings of DELTA, 2010, pp. 99-102.
[7] M. S K. Lau, K. V. Ling, Y C Chu, and A. Bhanu,"Modeling of probabilistic ripple-carry adders," Proceedings of DELTA, 2010, pp. 201-206.
[8] J. M. Rabaey, A. Chandrakasan, and B. Nikoli' c, Digital Integrated Circuits: A Design Perspective, 3rd ed. Prentice Hall, 2003.
[9] Shivshankar Mishra, V. Narendar, Dr. R. A. Mishra " On the Design of High-Performance CMOS 1-Bit Full Adder Circuits," Proceedings published by International Journal of Computer Applications® (IJCA)2011.
[10] Hemantha S,Dhawan A and Kar H ,"Multi-threshold CMOS design for low power digital circuits",TENCON 2008-2008 IEEE Region 10 Conference,pp.1-5,2008.
[11] H. B. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," IEEE Trans. on Electron Devices, vol. ED-32, no. 5, pp. 903–909, May 1985.
[12] G. Chen and E. Friedman, "Low power repeaters driving RC interconnects with delay and bandwidth constraints," in Proc. Of ASIC/SOC, pp. 335–339, 2004.
[13] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," IEEE Trans. on Electron Devices, vol. 49, pp. 2001–2007, Nov. 2002.
[14] H. Fatemi, S. Nazarian, and M. Pedram, "A current-based method for short circuit power calculation under noisy input waveforms," in Proc. of ASP-DAC, pp. 774-779, 2007.
[15] Semiconductor Industry Association, International Technology Roadmap for Semiconductors, 2003 edition.
[16] R. Rao, K. Agarwal, D. Sylvester, et al. "Approaches to run-time and standby mode leakage reduction in global buses," in Proc. Of ISLPED, pp. 188-193, 2004.
[17] Jin-Fa-Lin, Yin Tsung Hwang, Ming-Hwa Sheu, and Cheng-Che Ho, "A Novel High-Speed and Energy Efficient 10 Transistor Full Adder Design" IEEE Trans. Circuits Syst. I: Regular Papers, vol.54, no.5, pp.1050-1059, May 2007.
[18] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.
[19] Anis, M.; Areibi, Mahmoud, Elmasry, (2002). "Dynamic and leakage power reduction in MTCMOS circuits". *Design Automatio Conference, 2002*. Proceedings **39th**, pp 480–485
[20] . J. Rodrigues, O. C. Akgun, and V. Owall, "A <1 pJ sub-VT cardiac event detector in 65 nm LL-HVT CMOS," in Proc. VLSI-SoC, June 2010.