Analyzing and minimization effect of Temperature Variation of 2:1 MUX using FINFET

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Abstract. —This paper proposes a Transmission gate based 2:1 MUX using FINFET (Fin Shaped Field Effect Transistor) using 45nm CMOS technology .The mobility was enhanced in devices with taller fins due to increase tensile stress. We have estimated the Optimum Power, Optimum Current, Leakage Power, Leakage Current, Operating Power and Operating Current in different voltage supply 0.3V, 0.5V and 0.7V at different temperature such as 10°C, 27°C and 50°C respectively. We have also calculated Duty cycle are 67.41%, 54.48% and 10.96%, 45.99%, rise time are 0.277ps, 0.0013ps and 0.534ps, 0.003ps, Bandwidth are 3.502GHz, 0.03THz and 3.505GHz, 0.07THz, Frequency jitter are 5.24GHz, 1.73THz and 21.51GHz, 1.199THz Period jitter are 3.424ps, 38.89ps and 21.51ps, 1.707ps in 0.7V and 0.5V supply at 27°C of FINFET as well as Transmission gate 2:1 MUX.

Keywords: MUX; CMOS; Leakage Power; Leakage Current; Frequency; FINFET; Optimum Power; Operating Current

1 Introduction

In silicon n-channel field-effect transistors (n-FETs) silicon-carbon (Si: C) source/drain (S/D) stressors may be adopted for attractive the electron mobility and drive current [1].These values are extensively higher than the doping extracted by electrical categorization, signifying doping loss in fins and/or partial activation [2]. Doped-channel FINFETs are appropriate for system-on-chip applications require various threshold voltages on the same die. For an unusual device structure for replacing the planer CMOS device structure, FINFET technology is one of the most proficient candidates [3]. In the operation of planar MOSFET scaling down

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of CMOS technology leads severe short channel effects. However increase in short channel effects will lead to degrade the performance. Another device structure is essential, to attain superior control over gate. They have an intrinsic force against the SCE. Therefore, many studies have focused on the FINFET SRAM cells to overcome the rapid decrease in the conventional bulk SRAM performance [4]. The effect of FINFET variability on the 2:1 MUX has been also studied [5] In sub-22-nm CMOS technology nodes due to their superior electrostatic integrity as compared to the conventional planar bulk MOSFET, .three-dimensional transistor structures such as double gate FINFET and tri gate FET are slated for adoption [6]. Even when the fin width is reduced to ~4 nm to enable gate length (Lg) scaling down to 10 nm, recent experimental results show that the FINFET performs well [7]. The process simulator within the Sentaurus technology computer-aided-design software suite [8], which uses the finite-element method, was used to perform 3-D simulations of stress within FINFETs with (100) top and (110) sidewall surfaces and [110] channel direction. Since the bulk-silicon substrate provides a pattern for epitaxial growth, so that the entire S/D regions are anxious for bulk FINFETs, the fin S/D regions are implicit to be etched away earlier to the discriminating epitaxial, [9] a gate-last (i.e., replacement metal gate) process flow, in which a dummy gate is formed earlier to the S/D epitaxial and then replaced by the metal gate [10].

2 Transmission Gate Based 2:1 MUX

This is the Transmission Gate based 2:1 MUX structure implemented with very minimum transistors (4 MOS transistors) compare to the CMOS based 2:1 MUX which has 20 CMOS devices. The back to back connected PMOS & NMOS transistors arrangement acts as a switch is so called Transmission Gate. In Transmission Gate NMOS transistor pass a strong 0, but a weak 1, while PMOS transistor pass a strong 1, but a weak 0. The CMOS based 2:1 MUX use NMOS transistor act as pull down network and PMOS transistor act as pull up network. Whereas in the transmission gate, combines the both properties by placing NMOS transistor in parallel with the PMOS transistor. Two transmission gates are connected as shows the schematic of Transmission based 2:1 MUX in Figure 1 to form a MUX structure and output waveform is shown in figure 2. Each the Transmission Gate acts as an AND switch to replace the AND logic gate which is used in a CMOS Based design of MUX. Hence the transistor count is reduced to 4 it shows that it occupies less area as compared to CMOS Based MUX. One more change when compared to CMOS Based 2:1 MUX is that there is no supply voltage applied to the circuit. It results in less operating power. It has lower gate delay and the circuit propagates faster than that of the CMOS Based 2:1 MUX. The gate delay as mentioned can be calculated as

$$t_{pd} \propto C_L V_{dd} / I_{ds}$$

Where, t_{pd} is the propagation delay, CL is the load Capacitance, V_{dd} is the supply voltage and I_{DS} is the drain saturation current.

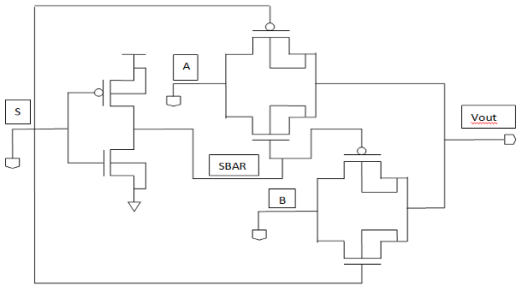

Fig. 1. Schematic of Transmission gate 2:1 MUX

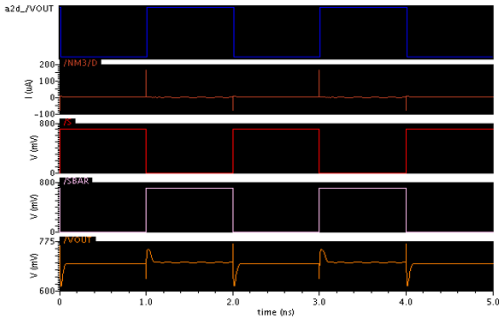

Fig. 2. Output Waveform of Transmission gate 2:1 MUX

3 Transmission gate Based 2:1 MUX using FINFET

In due to its base material the uninterrupted down in scaling of bulk CMOS creates key issues. The crucial obstacles to the scaling of bulk CMOS to 45nm gate lengths include short channel effects, optimum current, gate-dielectric leakage, and device to device variations. But FINFET based designs offers the superior control over short channel effects, low leakage and better yield [11] in 45nm helps to overcome the obstacles in scaling. Preliminary results capturing the consequence of defects manifested as cuts on the back gate were presented, demonstrating a redoubtable challenge toward the improvement of a consistent fault model [12]. However, FINFET performance is exaggerated by numerous factors, such as parasitic resistance Rp, channel stress due to the Multi Gate [13]. The author in optimizes the compensate spacer and initiate under lap on source and drain side which leads to decrease in on current [14]. In addition, for use in future

one-transistor (1T) capacitor less memory devices bulk FINFETs are also investigated. While expectant results have been obtained so far, there are some exceptional issues [15], such as the hot-carrier deprivation induced by the indoctrination, either relying on the gate induced drain leakage or the bipolar junction transistor mode [16].The gate oxide thickness is not scaled too insistently to reduce the gate leakage current and its prospective contact on retention in 1T memory applications. Both p-well and ground-plane implantations have been performed earlier to gate stack processing [17].

A parallel transistor pair consists of two transistors with their source and drain terminals tied together. The second gate is added opposite to the conventional gate in Double-Gate (DG) FINFETS, which has been predictable for their prospective to superior control short channel effects, as well as to control leakage current. The operations of FINFET is recognized as short gate (SG) mode with transistor gates attached together, the independent gate (IG) mode where self-determining digital signals are used to drive the two device gates, the low-power and optimum power mode where the back gate is attached to a reverse-bias voltage to reduce leakage power and the hybrid mode, which employs a arrangement of low power and self-determining gate modes. The schematic of transmission gate based 2:1 MUX using FINFET is shown in figure 3 and Output waveform of 2:1 MUX using FINFET is shown in figure 4.

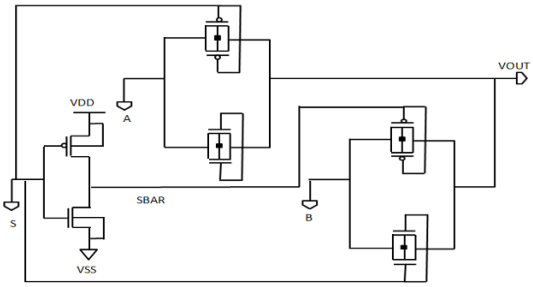

Fig. 3. Schematic of Transmission gate 2:1 MUX using FINFET

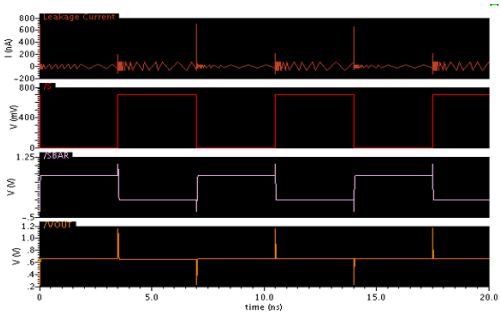

Fig. 4. Output Waveform of Transmission gate 2:1 MUX using FINFET**.**

4. Design parameters of 2:1 MUX

We have estimated the different design parameters of Transmission Gate as well as FINFET. Design parameters are Duty cycle, Bandwidth, Rise time, Frequency, Frequency jitter and Period jitter.

4.1. Duty Cycle

In a periodic event, duty cycle is the ratio of the duration of the event to the total period of signal [18].

Duty Cycle (D) = τ / T
Where τ is the duration that functions is active. T is the period of the function.

4.1. a Duty Cycle for Transmission Gate

The Duty Cycle of Transmission Gate is 54.48% and 45.99% in 0.7V and 0.5V at 27^{o}C temperature respectively. From figure5 shows that at 1ns the duty cycle is 45.99% and rise in time i.e. 2ns the duty cycle become 54.48%. After 54.48% the MUX is fully saturate therefore after 3ns,4ns and 5ns the duty cycle remains constant.

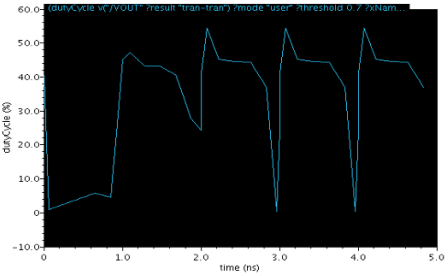

Fig.5. Duty Cycle of Transmission gate 2:1 MUX

4.1. b Duty Cycle for FINFET

The Duty Cycle of Transmission Gate is 67.41% and 10.96% in 0.7V and 0.5V at 27^{o}C temperature respectively. The eye diagram of transmission gate based 2:1 MUX using FINFET is shown in figure 7, it shows that the wide opened eye during transmission data rates of the signal .From figure 6 shows that at 1ns the duty cycle are 50% and rise in time i.e. 10ns the duty cycle becomes 67.41%.

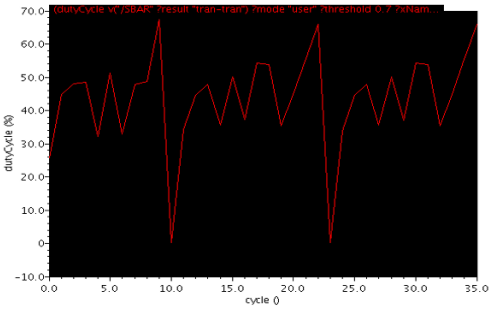

Fig.6.Duty Cycle of Transmission gate 2:1 MUX using FINFET

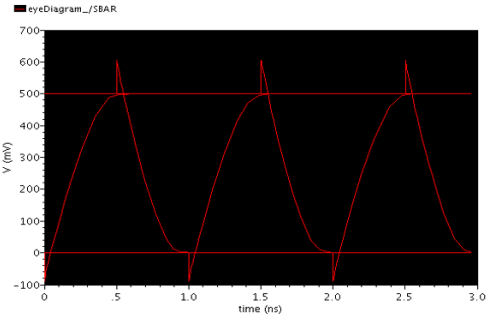

Fig.7.Eye Diagram of Transmission gate 2:1 MUX using FINFET

4.2 Jitter

Jitter is the undesired deviation from the true periodicity of an assumed periodic signal in electronics and telecommunications, often in relation to a reference clock source. Jitter may be observed in characteristics such as the frequency of successive pulses, the signal amplitude, or phase of periodic signal. Jitter can be classified in two types such as period jitter and frequency jitter.

4.2. a Period Jitter

Period Jitter is the interval between two times of maximum effect (or minimum effect) of a signal characteristic that varies regular with time.

4.2. a. 1 Period Jitter for Transmission gate

The Period Jitter of Transmission Gate is 38.89ps and 1.707ps in 0.7V and 0.5V at 27^{o}C temperature respectively. The Output waveform is shown in figure 8.From figure 8 it shows that at 1 to 1.9ns the period jitter raises 38.89ps and at 2ns it fall and again rises 2.1 to 2.9 ns it become maximum value and at 3ns it fall. After 2ns the period jitter becomes 1.707ps and at 3ns, 4ns remains constant.

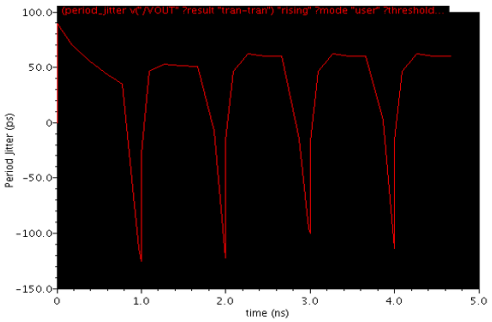

Fig.8. Period Jitter of Transmission gate 2:1 MUX

4.2. a. 2 Period Jitter for FINFET

The Period Jitter of FINFET is 3.424ps and 21.51ps in 0.7V and 0.5V at 27^{o}C temperature respectively. The Output waveform is shown in figure 9. From figure 9 it shows that at 1ns it rises and fall, again at 3ns it becomes maximum value of period jitter is 3.424ps and remains constant with rise in time.

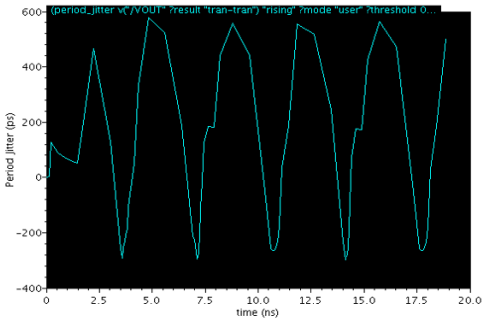

Fig.9.Peroid Jitter of Transmission gate 2:1 MUX using FINFET

4.2.b Frequency Jitter

Frequency Jitter, the more commonly quoted figure, is it inverse. Jitter frequencies below 10 Hz as wander and frequencies at or above 10Hz as Jitter.

4.2.b. 1 Frequency Jitter for Transmission Gate

The Frequency Jitter of Transmission Gate is 1.734THz and 1.199 THz in 0.7V and 0.5V at 27°C temperature respectively. The Output waveform is shown in figure 10. From figure 10 it shows that at 1ns the frequency jitter rises is 1.734THz and fall, till 1ns to 2ns the frequency jitter becomes constant and remains same.

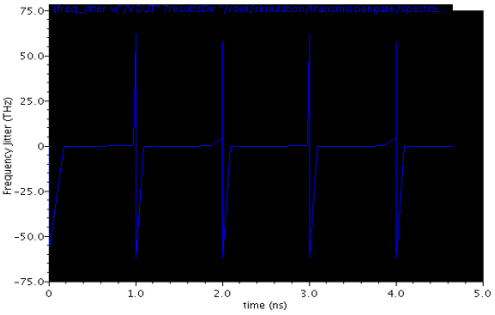

Fig.10.Frequency Jitter of Transmission gate 2:1 MUX

4.2.b. 2 Frequency Jitter for FINFET

The Frequency Jitter of FINFET is 5.24 GHz and 21.51 GHz in 0.7V and 0.5V at 27°C temperature respectively. The Output waveform is shown in figure 11. From figure 11 it shows that at 2.5 ns it rises and falls till 7.5ns. At 7.5ns it reaches its maximum value is 5.24 GHz and fall.

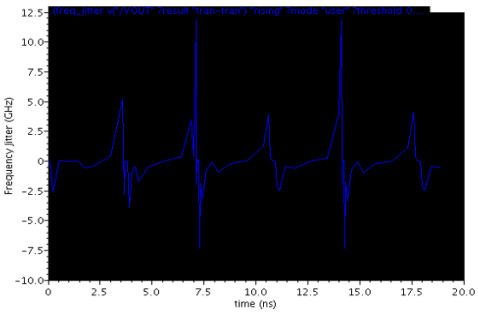

Fig.11.Frequency Jitter of Transmission gate 2:1 MUX using FINFET

5 Simulated Result Summary

To evaluate the parameters of FINFET in different power supply at various temperatures and design parameter of transmission gate and FINFET, which is shown in TABLE 1 and TABLE 2. Furthermore, accuracy of the circuit is validated by measurements in [19]. It is shown that the measured energy is in the near locality of the simulated energy dissipation. The MUX circuit often limits the operation speed of the whole system. Simulation result is calculated by CANDENCE VIRTUOSO Tool.

Table 1. Summary of 2:1 MUX using FINFET

Parameters	2:1 MUX using FINFET								
Supply Voltage	0.7V			0.5V			0.3V		
Temperature	10 °C	27 °C	50 °C	10 °C	27 °C	50° C	10° C	27°C	50°C
Operating Current	58.09µA	13.45 µA	59.03 µA	30.39 µA	27.67 µA	32.41 µA	15.43 µA	56.81 µA	15.81 µA
Operating Power	25.54nW	1.145 nW	26.05 nW	30.69 nW	16.02 nW	12.45nW	841.2nW	33.91nW	1.50 nW
Leakage Current	873.71nA	50.21 nA	599.7 nA	108.1 nA	103.6 nA	87.76nA	49.1 nA	702.1nA	90.17nA
Leakage	21	0.1	12.	2.5	1.0	1.80	1.01	5.75	1.08

Power	.65pW	48pW	19pW	37pW	22pW	2pW	pW	5pW	pW
Optimum Current	17.54µA	3.77 µA	17.34 µA	9.31 µA	9.04 µA	9.39 µA	4.05 µA	17.04 µA	3.91 µA
Optimum Power	15.16pW	32.51 pW	6.94pW	10.28 pW	.303pW	15.3 pW	36.30pW	7.582pW	30.27pW

Table 2. Computational result of transmission gate and FINFET

Parameters	Transmission Gate		FINFET	
Supply Voltage	0.7V	0.5V	0.7V	0.5V
Temperature	27oC	27oC	27oC	27oC
Duty Cycle	54.48%	45.99%	67.41%	10.96%
Bandwidth	30.0THz	70.7THz	3.502GHz	3.505GHz
Rise Time	0.0013ps	0.0036ps	0.277ps	0.534ps
Frequency	250.1MHz	270.3MHz	142.9MHz	287.9MHz
Frequency Jitter	1.73THz	1.19THz	5.24GHz	21.51GHz
Period Jitter	38.89ps	1.707ps	3.424ps	21.51ps

6 Conclusion

We have experimentally investigated the device performance and parameters such as operating current, operating power, leakage current, leakage power, optimum current and optimum power of transmission gate based 2:1 MUX using FINFETs with different power supply 0.3V, 0.5V and 0.7V at various temperatures such as 10^{o}C, 27^{o}C and 50^{o}C respectively. Mobility was enhanced in the tall-fin devices due to increased tensile stress. We have also calculated Duty cycle are 67.41%, 54.48% and 10.96%, 45.99%, rise time are 0.277ps, 0.0013ps and 0.534ps, 0.003ps, Bandwidth are 3.502GHz, 0.03THz and 3.505GHz, 0.07THz,Frequency are 142.9MHz, 287.9MHz and 270.1MHz, 270.3MHz, Frequency jitter are 5.24GHz, 1.73THz and 21.51GHz, 1.199THz Period jitter are 3.424ps, 38.89ps and 21.51ps, 1.707ps in 0.7V and 0.5V supply at 27^{o}C of FINFET as well as Transmission gate 2:1 MUX.

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