Effect of MT and VT CMOS, On Transmission gate Logic for Low Power 4:1 MUX in 45nm Technology

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Abstract. This paper describes the influence of leakage reduction techniques on 4:1 Multiplexer. The techniques investigated in this paper include multi-threshold (MTCMOS) and variable-threshold (VTCMOS). Impact of temperature sensitivity on power consumption is also evaluated. The CMOS transmission gate logic (TGL) is used to design a new 4:1 MUX, based on this design, it removes the degraded output, the NMOS and PMOS are combined together for strong output level with the gain in area is a central result of proposed MUX. The designed circuit is realized in 45 nm technology, with the power dissipation of 1.35pW from a 0.7V supply voltage. The MUX can operate well up to 200 Gb/s.

Keywords: Multiplexers, Low Power, transmission gate, Leakage Current, MTCMOS, VTCMOS

1 Introduction

A data multiplexer (MUX) is a key block in high-speed data communication systems. The acronym used for Multiplexer is MUX. The MUX is the heart of arithmetic circuit. MUX are a common building block for data paths and data-switching structures, and are used effectively in a number of applications including processors [2], processor buses, network switches, and DSPs with resource sharing. Several MUX circuits have been reported in technologies such as SiGe, GaAs and InP at speeds of 10 Gb/s or higher [6]-[8].Multiplexer (MUX) has become the bottleneck of speed. The speed of MUX determines the performance of the whole optic-fiber transceiver. DG-CNTFET structure uses specific properties, with structures based on conventional CMOS circuit design techniques. [3]

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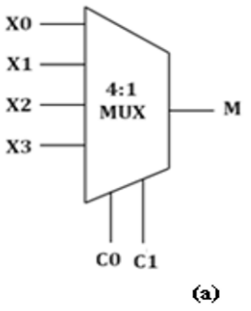
Star-junction topology with a resonating junction is proposed for multiplexer circuit. [1]. The high-speed MUX is designed, and CMOS technology has been verified to be feasible for high speed MUX with a date rate far beyond 10 Gb/s[10], [11]. However, the power consumption is a bothering problem along with the operating rate rising, since current-model logic (CML) has to be used mostly. The reported MUX with a data rate below 5 Gb/s [3], [4] also has low power efficiency, even though CMOS logic was applied. A well-known tree-type architecture [5] is adopted for the 4:1 MUX, and high-speed with low-power dissipation can be achieved through applying dynamic CMOS logic and eliminating dispensable impedance matching.

With successive technology scaling, device feature sizes and supply voltage have shrunk to recover manufacturing cost and power of VLSI circuits. Whereas dynamic power has been recede due to the supply voltage decrease, leakage current has extremely intensified due to threshold voltage (shortly Vt) and feature size scaling down. Hence, leakage current is acquired as a major source in total power dissipation [19], and it is a key to achieve low power design, especially for mobile applications. The various approaches have been proposed to reduce power consumption of MUX trees. Some of the papers contract it at the algorithm level [13]-[15] and some at the circuit level [16]-[17]. Instantly, a new functional CMOS device called Variable Threshold Voltage MOSFET (VTCMOS) has affirmed to be, throughout the next generation of ultra-low power devices operating at low supply voltage [12][20-21].

2 MULTIPLEXER

Multiplexers are used as one method of reducing the number of integrated circuit packages required by a particular circuit design. This in turn reduces the cost of the system.



C0	C1	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

(b)

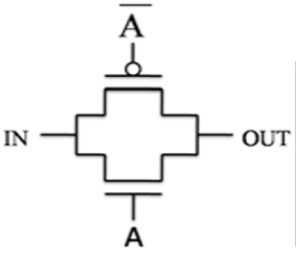
Fig. 1. Graphical Symbol 4:1 MUX.

$$\text{Output}=X0.\overline{C_0}.\overline{C_1}+X1.\overline{C_0}.C1+X2.C0.\overline{C_1}+X3.C0.C1 \quad \text{.....(1)}$$

Output of 4:1 MUX can be calculated from equation 1.Assume that we have four lines, X0, X1,X2 and X3,which are to be multiplexed on a single line, Output The four input lines are also known as the Data Inputs. Since there are four inputs, we will need two additional inputs to multiplexer, known as the Select Inputs, to select which of the X inputs is to appear at the output, called as select lines C0 and C1. The graphical symbol (a) and truth table (b) of 4:1 MUX is shown in fig.1. Output of 4:1 can be calculated from equation 1. A multiplexer performs the function of selecting the input on any one of 'n' input lines and feeding this input to one output line.

2.1 Operation of Transmission Gate

This section describes the purpose and basic operation of a transmission gate. A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The solid-state-switch is comprised of parallel connection of a PMOS transistor and NMOS transistor. The control gates are biased in a complementary manner so that both transistors are either ON or OFF.



A	IN	OUT
H	H	H
H	L	L
L	X (don't care)	Z(high impedance)

(b)

Fig. 2. Transmission gate graphical symbol (a) ,truth table (b)

When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node active-low A, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low A is a Logic 0,the complementary Logic 1 is applied to node A., turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes. The schematic diagram (Fig.2) Includes the arbitrary labels for IN and OUT, as the circuit will operate in

an identical manner if those labels were reversed. The Transmission Gate graphical symbol and truth table is shown in figure 2.

2.2 Transmission CMOS logic 4:1 MUX

The transmission gate based 4:1 MUX is designed in Fig. 3.This design is the transmission gate type of MUX structure implemented with very minimum transistors compare to conventional CMOS based design. The design is implemented with minimum number of transistor. The back to back connected PMOS and NMOS arrangement acts as a switch is so called Transmission Gate. NMOS devices pass a strong 0, but a weak 1, while PMOS pass a strong 1, but a weak 0.

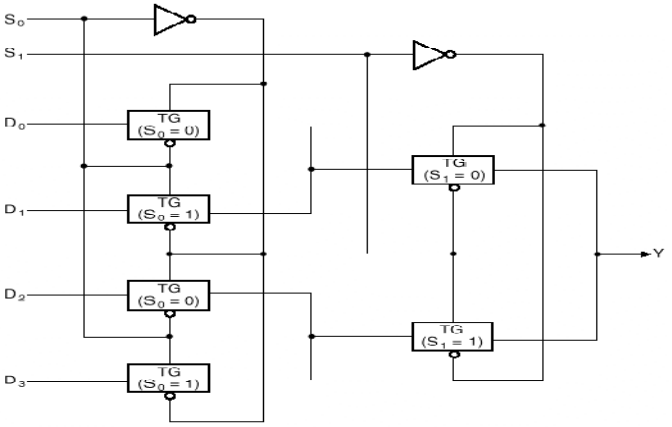


Fig. 3. Transmission gate Logic for 4:1 MUX.

The transmission gate combines the best of both the properties by placing NMOS in parallel with the PMOS device. Four transmission gates are connected as in Fig. 2 to form a MUX structure. Each transmission gate acts as an AND switch to replace the AND logic gate which is used in a conventional gate design of MUX. Hence the device count is reduced. The Transmission gate based 4:1 MUX is shown in figure 3.An advantage of the new MUX design is the remarkable gain in terms of transistors count. To the best of our knowledge, no 4:1 MUX has been realized with so few devices. Hence the gain in area is a central result for the proposed MUX.

2.3 Temperature effect on Power Consumption

Temperature dependence of leakage power is important, since digital very large scale integration circuits generally operate at elevated temperatures due to the power dissipation of the circuit. The power consumption increases with the rise in temperature. The effect of temperature on power consumption in TGL based 4:1 MUX is shown in Fig.4.

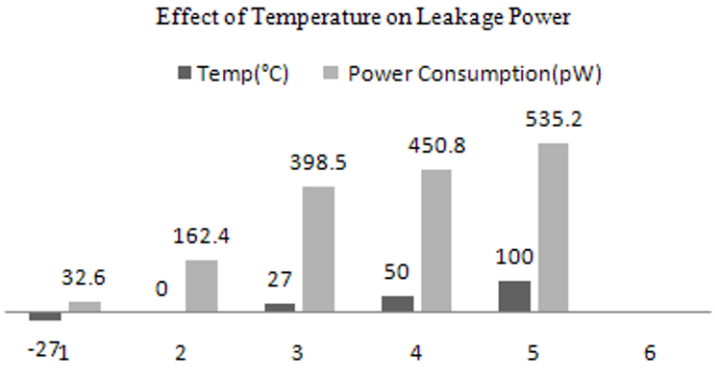


Fig. 4 .Effect of Temperature on TGL based 4:1 MUX.

3 LEAKAGE REDUCTION TECHNIQUES

In this section, two major circuit design techniques namely, MTCMOS, VTCMOS for leakage reduction in digital circuits are described:

3.1 MTCMOS (Multi-threshold CMOS)

Multi-Threshold CMOS (MTCMOS) is a popular power gating approach that uses high Vth devices for power switches [23]. Fig. 5 shows the basic MTCMOS structure, where a low Vth computational block uses high Vth switches for power gating. Low Vth transistor in the logic gate provides a high performance operation. However, by introducing a series device to the power supplies, MTCMOS circuits incur a performance penalty compared to CMOS circuits. The basic

MTCMOS structure is shown in fig.5, where a low V_{th} computation block is gated with high V_{th} power switches.

A specialized case of dual V_{th} technology that is more effective at reducing leakage currents in the standby mode is MTCMOS (Multi-Threshold CMOS). Though, by introducing an extra series device to the power supplies, MTCMOS circuits will provoke a performance penalty compared to CMOS circuits, which declines if the devices are not sized large enough. When the high V_{th} transistors are turned on, the low V_{th} logic gates are connected to virtual ground and power, and switching is performed through fast devices [22]. When the circuit enters the sleep mode, the high V_{th} gating transistors are turned off, resulting in a very low sub threshold leakage current from V_{CC} to ground. MTCMOS is only effective at reducing standby leakage currents and therefore is most effective in burst mode type application, where reducing standby power is a major benefit.

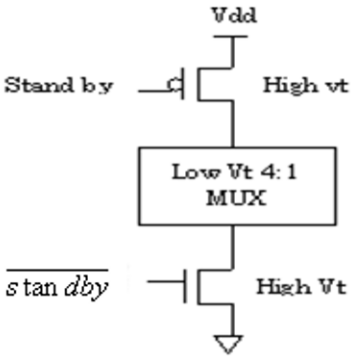


Fig. 5. MTCMOS.

3.2 VTCMOS (Variable Threshold CMOS)

Variable threshold CMOS is a body biasing based design technique Fig. 6 illustrates the VTCMOS scheme. To achieve different threshold voltages, it uses a self-substrate bias circuit to control the body bias. Regarding the speed performance of VTCMOS circuits the gate delay is the vital factor. In CMOS digital circuits, the gate delay time (t_{pd}) is given by equation 2.

$$Tpd \propto \frac{CVcc}{(Vcc-Vt)^{\alpha}} \quad \text{..... (2)}$$

α- power law model
The operating principle of VTCMOS is that its threshold voltage (V_{th}) is controlled by the applied substrate bias (- $|V_{bs}|$), leading to lower stand-by off current or higher active on-current. The V_{th} shift is given by: $\Delta V_{th} = \gamma |V_{bs}|$ where γ is the body effect factor [4]. Variable Threshold CMOS or (VTCMOS) is the another technique that has been developed to reduce standby leakage currents, relatively than apply multiple threshold voltage options, VTCMOS relies on a triple well process where the device V_t is dynamically is adjusted by biasing the body terminal.

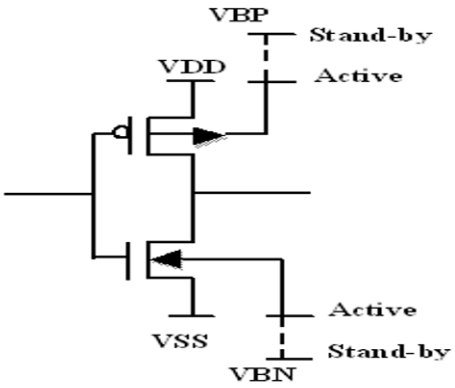


Fig. 6. VTCMOS.

4 SIMULATION RESULTS

The Simulation result is measured by CADENCE VIRTUOSO Tool.
The Simulation Conditions for 4:1 MUX circuit is summarized in TABLE I and the effect of Leakage reduction techniques (MTCMOS and VTCMOS) for 4:1 MUX is figure out in TABLE II.

4.1 Input Output Pattern for TGL 4:1 MUX

The simulation waveform of proposed 4:1 MUX is shown in Fig. 7.The resultant waveform attains a single output during power supply of 0.7v although the rise and fall time of simulation is 100 fs. The output pattern is shown in the fig.7,

S0 and S1 are the select lines for the 4:1 multiplexer and, S0bar (S0b) and S1bar (S1b) are the opposite signal of S0 and S1 respectively. Z is the output of 4:1 MUX.

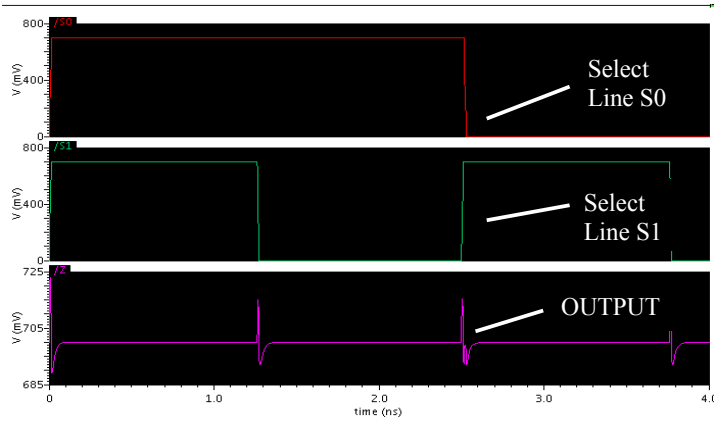


Fig. 7. Simulation Input output pattern.

4.2 Power and Current Consumption

Digital CMOS circuit may have three major sources of power dissipation namely dynamic, short and leakage power. Hence the total power consumed by every MUX style can be evaluated using the following equation 3.

$$\begin{aligned} Ptot &= Pdyn + Psc + P\ leak \\ &= CLVddV f clk + ISCVdd + I\ leakVdd \end{aligned} \qquad \ldots\ldots. (3)$$

Thus for low-power design the important task is to minimize C_L V_{dd} V f_{Clk} while retaining required functionality. The first term P_{dyn} represents the switching component of power, the next component P_{sc} is the short circuit power and P_{leak} is the leakage power. Where, CL is the loading capacitance, f_{Clk} is the clock frequency which is actually the probability of logic 0 to 1 transition occurs (the activity factor). Vdd is the supply voltage; V is the output voltage swing which is equal to Vdd. The current I_{SC} is due to the direct path short circuit current. Finally, leakage current I leak, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. The Leakage Current of TGL based MUX is shown in fig. 8.

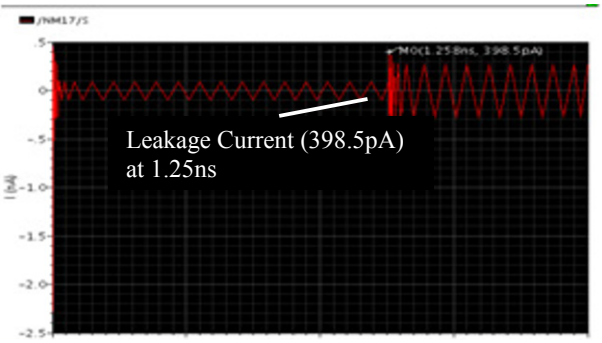


Fig. 8. Leakage current of TGL based 4:1 MUX.

4.3 Eye Diagram

Eye diagram of the output signal at a data rate of 200Gb/s. The measured eye diagram is shown in Fig.9.

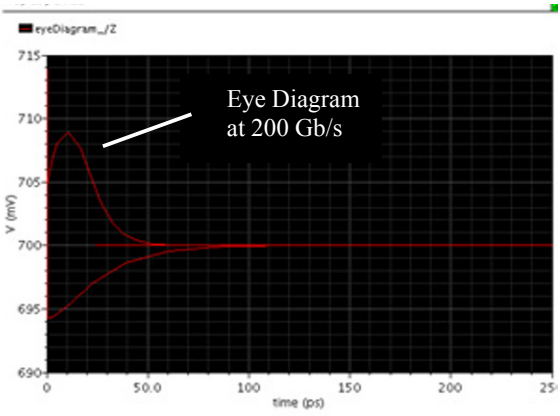


Fig. 9. Measured Eye diagrams of MUX Output at 200 Gb/s.

Table 1. Simulation Conditions of TGL based 4:1 MUX

Technology	45nm
Function	4:1 MUX
Lgate(nm)	45
Width(nm)	120
|Vth| (V)	0.16
Vdd(V)	0.7
Temp.(°C)	27

Table 2. Simulation of TGL based 4:1 MUX with MTCMOS and VTCMOS

4:1 MUX	Parameters		
	Leakage Current	Leakage Power	Delay
Earlier work[5]	29.6 mA	53.3 mW	-
TGL	398.5pA	1.35pW	1.25ns
MTCMOS	182.8pA	1.23pW	1.45ns
VTCMOS	355.4pA	1.31pW	1.31ns

6 Conclusions

The techniques investigated in this paper include multi-threshold (MTCMOS) and variable-threshold (VTCMOS). Impact of temperature sensitivity on power consumption is also evaluated. The transmission gate logic results to be the efficient design styles for MUX design [18] Transistors are reduced to great extent, so that the overall area is minimized. The designed circuit is realized in 45 nm technologies, with the power consumption of 1.35 pW from a 0.7 V supply voltage at 27°C. Leakage current is also reduced to 398.5 pA. MTCMOS is only effective at reducing standby leakage currents and therefore is most effective in burst mode type application, where reducing standby power is a major benefit, while delay gets increases. For VTCMOS slightly forward substrate bias can be used to increase the circuit speed. Finally, the impact of Leakage reduction techniques (MTCMOS and VTCMOS) is analyzed in this paper; VTCMOS impart circuit

designer's complete flexibility to set both V_{DD} and V_{th} during active modes to perfect balance between performance and Leakage power.

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