43. Packaging and Reliability Issues in Micro/Nano Systems

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The potential of microelectromechanical systems (MEMS)/nanoelectromechanical systems (NEMS) technologies has been viewed as a revolution comparable to or even greater than that of microelectronics. The scientific and engineering advancements in MEMS/NEMS could enable applications that were previously unthinkable, from space systems, environmental instruments, to appliances for use in daily life. As presented in previous chapters, development of core MEMS/NEMS processes has already demonstrated many commercial applications as well as potential for advanced functionality in the future. However, low-cost and reliable packaging for protection of these MEMS/NEMS products remains a very difficult challenge. Without addressing these packaging and reliability issues, no commercial products can be sold on the market. Packaging design and modeling, packaging material selection, packaging process integration, and packaging cost are the main issues to be considered when developing a new MEMS packaging process. In this chapter, we present the fundamentals of MEMS/NEMS packaging technology, including packaging processes, hermetic and vacuum encapsulation, wafer-level packaging, three-dimensional (3-D) packaging, polymer-MEMS assembly and encapsulation, thermal issues, packaging reliability, and future packaging trends. Specifically, development of MEMS packaging will rely on successful implementation of several unique techniques, including packaging design kits for system and circuit designers, low-cost and high-yield wafer-level, chip-scale packaging techniques, effective testing techniques at wafer level to reduce overall testing costs, and reliable fabrication of an interposer [43.1] with vertical through interconnects for device integration.

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43.1 Introduction to MEMS Packaging

MEMS are miniaturized systems of micrometer to millimeter size, integrating mechanical, chemical, or biomedical features with IC circuitry for sensor or actuator applications [43.2]; For example, pressure [43.3], temperature, flow [43.4], acceleration [43.5], gyroscopic [43.6], and chemical sensors [43.7] can be fabricated using MEMS technologies for sensing applications, while fluidic valves [43.8], pumps [43.9], and inkjet printer heads are examples of actuation devices for medical, environmental, office, and industrial applications. Silicon is typically used as the primary substrate material for MEMS fabrication, because of its unique electrical, thermal, and mechanical properties as well as its easy micromachining in batch processing and

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potential incorporation with microelectronic circuitry mostly using conventional semiconductor manufacturing processes and tools. The resulting MEMS devices offer the advantages of smaller size, lighter weight, lower power consumption, and lower fabrication cost compared with existing macroscale systems offering similar functionality. With the advances of MEMS fabrication technology in recent decades, the MEMS market at component level now exceeds 5 billion, driving end-product markets of more than 100 billion [43.10].

Nevertheless, the road to commercialization of MEMS does not look as promising as expected. Many industrial companies have taken advantage of MEMS technology due to the high production volumes and high added value resulting from product integrations. Therefore, cost-efficiency has become the major factor driving MEMS toward commercialization. Several MEMS devices have been developed for and applied in the automotive industry and information technology field, dominating the MEMS market due to their high production volumes. However, custom-designed MEMS products remain very diverse, aiming for different applications, and their initial costs in small- to medium-scale production are still much higher than market-acceptable levels. In this regard, high packaging and testing costs have hindered MEMS commercialization. Furthermore, based on past experience in the IC industry, the cost of packaging processes is about 30% and can sometimes be more than 70% of total production costs. MEMS packaging processes are expected to be even more costly, because of the challenging and stringent packaging issues related to the MEMS components, in addition to microelectronic circuitry, in a typical MEMS product [43.11].

43.1.1 MEMS Packaging Fundamentals

Sealing or encapsulation is an important step in either integrated circuit (IC) or MEMS packaging processes, to protect devices during operation. In traditional IC packaging procedures, the overall packaging steps often involve [43.12, 13]:

1. Wafer dicing
2. Pick-and-place
3. Electrical connections, such as wire bonding
4. Plastic molding or housing for the sealing process.

With the increasing requirement for high-performance and multifunctional consumer electronic products, IC packaging processes have incorporated more complex designs and advanced fabrication technologies, such as Cu interconnects [43.14], flip-chip bonding [43.15], ball grid array [43.16], wafer-level chip-scale packaging [43.17], 3-D packaging [43.18], etc. to satisfy the needs for high I/O density, large die area, and high clock frequency. The functions of conventional IC packaging are to protect, power, and cool the microelectronic chips or components and provide electrical and mechanical connection between the microelectronic part and the outside world. Unlike regular ICs, the diversity of MEMS products complicates the sealing issue. MEMS packaging processes cannot directly follow the procedures applied in the IC packaging industry due to inclusion of free-standing physical microstructures or chemical substances which cannot survive dicing or pick-and-place steps before the sealing process. Moreover, MEMS components may need to interface with the outside environment (for example, fluidic interconnectors [43.19]), while other components may need to be hermetically sealed (for example, accelerometers [43.5]) in addition to the need for electrical interconnects. Therefore, MEMS packaging processes may have to provide more functionality, including better mechanical protection, thermal management, hermetic sealing, and complex electrical and signal distributions.

It has been suggested that MEMS packaging should be incorporated in the device fabrication stage as part of the micromachining process. Although this approach solves the packaging requirement for some specific devices, it does not address it for general microsystems. In particular, many MEMS devices are now fabricated using various foundry services [43.20, 21], and there is a tremendous need for a uniform packaging process. Figure 43.1 shows a typical MEMS device being encapsulated by a packaging cap. The most fragile part of this device is the suspended mechanical sensor, which is a freestanding mass–spring microstructure. This mechanical part should be protected during packaging and handling processes. Moreover, vacuum encapsulation may be required for such microstructures in applications including resonant accelerometers [43.5] or gyroscopes [43.6, 22]. A *packaging cap* with a properly designed microcavity should be fabricated to encapsulate and protect such fragile MEMS structures as a first-level postpackaging process. The wafer can then be diced and well-established packaging technology from the IC industry applied to complete the packaging. Additionally, a common packaging requirement for MEMS devices is hermetic sealing and sometimes vacuum encapsulation. Hermetic sealing is important to ensure that no moisture or contamination can enter the package and affect the functionality of microstructures. This increases the difficulty of common IC packaging processes tremendously. Although most single-function MEMS chips can employ typical IC packaging techniques, such as die-attachment pro-

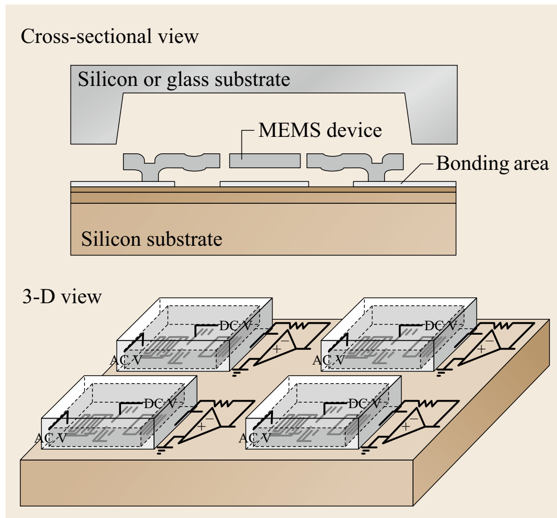

Fig. 43.1 Typical MEMS packaging with a MEMS structure encapsulated and protected by a packaging cap

cesses and wiring interconnects, using molded plastic, ceramic, or metal for packaging [43.12], the increasing complexity of MEMS devices requires more advanced packaging techniques, especially wafer-level packaging, for integration of multiple chips for multifunctional applications; for example, if chemical or biomedical substances are present [43.23], any sealing process must not exceed low processing temperatures. For optical devices [43.24], the sealing process should provide good optical paths. If mechanical resonators are included [43.25], vacuum sealing might be required to improve device performance, with the desired vacuum level depending on the device specification.

Before state-of-the-art MEMS packaging processes are discussed, several primary microfabrication processes for packaging applications are summarized. These processes include the flip-chip (FC) technique, ball grid array (BGA), through-wafer etching, and electroplating. Other silicon-based processes, such as thin-film deposition, wet and dry chemical etching, lithography, lift-off, and wire-bonding processes, are described in many textbooks [43.26].

Flip-Chip (FC) Technique

This technique is commonly used in the assembly process of a chip with microelectronics and a packaging substrate [43.15]. The microelectronic chip is *flip joined* with the packaging substrate, and metal solder bumps are used for both bonding and to form electrical paths between bond pads on the microelectronic chip and metal pads on the packaging substrate. Because the vertical bonding space may be very narrow, being controlled by the height of the solder bumps, and the bond pads can be distributed across the whole chip rather than only on the edge, this technique can provide high-density input/output (I/O) connections. In the FC technique, solder bumps are generally fabricated by means of electroplating. Before the bumping process, multiple metal layers, such as TiW-Cu, Cr-Cu, Cr-Ni, or TaN/Ta/Ni, are deposited to form a seed layer for electroplating and as a diffusion barrier to prevent diffusion of solder into underlying electrical interconnects.

Ball Grid Array (BGA)

This technology is very similar to the FC technique. An area array of solder balls on a single- or multichip module are used in the packaging process as electrical, thermal, and mechanical connects to join the module with the next-level package, usually a printed circuit board [43.16]. The major difference between typical BGA and FC chips is the size of the solder bumps; in a BGA chip, the bumps are in the order of 750 μm in diameter, which is 10 times larger than those commonly used in an FC chip.

Through-Wafer Etching

This is a chemical etching process to make through-wafer channels on a silicon substrate for fabrication of vertical through-wafer interconnects. The chemical etching can be either a wet or dry process. Anisotropic or isotropic etching solutions can be used in a wet etching process, while the dry etch process is based on plasma and ion-assisted chemical reactions, which can be either isotropic or anisotropic. To create high-density and high-aspect-ratio through-wafer vias, deep reactive-ion etching (DRIE) is typically used. Two popular DRIE approaches, Bosch and Cyro, are well described in literature [43.27].

Electroplating

Electroplating is another common microfabrication process. It can be used for deposition of an adherent metallic layer onto a conductive or nonconductive substrate. The process on a conductive substrate is called electrolytic plating, utilizing a seed layer as the anode to transfer metal ions onto the cathode surface when a DC current is passed through the plating solution. The plating process without use of an electrical current is called electroless plating and can be applied on both conducive and nonconductive surfaces. The electroless plating process requires a layer of noble metal such as Pd, Pt, or Ru on the substrate to catalyze the self-decomposition reaction in the plating solution. Electroplating processes are very important for fabrication of electrical interconnects and solder bumps for packaging applications, because of their low process temperature and cost. They are generally applied to pro-

vide electrical and thermal paths for various IC/MEMS packaging approaches.

43.1.2 Contemporary MEMS Packaging Approaches

Several MEMS packaging issues and approaches before 1985 were discussed in the book *Micromachining and Micropackaging of Transducers* [43.28], and researchers have been working on MEMS packaging approaches continuously since then; for example, *Senturia* and *Smith* [43.29] discussed packaging and partitioning issues for microsystems, and *Smith* and *Collins* [43.23] used epoxy to bond glass and silicon for chemical sensors. Several multichip module (MCM) methods have been proposed. *Butler* et al. [43.30] proposed adapting multichip module foundries using the chip-on-flex (COF) process. *Schuenemann* et al. [43.31] introduced a 3-D stackable packaging concept based on the top–bottom ball grid array (TB-BGA) that includes electric, fluidic, optical, and communication interfaces. *Lee* et al. [43.32] and *Ok* and *Baldwin* [43.10] presented a direct-chip-attach MEMS packaging approach using through-wafer electrical interconnects. *Laskar* and *Blythe* [43.33] developed an MCM packaging process using epoxy. *Reichl* [43.34] discussed different materials for bonding and interconnection. *Grisel* et al. [43.35] designed a special process to package microchemical sensors. Special processes have also been developed for MEMS packaging, such as packaging for microelectrodes [43.36], packaging for biomedical systems [43.37], and packaging for space systems [43.38]. These specially designed, device-oriented packaging methods are aimed at individual systems. However, there are few reliable methods that would qualify as versatile MEMS postpackaging processes that meet the rigorous process requirements of low temperature, hermetic sealing, and long-term stability.

Several MEMS postpackaging processes have been proposed. *Butler* et al. [43.30] demonstrated an advanced MCM packaging scheme. It adopts the high-density interconnect (HDI) process consisting of embedding bare die into premilled substrates. Because MEMS structures have to be released after the packaging process, this scheme is undesirable for general microsystems. *Van der Groen* et al. [43.39] reported a transfer technique for complementary metal–oxide–semiconductor (CMOS) circuits based on epoxy bonding. This process overcomes the surface roughness problem, but epoxy is not a good material for hermetic sealing. In 1996, Cohn et al. demonstrated a wafer-to-wafer vacuum packaging process using silicon-gold eutectic bonding with a 2 μm-thick polysilicon microcap. However, experimental results showed substantial leakage after a period of 50 days. *Cheng* et al. [43.40] developed a vacuum packaging technology using localized aluminum/silicon-to-glass bonding. In 2002, *Chiao* and *Lin* [43.41] demonstrated vacuum packaging of microresonators by rapid thermal processing. These research efforts indicate the strong need for a versatile MEMS postpackaging process.

43.1.3 Bonding Processes for MEMS Packaging Applications

Silicon bonding technologies have been used in many MEMS fabrication and packaging applications, two types of which are commonly applied:

- Direct bonding processes such as anodic bonding and fusion bonding
- Bonding processes with intermediate layers, such as epoxy bonding, eutectic bonding, and solder bonding.

Direct wafer bonding processes are procedures that facilitate permanent attachment between two wafers without any intermediate layer. A permanent bond between two wafers can also be accomplished by using intermediate layers. Joining processes using intermediate layers have been extensively used in the ceramic industry to form metal-to-metal and metal-to-ceramic joints [43.42, 43] and can be characterized as [43.44]:

1. Fusion or melting of two materials to form a stable intermediate compound which facilitates the bond
2. Diffusion, in which pressurized joint parts are heated to 70% of the material's melting temperature to form a stable intermediate compound at the interface
3. Brazing, where a filler material is placed between the two parts to be joint, forming a stable intermediate compound upon heating.

These processes are commonly used when a lower bonding temperature or stronger bonding interface is required but cannot be achieved by a direct bonding process. Furthermore, the intermediate layers may reflow during the bonding process and fill the gaps between two bonding surfaces to overcome the surface roughness problem commonly encountered during direct wafer bonding processes. As such, the requirement for fine surface roughness for direct wafer bonding processes can be greatly relieved by using such intermediate layers.

Many MEMS applications have used both direct bonding as well as other bonding processes based on intermediate layers; For example, devices such as pressure sensors, micropumps, and biomedi-

cal or chemical sensors require mechanical interconnection when bonded onto the substrate [43.7, 19, 45]. Glass has been commonly used as the bonding material for anodic bonding at temperature of about 300–450 °C [43.46, 47]. *Klaassen* et al. [43.48] and *Hsu* and *Schmidt* [43.49] demonstrated different types of silicon fusion and Si–SiO_2 bonding processes at very high temperatures above 1000 °C. *Ko* et al. [43.28], *Tiensuu* et al. [43.50], *Lee* et al. [43.51], and *Cohn* et al. [43.52] used eutectic bonding for different applications. All of these bonding techniques have different mechanisms that determine the individual bonding characteristics and process parameters. This section discusses the details of these processes.

Fusion Bonding

Silicon fusion bonding is an important fabrication technique for silicon-on-insulator (SOI) technology. This method is based on the strong Si–O, Si–N, or Si–Si covalent bonds. However, very high bonding temperature (above 1000 °C) and flat bonding surfaces (below 6 nm) to ensure intimate contact are the two basic requirements for strong, uniform, and hermetic bonding. The common silicon-to-silicon fusion bonding process starts with wafer hydration (soaking in H_2O_2–H_2SO_4 mixture, diluted H_2SO_4, or boiling nitric acid, or use of oxygen plasma) to create a hydrophilic top layer consisting of O–H bonds [43.53]. Prebonding is accomplished when the two wafers are brought into intimate contact and van der Waals forces create a bond between the two wafers. An annealing step at elevated temperature is required to strengthen the bond. Although hydrophilic surface treatment can lower the bonding temperature, annealing above 800 °C is still required to prevent bubble formation at the bonding interface. *Bower* et al. [43.54] proposed that Si_3N_4 fusion bonding could be achieved at temperature below 300 °C. *Takagi* et al. [43.55] proposed that silicon fusion bonding could be achieved at room temperature by using Ar^+-beam treatment of the wafer surface with bond strength comparable to conventional fusion bonding. In summary, fusion bonding is a popular fabrication technique for MEMS fabrication and packaging.

Anodic Bonding

The invention of anodic bonding dates back to 1969, when *Wallis* and *Pomerantz* [43.56] found that glass and metal could be bonded together at about 200–400 °C below the melting point of glass with the aid of a high electrical field. This technology has been widely used for protecting onboard electronics in biosensors [43.57–59] and sealing cavities in pressure sensors [43.60]. Many reports have also discussed the possibility of lowering the bonding temperature using different approaches [43.61, 62]. Anodic bonding forms Si–O or Si–Si covalent bonds, some of the strongest chemical bonds available for silicon-based systems. The bonding process can be accomplished on a hot-plate at temperature of 180–500 °C in atmosphere or vacuum environment. When a static electrical field is applied between Pyrex glass and silicon, sodium ions in the glass migrate away from the silicon–glass interface, creating a locally high electrical field, and a bond forms due to electrochemical effects [43.56]. To create a high electrical field, a flat bonding surface with roughness of less than 50 nm is required. In addition, the electrical field required for bonding is larger than 3×10^6 V/cm [43.28]. Such a high electrical field is generated by a power supply of 200–1000 V. Figure 43.2 shows the setup for anodic bonding, where two bonding wafers are brought together and heated to an elevated temperature to supply the bonding energy. Care must be taken if there are free-standing, conductive micromechanical structures on either wafer to be bonded, as the high voltage tends to pull and may damage such structures. A thin metal film can be formed on the glass cap to provide shielding to solve this problem, as shown in Fig. 43.2. Furthermore, Corning 7740 Pyrex is commonly used in silicon-to-glass bonding systems, because it contains sodium ions and has a thermal expansion coefficient close to that of single-crystalline silicon in the range of 200–300 °C. The problem of induced residual stress can thereby be minimized in this temperature range. *Hanneborg* et al. [43.63] successfully bonded silicon with other thin solid films, such as silicon dioxide, nitride, and polysilicon, by using an intermediate glass layer with the anodic bonding technique. *Chavan* and *Wise* [43.64] reported absolute pressure sensors fabricated using the anodic bonding technique. In this process, a silicon cap with a thin, heavily doped boron layer and a recess cavity was bonded in vacuum environment to a glass substrate with prefabricated interconnection lines. However, the problem of oxygen outgassing due to the high electrical field in the anodic bonding process presents a challenge for the vacuum sealing process [43.65]. A thin Ti/Pt

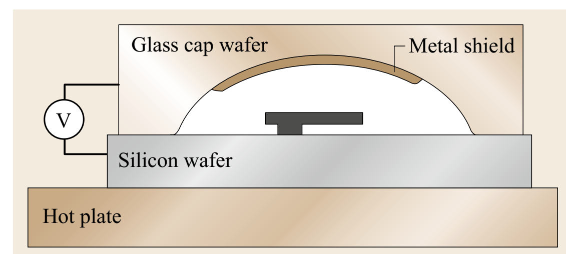

Fig. 43.2 Schematic diagram of setup for silicon-to-glass anodic bonding

layer predeposited on the glass surface has been shown to provide a good diffusion barrier, and the resulting pressure in the cavity can reach 200 mTorr [43.64]. In another example, microgyroscopes were fabricated using the anodic bonding technique by *Hara* et al. [43.66].

In practice, electrostatic bonding has become widely accepted for MEMS fabrication and packaging applications, as described above. Unfortunately, the possibility of contamination due to excessive alkali metal in the glass or damage to microelectronics due to the high electrical field, and the requirement for flat bonding surfaces limit application of anodic bonding for MEMS postpackaging [43.67].

Epoxy Bonding (Adhesive Bonding)

Epoxy comprises four major components: epoxy resin, filler-like silver slake, solvent or reactive epoxy diluent, and additives such as hardeners and catalysts [43.68, 69]. The bonding mechanism is very complicated, depending on the type of epoxy applied. In general, the main source of bonding strength is the van der Waals force. Because epoxy is a soft polymer material and its curing temperature for bonding is only around 150 °C, low residual stress and process temperature are the major advantages of epoxy bonding. However, the properties of epoxy can be easily changed by environmental humidity and temperature, so the bonding strength decays over time. In addition, epoxy bonding has low moisture resistance and is a dirty process due to its additives. These disadvantages make epoxy bonding unfavorable for special MEMS packaging requirements such as hermetic or vacuum sealing.

Eutectic Bonding

In many binary systems, there is a eutectic point corresponding to the alloy composition with the lowest melting temperature. If the environmental temperature is maintained above this eutectic point, two contacting surfaces containing the two elements with the eutectic composition can form liquid-phase alloy. Solidification of this eutectic alloy results in *eutectic bonding* at a temperature lower than the melting temperature of either element in the alloy. Eutectic bonding can form a strong metal bond; For example, in the case of the Au–Si alloy system, the eutectic temperature is only 363 °C for the composition with atomic ratio of 81.4% Au to 18.6% Si, and the bonding strength is above 5.5 GPa [43.70]. Because other alloy systems may have lower eutectic temperature than the Al–Si system, they have great potential for use in MEMS packaging applications. In addition to the Au–Si system, the Al–Ge, Au–SnSi, and Au–Ge–Si systems have been applied for MEMS packaging. Specifically, InvenSense has used the Al–Ge bonding process for their gyroscope products [43.71].

Solder Bonding

Solder bonding has been widely used in microelectronic packaging [43.72], offering the advantages of both low bonding temperature and high bonding strength for packaging applications. Furthermore, there are a variety of choices of solder material for specific applications. *Singh* et al. [43.73] successfully applied solder bump bonding for integration of electronic components and mechanical devices in MEMS fabrication [43.74]. In this case, indium metal was used to bond two separated silicon surfaces together by applying 350 MPa pressure, with bonding strength as high as 10 MPa. Glass frit can also be treated as a solder material and has been extensively used for vacuum encapsulation in the MEMS industry. Glass frits are ceramic materials that can provide strong bonding strength with silicon and good hermeticity. The bonding temperature is lower than 400 °C, suitable for electronic components. However, bonding width of greater than 200 μm is required to achieve good bonding results, which may become a drawback because area is a measure of manufacturing cost in the IC industry. Nevertheless, glass frit is the most popular bonding process used in current MEMS products.

Localized Heating and Bonding

Low bonding temperature and short process time are desirable process parameters for MEMS packaging fabrication, to decrease the thermal budget and increase throughput. However, most chemical bonding reactions require a minimum thermal energy to overcome the reaction energy barrier, or activation energy, to start the reaction and form a strong bond. As a result, high bonding temperature generally results in shorter processing time to reach the same bonding quality at a lower bonding temperature [43.75]. The common limitations of the bonding techniques described above are their individual bonding characteristics and temperature requirements. In general, MEMS packaging requires good bonding for hermetic sealing, while the processing temperature must be kept low at wafer level to have less thermal effects on devices that are already present; For example, a MEMS device may have prefabricated circuitry, biomaterial or other temperature-sensitive materials such as organic polymer, magnetic metal alloy, or piezoceramic. Since the packaging step comes after the MEMS device fabrication processes, the bonding temperature should be kept low to avoid effects of high temperature on the system. Possible temperature effects include residual stress due to thermal expansion coefficient mismatch between bonding materials and substrates, electrical contact failure due to atomic interdiffusion at the interface, and contamination due to outgassing or evaporation of materials. In addition to control of

Table 43.1 Summary of bonding mechanisms

Bonding method	Temperature	Roughness	Hermeticity	Postpackaging	Reliability
Fusion bonding	Very high	Highly sensitive	Yes	Yes by LH[a]	Good
Anodic bonding	Medium	Highly sensitive	Yes	Difficult	Good
Epoxy bonding	Low	Low	No	Yes	–[b]
Integrated process	High	Medium	Yes	No	Good
Low-temp. bonding	Low	Highly sensitive	–[b]	No	–[b]
Eutectic bonding	Medium	Low	Yes	Yes by LH[a]	–[b]
Brazing	Very high	Low	Yes	Yes by LH[a]	Good

[a] Localized heating
[b] No conclusive data

the bonding temperature, the magnitude of the force applied to create intimate contact for bonding and control of the atmospheric environment are other factors that should be considered. Based on heat transfer simulations [43.76], it is possible to confine the high-temperature area to a small region by using localized heating without heating the whole substrate. Therefore, assembly steps can always be applied after device fabrication without having detrimental effects. As such, localized heating and bonding techniques have been introduced and implemented as postprocessing approaches for fabrication of MEMS packaging [43.75, 77].

Table 43.1 summarizes these MEMS packaging technologies and their limitations, including the localized heating and bonding approach. The localized heating approach introduces several new opportunities. First, better and faster temperature control can be achieved. Second, higher temperature can be applied to improve the bonding quality. Third, new bonding mechanisms that require high temperature such as brazing [43.78] may now be explored for use in MEMS applications. As such, this approach has potential applications for a wide range of MEMS devices and is expected to advance the field of MEMS packaging.

43.2 Hermetic and Vacuum Packaging

Hermetic packaging is beneficial because it provides a moisture-free environment to avoid charge separation in capacitive devices, corrosion of metallization, and electrolytic conduction, thereby prolonging the lifetime of electronic circuitry. Especially for MEMS packaging, hermeticity is desirable in most cases since one of the main failure mechanisms for MEMS devices is humidity, and the surface tension of water can cause stiction of micromechanical structures, leading to malfunction. In several device applications, vacuum encapsulation is necessary but can be costly. Many surface-micromachined resonant devices need vacuum to improve their performance, such as comb-shaped μ-resonators and ring-type μ-gyroscopes, which have very high surface-to-volume ratio and vibrate in a very tight space [43.22, 79]. Two major approaches for hermetic and vacuum packaging of MEMS have been demonstrated and are discussed in this section:

- The integrated encapsulation approach
- The postprocess packaging approach.

Moreover, vacuum encapsulation by means of localized heating and bonding is discussed separately as another example of issues related to hermetic and vacuum packaging.

43.2.1 Integrated Micromachining Processes

Several hermetic and vacuum packaging processes for MEMS have been demonstrated based on integrated micromachining processes, where construction of sealing or protection caps is integrated with the MEMS device manufacturing process. This integrated approach has the advantage of sealing mechanical components in situ prior to the chip dicing and handling steps, to avoid contamination. An integrated vacuum sealing process using low-pressure chemical vapor deposition (LPCVD) is presented here as an illustrative example. This integrated process can encapsulate comb-shaped microresonators [43.80] in vacuum at wafer level. Figure 43.3 presents a cross-sectional view of the manufacturing process. First, a standard surface micromachining process [43.81] is conducted by using four masks to define a first polysilicon layer, anchors to the substrate, dimples, and a second polysilicon layer, as shown in Fig. 43.3a. The process so far is similar to the polyMUMPs process (MUMP: multi-user MEMS process) [43.21], and comb-shaped microstructures are fabricated at the end of these steps. In the standard surface micromachining process, the sacrificial layer (oxide) would be etched away to release the microstruc-

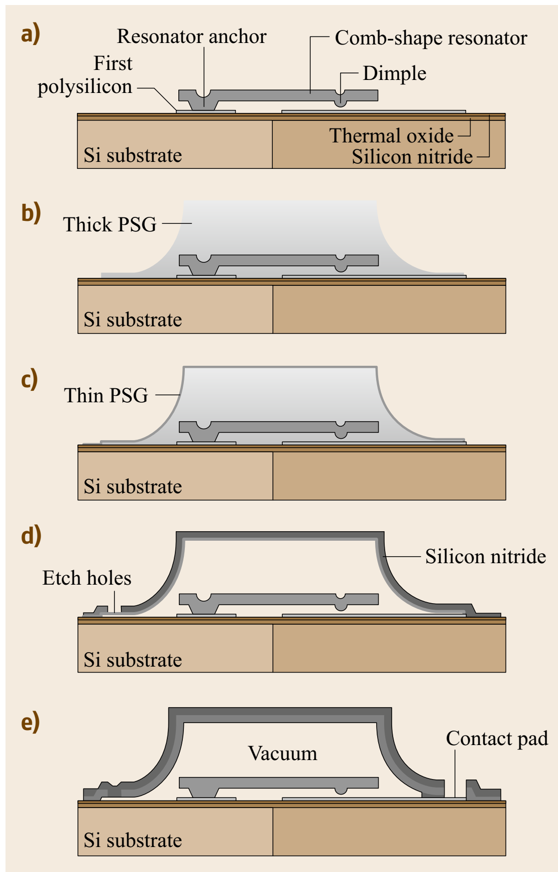

Fig. 43.3a–e Integrated vacuum encapsulation process using LPCVD nitride sealing to package micromechanical resonators. **(a)** Surface micromachining; **(b)** microshell; **(c)** etch channels; **(d)** etching and drying; **(e)** sealing (after [43.76])

tures. In the MEMS postpackaging process, a thick (7 µm) layer of phosphorus-doped glass (PSG) is deposited to cover the microstructure and patterned by using 5 : 1 buffered HF (BHF) to define a microshell area, as shown in Fig. 43.3b. A thin PSG layer of 1 µm is then deposited and defined to form etch channels, as illustrated in Fig. 43.3c. The microshell material, low-stress silicon nitride, is now deposited with thickness of 1 µm. Etch holes are defined and opened on the silicon nitride layer by using a plasma etcher. Silicon dioxide inside the packaging shell is now etched away using concentrated HF, and the wafer is dried by using the supercritical CO_2 drying process [43.82]. The result after these steps is shown in Fig. 43.3d. A 2 µm-thick LPCVD low-stress nitride is then deposited at pressure of 300 mTorr to seal the shell in the vacuum condition. Finally, the contact pads are opened, as shown in Fig. 43.3e. Figure 43.4 shows a scanning electron

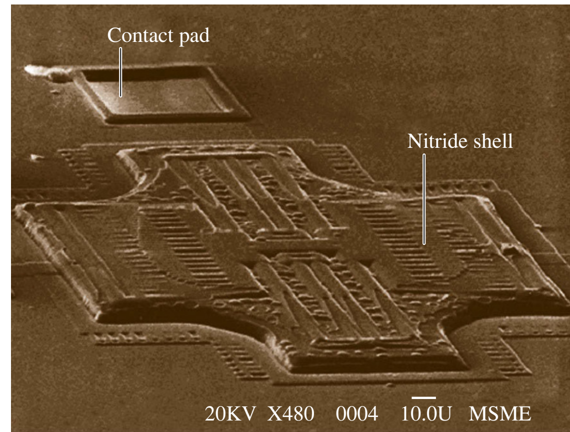

Fig. 43.4 SEM image showing a MEMS mechanical comb-shaped resonator vacuum-packaged using integrated LPCVD sealing as depicted in Fig. 43.3 (after [43.76])

microscopy (SEM) image of a finished device with a protective microshell on top. The total packaging area (microshell) has dimensions of about $400 \times 400\,\mu m^2$. A contact pad is shown with the covering nitride layer removed. The shape of the microresonator, with beams 150 µm long and 2 µm wide, is reflected on the surface of the microshell due to the integrated packaging process. The total height of the nitride shell is 12 µm, as seen standing above the substrate. Spectral measurements of the comb resonator inside the packaging revealed that a vacuum level of about 200 mTorr is accomplished using this method [43.83].

Similarly, *R. Aigner* et al. [43.84] reported a Bi-CMOS-compatible, integrated vacuum sealing process to package a polysilicon microaccelerometer. The protective shell was a polysilicon layer with supporting pillars anchored on the structural polysilicon. Release was achieved using a HF gas-phase etching process to remove the sacrificial oxide layer, and the release holes were sealed in a vacuum environment. The device was then injection molded into a plastic package at pressure of 100 bar. The supporting pillars were strong enough to hold the polysilicon shell under this high-pressure molding process.

An integrated sealing process based on evaporation of aluminum has also been reported [43.85]. A silicon substrate was deposited with a 4 µm-thick epitaxial n-type silicon layer. A controlled plasma etching and oxidation process formed a sharp tip, and a layer of borophosphosilicate glass (BPSG) was used to fill the trench as a sacrificial layer. The nitride sealing cap was deposited and patterned, and a 290 nm-thick PSG sacrificial release via was deposited and patterned, followed by deposition and patterning of the polysilicon anode. After the release etching process, aluminum evapora-

tion was applied in a 2×10^{-6} Torr vacuum chamber to deposit an 800 nm-thick aluminum layer to seal the release via. The resulting pressure was estimated as 1 mPa by measuring vacuum diode characteristics.

Other similar processes based on the integrated encapsulation concept have been demonstrated; For example, *Sniegowski* et al. [43.86] developed a reactive sealing method to seal vibratory micromachined beams; *Ikeda* et al. [43.79] used epitaxial silicon to seal microstructures; *Mastrangelo* et al. [43.87] used silicon nitride to seal mechanical beams as light sources; *Smith* et al. [43.88] used the approach of embedding microstructures and CMOS circuitry. All of these approaches integrate the encapsulation process within the MEMS fabrication process. The typical advantage of this approach is that such devices are ready for standard IC packaging processes such as dicing, pick-and-place, etc. once the wafer-level integrated sealing processes are completed. Specifically, SiTime has used a similar vacuum integration process to make their time-reference resonators [43.89].

Although the above vacuum sealing processes can successfully achieve MEMS hermetic and vacuum packaging, they suffer from some drawbacks; For example, these postpackaging processes are highly process dependent and are not suitable for generic MEMS postpackaging. MEMS companies or researchers have to adapt these postpackaging processes for their own device manufacturing process. Currently, standard MEMS foundry services do not support any of these integrated processes. Also, integrated encapsulation does not enable control of the cavity pressure, although it can achieve low pressure by wafer-level fabrication and provide lower manufacturing cost.

43.2.2 Postpackaging Processes

The second approach is defined as postpackaging processing. Such a packaging process starts when the device fabrication processes are completed, so this approach has high flexibility for various microsystems; For example, Fig. 43.5 shows a common industrial hermetic postpackaging technique called dual-in-line packaging (DIP) [43.90, 91]. A die is placed inside a ceramic holder covered by a sealing lid. Solder or ceramic joining is generally used for assembling the lid and holder under a pressure-controlled environment. High cost is the major drawback of this method, because of the expensive ceramic holder and low fabrication throughput. Another example postpackaging method is based on wafer bonding techniques combined with microshell encapsulation. Devices are sealed by stacking another micromachined silicon or glass substrate, as illustrated in Fig. 43.1. Integrated microsystems and

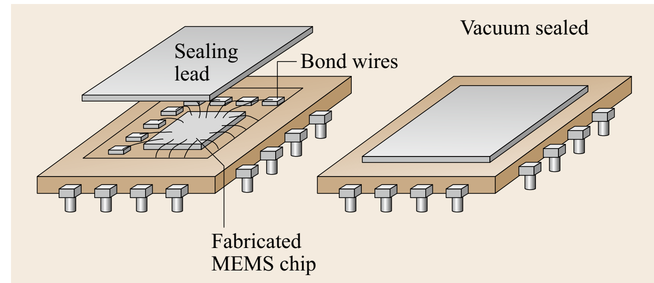

Fig. 43.5 Schematic of industrial post-packaging (DIPs) using a ceramic holder to be covered by a sealing lid

protection shells are fabricated on different wafers, either silicon or glass, at the same time. After the two substrates are assembled together using silicon fusion, anodic, or low-temperature solder bonding to achieve the final encapsulation, these microshells provide mechanical support, thermal paths, or electrical contact for the MEMS devices. Low packaging cost can be expected due to wafer-level processing.

A special heating method using rapid thermal processing (RTP) for wafer bonding applications is explained here to illustrate the roles of various control parameters such as temperature, time, and intermediate bonding materials. *Chiao* and *Lin* [43.92] reported a wafer bonding process by melting an intermediate filler material to facilitate sealing of micromechanical structures. Figure 43.6a shows the concept of the bonding and sealing scheme using an aluminum-to-glass bonding system, while Fig. 43.6b shows the experimental setup for aluminum-to-nitride bonding with integrated comb resonators inside. Aluminum with thickness of 3–4 μm was patterned to form sealing rings that surround the micromechanical structures on the device wafer. The width of a typical aluminum sealing ring was 100–200 μm, and the sealing area was $600 \times 600\,\mu m^2$. A glass (Pyrex, Corning 7740) wafer was used as the cap to cover the MEMS devices. The heating and bonding energy was provided by RTP; a typical heating history is shown in Fig. 43.7, where the overall heating process can be completed in 1 min, during which the temperature rises from room temperature to 990 °C then decreases to 350 °C. The aluminum-to-glass bonding and joining process was accomplished by heating at 990 °C for 2 s in the RTP chamber. It was shown that aluminum could extract oxygen to form aluminum oxide to create the bond [43.93]. Figure 43.8 shows a microheatuator successfully packaged using this bonding process; the surrounded liquid, isopropanol alcohol (IPA) in this case, was sealed without penetrating inside the package.

Other material systems have also been bonded using this RTP process, e.g., aluminum-to-silicon nitride

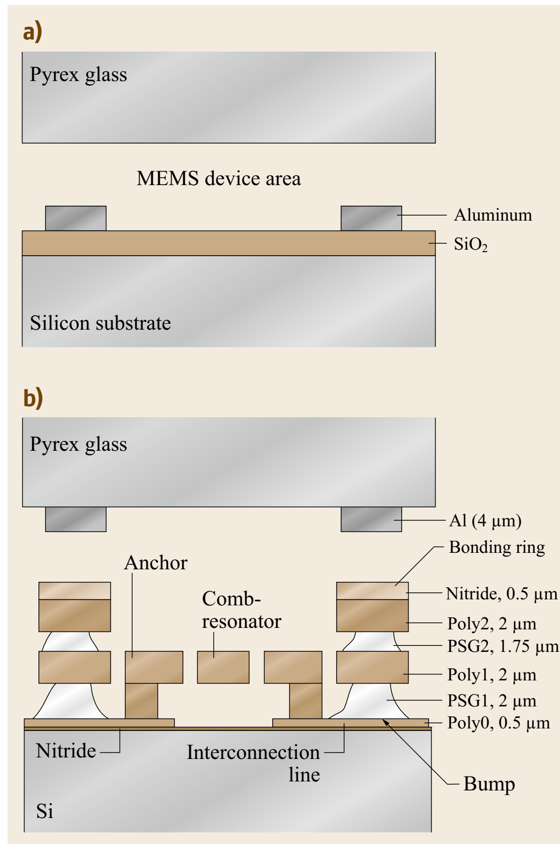

Fig. 43.6a,b Schematics of RTP bonding experiments: **(a)** the concept of aluminum-to-glass bonding, and **(b)** aluminum-to-nitride bonding with comb resonators

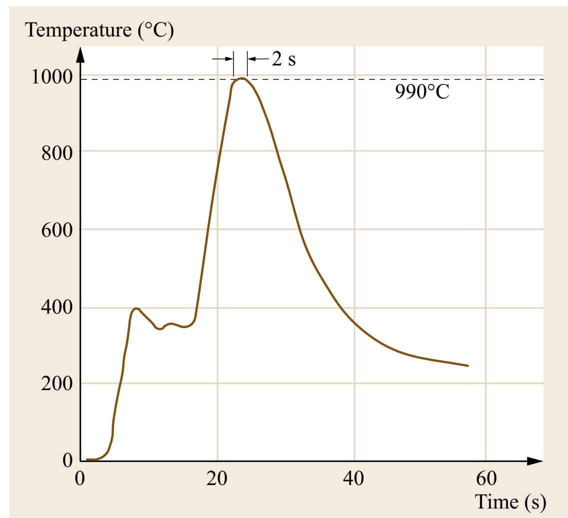

Fig. 43.7 Temperature history in an RTP bonding experiment

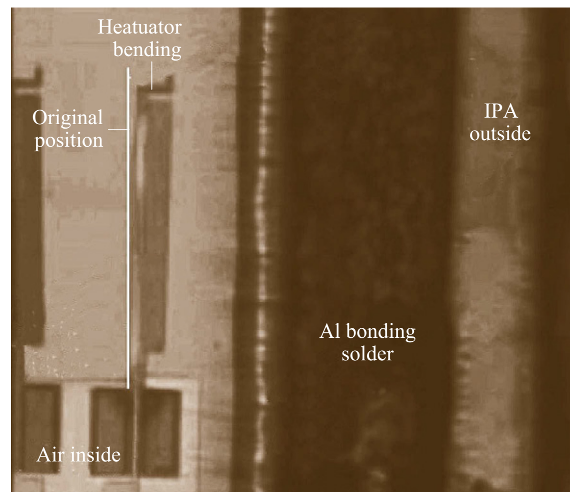

Fig. 43.8 A hermetically packaged microheatuator operating when immersed in liquid

joining (Fig. 43.6b) [43.94]. In this case, a 5000 Å-thick LPCVD silicon nitride layer was deposited and patterned on top of sealing ring structures that encompassed surface-micromachined comb-shaped resonators [43.81]. Using RTP with process time of 10 s at the peak temperature of 750 °C, a stable bond was formed at the aluminum–nitride interface. Figure 43.9 shows a packaged comb resonator that resonated at 19.6 kHz when immersed in deionized (DI) water, as seen under an optical microscope. The aluminum-to-nitride seal successfully blocked water from entering the package. To examine the bonding strength, the package was forcefully broken, as shown in Fig. 43.10. The glass debris was attached to the sealing ring surrounding the comb-drive resonator on the silicon substrate. This shows that the bonding strength of the aluminum-to-nitride system was greater than the glass fracture strength, which is estimated at around 270 MPa [43.95].

A vacuum sealing process using RTP bonding is discussed here in detail to address the technical issues in vacuum sealing processes. *Chiao* and *Lin* [43.96] reported a vacuum sealing process based on aluminum-to-nitride bonding using RTP. The RTP bonding process was conducted in a vacuum quartz tube, as shown in Fig. 43.11. Both device and cap wafers must be baked in vacuum at 300 °C for at least 4 h to drive out water and gas species that may adhere at the wafer surface [43.97]. This prebaking process in vacuum was necessary to minimize the outgassing effect during the bonding process in order to achieve high-quality vacuum. Afterwards, the device and cap wafers were immediately flip-chip-assembled, loaded into a sample holder, and placed inside a quartz chamber, as shown in Fig. 43.11. The system was then placed inside the RTP

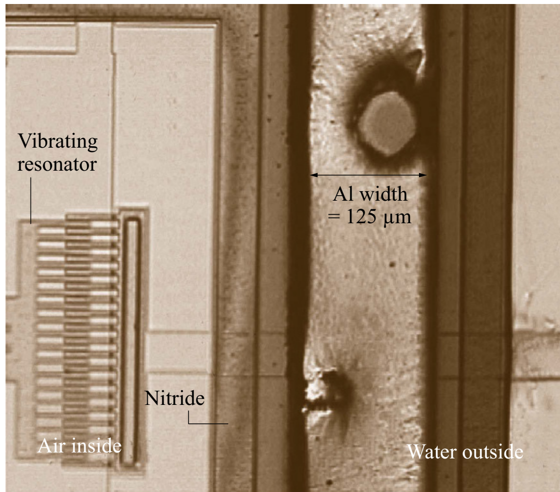

Fig. 43.9 A comb-drive resonator sealed in a a package chip and operating when the package was immersed in water

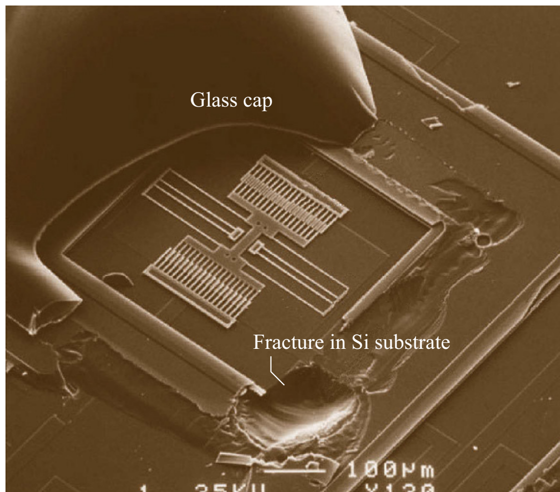

Fig. 43.10 SEM micrograph of a silicon substrate after forcefully breaking the aluminum-to-nitride bond. Glass debris was found attached to the silicon substrate

equipment, and the base pressure was pumped down to about 1 mTorr using a turbopump. The vacuum was held steady for 4 h to drive out gas trapped inside the package cavity [43.98]. The bonding and vacuum sealing process was achieved by RTP heating for 10 s at 750 °C to complete the bonding process.

Figure 43.12 shows the spectrum of a vacuum-packaged, double-folded beam comb-drive resonator measured using a microstroboscope. The central resonant frequency is at about 18 625 Hz, and the quality factor is extracted as 1800 ± 200, corresponding to a pressure level of about 200 mTorr inside the package [43.98]. This type of postpackaging process at wafer level has become the preferred approach for hermetic encapsulation, because it can provide lower cost and greater process flexibility. However, the packaging process relies on *good* bonding techniques. A strong and reliable bond between the two substrates should be provided, and the bonding procedure should be compatible with the other microsystem fabrication processes.

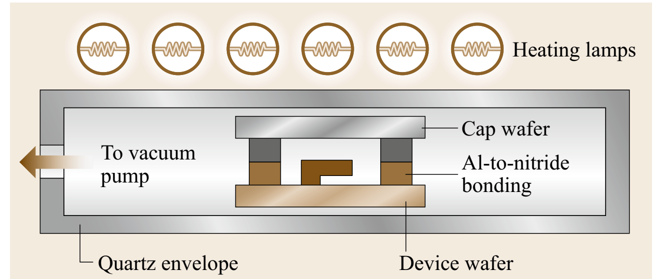

Fig. 43.11 Vacuum packaging apparatus for aluminum-to-nitride bonding using RTP

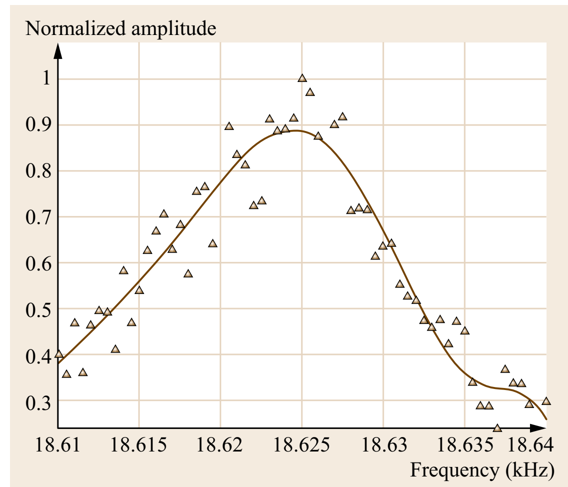

Fig. 43.12 Spectrum of a comb-shaped resonator vacuum-encapsulated by aluminum-to-nitride bonding using RTP (after [43.41])

43.2.3 Localized Heating and Bonding Processes

The approach of MEMS postpackaging by localized heating and bonding is proposed to address the problems of global heating effects. In this section, resistive microheaters are used as an example to provide localized heating, although several other means of localized heating have also been demonstrated, including laser welding [43.99], inductive heating [43.100], and ultrasonic bonding [43.101]. The principle of localized

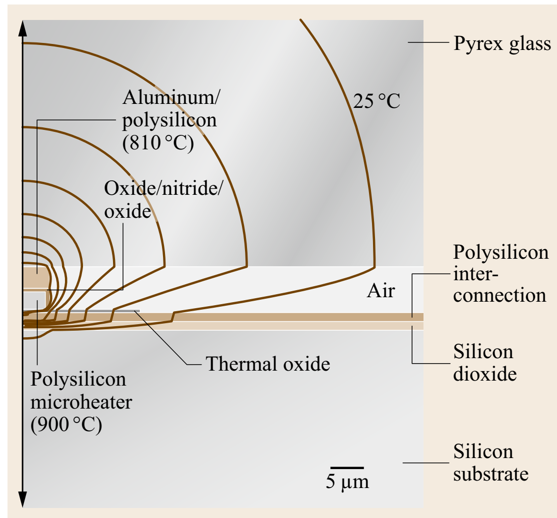

Fig. 43.13 Schematic of the 2-D heat transfer model with geometry and boundary conditions

heating is to achieve high temperature for bonding locally while maintaining low temperature globally at wafer level. Resistive heating by using microheaters on top of the device substrate is applied to form a strong bond with the silicon or glass cap. According to the results of two-dimensional (2-D) heat conduction finite element analysis (Fig. 43.13), the steady-state heating region of a 5 μm-wide polysilicon microheater capped with a Pyrex glass substrate can be confined locally as long as the bottom of the silicon substrate is constrained to ambient temperature. The physics of the localized heating behind this design can be understood by solving the governing heat conduction equations for the device structure without a cap [43.98]. As long as the width of the microheater and the thickness of the silicon substrate are much smaller than the die size and a good heat sink is placed underneath the silicon substrate, heating can be confined locally. The temperature of the silicon substrate can be kept low or close to room temperature. Several localized resistive heating and bonding techniques have been successfully developed for packaging applications, including localized silicon-to-glass fusion bonding, gold-to-silicon eutectic bonding, and localized solder bonding. Several solder materials have been successfully tested, including PSG, indium, and aluminum alloy [43.102].

The vacuum packaging example presented in this section is based on the localized aluminum/silicon-to-glass solder bonding technique. Built-in folded-beam comb drive μ-resonators are used to monitor the pressure of the package. Figure 43.14 shows the fabrication process for the package and resonators. Thermal oxide (2 μm) and LPCVD Si_3N_4 (3000 Å) are first deposited on a silicon substrate for electrical insulation, followed by deposition of 3000 Å LPCVD polysilicon. This polysilicon is used as both the ground plane and the electrical interconnect to the μ-resonators, as shown in

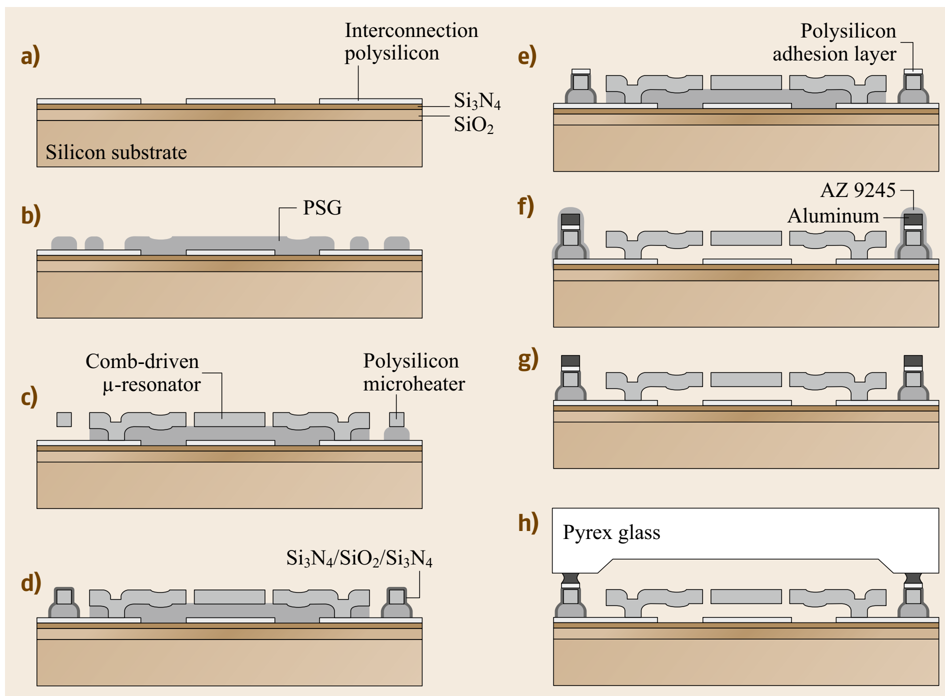

Fig. 43.14a–h Schematic process flow of vacuum encapsulation using localized aluminum/silicon-to-glass bonding. **(a)** Deposition and patterning; **(b)** sacrificial layer; **(c–g)** surface micromachining; **(h)** vacuum packaging

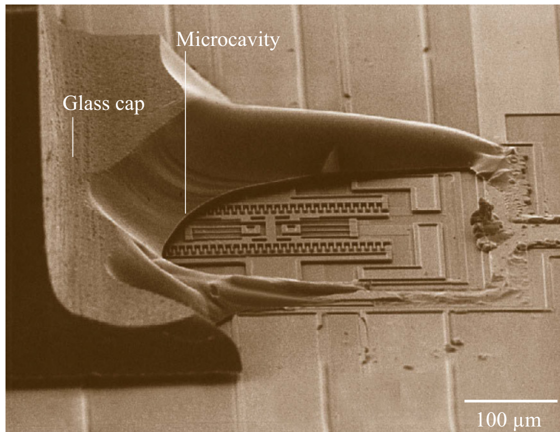

Fig. 43.15 SEM micrograph of encapsulated microresonators after the glass cap was forcefully broken

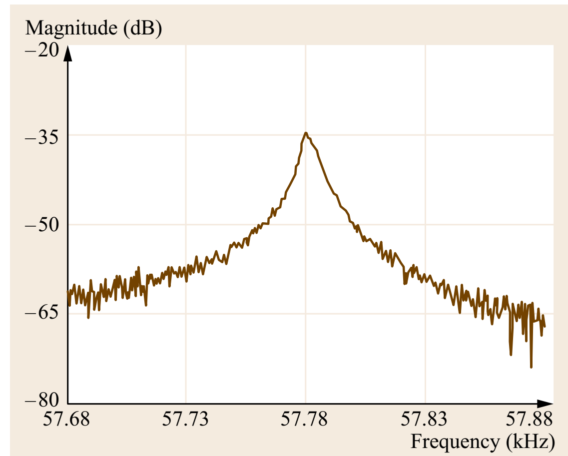

Fig. 43.16 Transmission spectrum of a glass-encapsulated μ-resonator after 120 min pump-down time in vacuum environment ($Q = 9600$)

Fig. 43.14a. Figure 43.14b shows a 2 µm LPCVD SiO_2 layer that is deposited and patterned as a sacrificial layer for fabrication of the polysilicon μ-resonators using a standard surface micromachining process. 2 µm-thick phosphorus-doped polysilicon is used as both the structural layer for the microresonators and the on-chip microheaters. This layer is formed over the sacrificial oxide in two steps to achieve a uniform doping profile. Lower input power and better process compatibility are two major advantages of using such on-chip microheaters for glass packages. The resonators are separated from the heater by a short distance of 30 µm, to effectively prevent their exposure to the high heater temperature, as shown in Fig. 43.14c. This concludes the fabrication of the μ-resonators.

To prevent the current supplied to the microheater from leaking into the aluminum solder during bonding, a LPCVD Si_3N_4 (750 Å)/SiO_2 (1000 Å)/Si_3N_4 (750 Å) sandwich layer is grown and patterned on top of the microheater, as shown in Fig. 43.14d. Figure 43.14e,f show how the aluminum (2.5 µm) and polysilicon (5000 Å) bonding materials are deposited and patterned. Sacrificial release is the final step to form the free-standing μ-resonators. Figure 43.14f shows how thick AZ 9245 photoresist is applied to cover the aluminum/silicon-to-glass bonding system to ensure that the system can withstand attack from concentrated hydrofluoric acid. After 20 min of sacrificial release in concentrated HF, the system as shown in Fig. 43.14g is ready for vacuum packaging. A Pyrex glass cap with a 10 µm-deep recess is then placed on top with applied pressure of ≈ 0.2 MPa under 25 mTorr vacuum, and the heater is heated using 3.4 W input power (the exact value depending on the design of the microheaters) for 10 min to complete the vacuum packaging process, as shown in Fig. 43.14h.

To evaluate the integrity of resonators packaged using such localized aluminum/silicon-to-glass solder bonding, the glass cap was forcefully broken and removed from the substrate. No damage was observed on the μ-resonator. A part of the microheater was stripped away, as shown in Fig. 43.15, demonstrating that a strong and uniform bond could be achieved

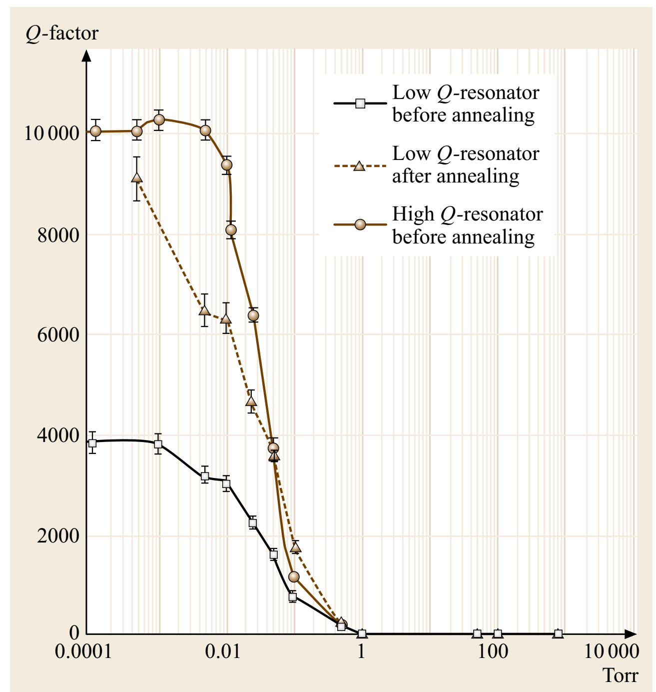

Fig. 43.17 Measured Q-factor versus pressure for unpackaged μ-resonators

without detrimental effects on the encapsulated device. Figure 43.16 shows a vacuum-encapsulated unannealed μ-resonator ($\approx 57\,\mathrm{kHz}$) after 120 min of wait time. The Q-factor measured after packaging was 9600. Q versus pressure measurements for a high-Q unpackaged μ-resonator (Fig. 43.17) demonstrated that the pressure inside the package was comparable to the vacuum level in the packaging chamber.

Postprocess packaging using the localized heating and bonding technique includes four basic components:

1. An electrical and thermal insulation layer such as silicon dioxide or silicon nitride for localized heating
2. Resistive microheaters to provide the heating source for localized bonding
3. Bonding materials such as metal or polysilicon to provide good bonding and hermeticity with the silicon or glass substrate
4. A good heat sink under the device substrate to ensure localized heating during the bonding experiments.

MEMS devices are fabricated on the device chip then hermetically sealed in a cavity formed by the device chip, resistive microheaters, and protective cap. The process can be either die level or wafer level. A schematic design for the wafer-level packaging process is shown in Fig. 43.18. The resistive microheaters are parallel to each other and connected together to ensure that identical current density is applied for individual packages at the same time. These heaters can be fabricated on either the chip or protection cap and can be built on a larger wafer for current inputs. The interconnections for these packaging cavities can be built in the dicing area, such that no extra space is required for the packaging process.

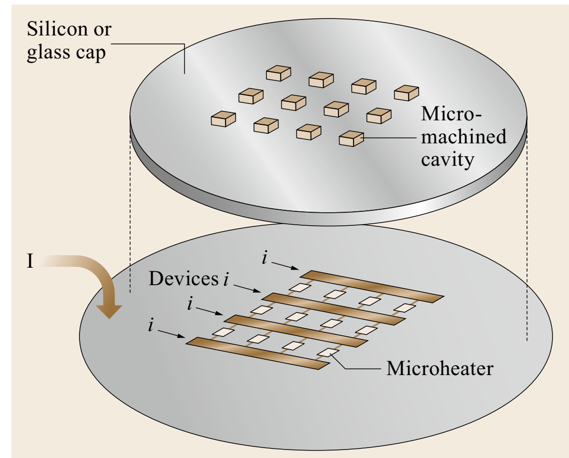

Fig. 43.18 Illustration of wafer-level vacuum packaging using the localized heating and bonding technique

43.3 Emerging Packaging Approaches

Wafer-level packaging and 3-D packaging have undoubtedly been the hottest emerging packaging technologies over the past few years and will be the trend in the near future [43.103, 104]. The process of packaging a wafer before dicing is called wafer-level packaging. Modern MEMS packaging usually involves at least three wafers, namely the application-specific integrated circuit (ASIC) wafer, the MEMS device wafer, and the cap wafer. These wafers are fabricated separately and bonded layer by layer to form the complete package. It is advantageous to encapsulate the MEMS devices early in the wafer processing to protect them mechanically and prevent contamination during subsequent fabrication and packaging processes. In this way, extra packaging equipment and repeated assembly processes can be largely eliminated. By dicing the bonded wafers at the end of the processes, one can obtain a large number of packaged chips with desired small footprint. For production of practical MEMS devices, this can reduce the cost of packaging and testing, and also improve yield and reliability. Meanwhile, 3-D packaging enables the combination of dissimilar classes of materials and components into a single system. Therefore, high-performance materials and subsystems can be combined in ways that would otherwise not be possible, thereby forming complex and highly integrated micro- or nanosystems; For example, polymers are being actively used for various MEMS sensors and actuators [43.105]. They provide many advantages in terms of cost, materials properties, and ease of processing. Integration of polymers for structural or functional purposes into microsystems is also a promising emerging technology with great potential for use in MEMS packaging.

43.3.1 Wafer-Level Packaging

Wafer-level packaging approaches for various applications can be classified into two categories:

- Interfacial bonding or bonding with intermediate melting materials
- Deposition sealing.

Mechanical protection of MEMS devices is realized by bonding a cap wafer on top of the device wafer, or by sealing of surface-micromachined cavities by deposition. Meanwhile, electrical feedthrough is needed for interconnection with the encapsulated MEMS. Normally, metal is used as the feedthrough material, while highly doped silicon can also be employed. In general, this is realized by either lateral feedthrough on the chip surface or vertical feedthrough using a through-hole via.

Wafer-Level Packaging by Interfacial Bonding

Transparent Pyrex glass wafers have thermal expansion coefficient similar to silicon wafers, and they are frequently used as cap wafers. In addition, interfacial bonding between metal and metal can also be employed. Electrical feedthrough is usually achieved using vias in the cap wafer. If silicon is used as the cap wafer, the thermal stress caused by thermal expansion mismatch between the device and cap wafers can be reduced, and holes in the cap wafer can be made using DRIE of silicon; For example, the fabrication process developed for film bulk acoustic resonator (FBAR) filters (RF MEMS devices) is shown in Fig. 43.19 [43.106]. Gold is electroplated using a photoresist mold, and the silicon substrate is etched by DRIE. The silicon cap wafer is bonded to the MEMS device wafer by Au–Au thermocompression bonding, and the etched holes are exposed by grinding the cap wafer. Finally, the packaged wafer is diced into individual chips, and wire bonding is carried out inside the exposed holes. In addition to Au–Au thermocompression bonding [43.107, 108], similar Al–Al [43.109] and Cu–Cu [43.110] thermocompression bonding can also be employed to achieve wafer-level packaging. Metal bonding surfaces are brought into contact with the application of force and heat simultaneously. Due to surface oxidation, high temperature is usually required to achieve high bonding quality, but MEMS packaging can be achieved at adequately low temperatures of about 300 °C or below. It has been demonstrated that Al-to-Al bonding can achieve wafer-level hermetic sealing and 3-D interconnects of MEMS devices [43.109]. Figure 43.20 shows wafer-level packaging processes employing Al-to-Al bonding and through-silicon vias (TSVs). After thermal oxidation for electrical isolation of the vias, highly doped poly-Si is deposited to fill the vias completely to form electrical signal paths. On the cap wafer, 2 μm-thick Al (with 2% Cu) is patterned at the perimeter of the individual dies as well as the input/output bond pads. On the MEMS device wafer, the seal rings and bond pads are also patterned using Al as described above. After cavity etching, the cap wafer is bonded to the MEMS wafer using Al bonding, creating both a hermetic seal around each die and conducting paths from the MEMS devices to the vias. The two wafers were bonded at ≈ 450 °C with various bond forces up to 80 kN. Leak detection on the capped device showed hermeticity of ≈ 10^{-12} cm^3 atm/s He leak rate with Al seal width as narrow as 3 μm. After back-grinding and polishing the bonded pair to expose the vias, new bond pads are formed on top of the cap wafer using standard passivation and redistribution layer (RDL) metallization. The electrical contact resistance of the Al-to-Al bonded interface was measured to be less than 1 Ω.

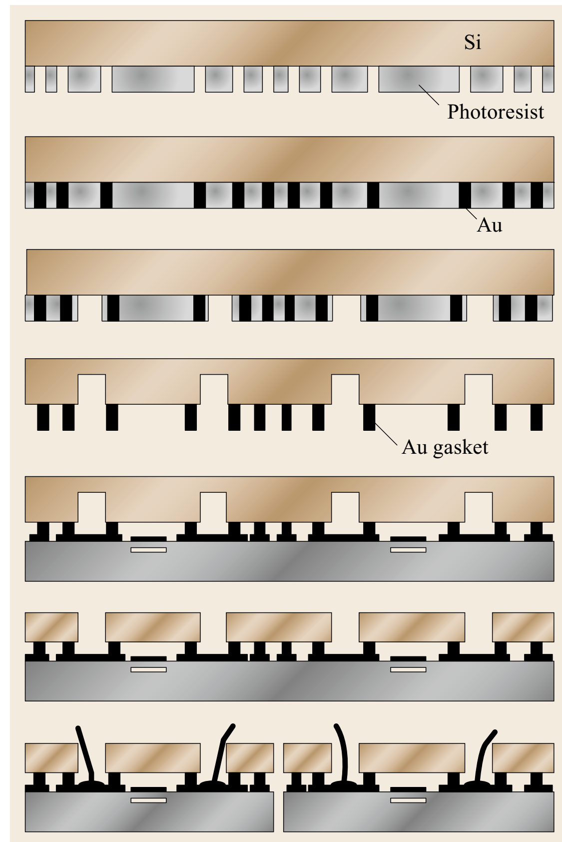

Fig. 43.19 Illustration of wafer-level packaging using metal-to-metal bonding (after [43.106])

Wafer-Level Packaging by Deposition Sealing

Narrow gaps for electrical feedthrough made between the MEMS wafer and the cap wafer can be sealed by depositing materials. Previously, an integrated process using surface-micromachined microshells was developed [43.111]. This process applies the concepts of sacrificial layer and low-pressure chemical vapor deposition (LPCVD) sealing to achieve wafer-level packaging. Similar processes have been

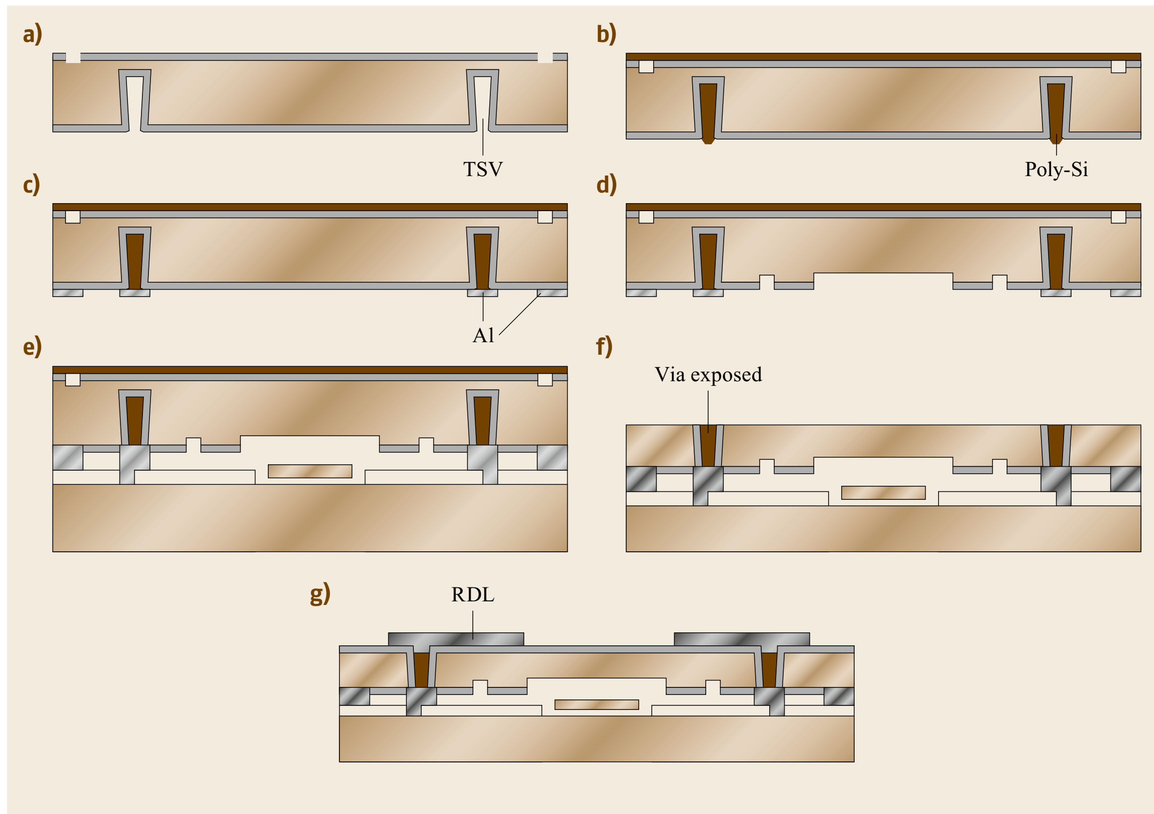

Fig. 43.20a–g Illustration of wafer-level hermetic packaging and 3-D interconnection using metal-to-metal bonding. **(a)** Etching and isolation; **(b)** filling and polishing; **(c)** deposition and patterning; **(d)** etching; **(e)** Al to Al thermo-compression bonding; **(f)** back-grinding and polishing; **(g)** passivation and interconnection (after [43.109])

demonstrated; For example, *Guckel* et al. [43.112] and *Sniegowski* et al. [43.86] developed a reactive sealing method to seal vibratory micromachined beams. *Ikeda* et al. [43.79] adopted epitaxial silicon to seal microstructures. *Mastrangelo* and *Muller* [43.113] used silicon nitride to seal mechanical beams as light sources. *Smith* et al. [43.88] presented a new fabrication technology by embedding microstructures and complementary metal–oxide–semiconductor (CMOS) circuitry. All of these methods integrate the MEMS process with the packaging process so that no extra bonding process is required. However, these schemes are highly process dependent and not suitable for prefabricated circuitry.

Sacrificial etching can also be performed through porous materials such as porous poly-Si [43.115, 116] or through a gas-permeable membrane. Sealing can be achieved by depositing material on the porous material; For example, a permeable membrane is used in Fig. 43.21 for the following process sequence [43.114]: After forming the MEMS in the silicon wafer by etching, they are covered with patterned photoresist and a polymer overcoat. Since the photoresist thermally decomposes at 200 °C, the decomposed gas diffuses out through the polymer overcoat on heating. Finally, a thin metal layer is deposited on the surface of the polymer overcoat for hermetic sealing. In addition to deposition sealing, soldering can also be employed to seal MEMS; For example, a technique to premold and transfer lead-free solder balls for MEMS/electronics packaging applications has been demonstrated [43.117].

Electrical Feedthrough

Electrical feedthrough is needed for interconnection with the MEMS encapsulated in a cavity. Normally, metals are used as the feedthrough material, because of their low resistance, while highly doped silicon can also be used to reduce potential thermal stresses. Stray capacitance and stray inductance have to be taken into account for RF MEMS. Lateral feedthrough on a chip can be realized by embedding a thin metal layer in silicon dioxide and sealing the surface by anodic bonding with a glass cap wafer [43.118]. After etching the silicon dioxide on a silicon wafer, the etched groove is

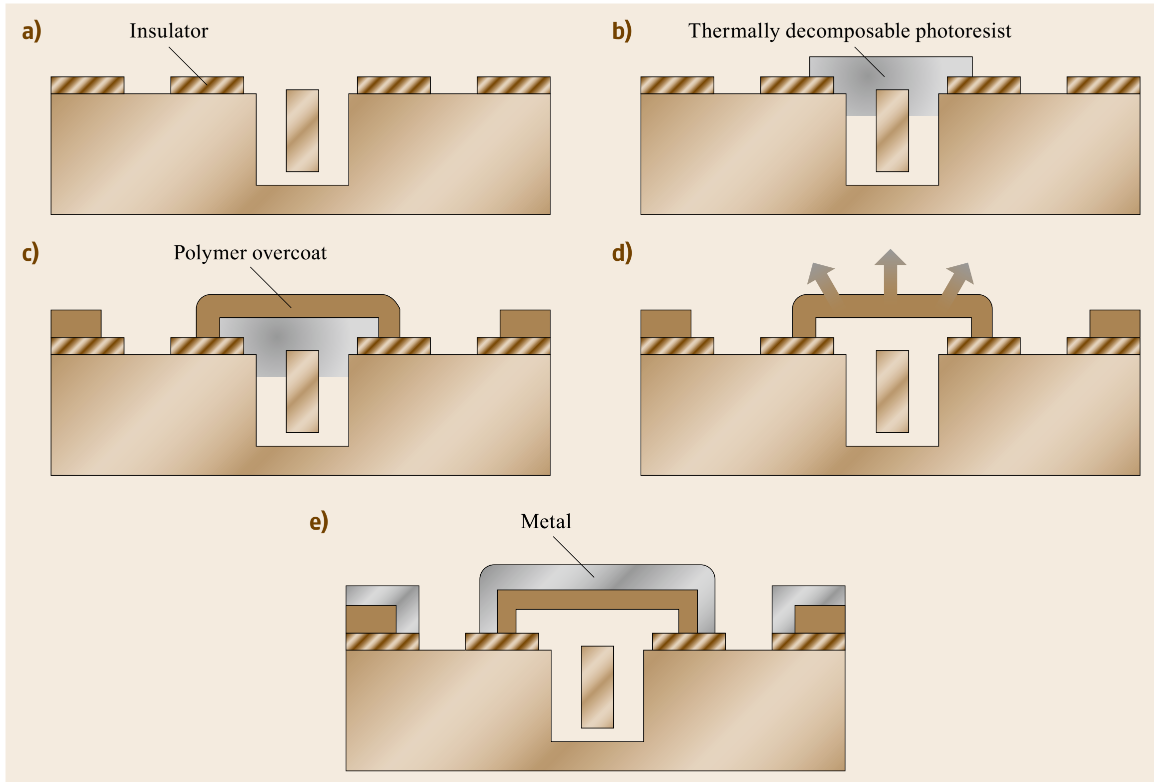

Fig. 43.21a–e Illustration of wafer-level packaging by deposition sealing. **(a)** Isolation; **(b)** cavity formation; **(c)** cap formation; **(d)** decomposition; **(e)** metallization (after [43.114])

filled with Cr–Al. The surface is coated with spin-on glass (SOG) to insulate and to make a planar surface, and silicon is sputter-deposited on it. This is anodically bonded to a Pyrex glass wafer. It was found that this lateral feedthrough is not as practically applicable compared with the vertical feedthrough described below, because the lateral feedthrough has to be fabricated on the same wafer as the MEMS.

Electrical interconnection can also be achieved using a through-hole via in the wafer, as shown in Fig. 43.22 [43.103]. The advantage of vertical feedthrough in the cap wafer is that the electrical interconnection can be fabricated on a different wafer from the MEMS wafer, so process compatibility is not required. For a glass cap wafer, it is not easy to make through holes. Meanwhile, vertical feedthrough can be achieved in a silicon wafer on which MEMS are fabricated [43.119].

43.3.2 3-D Packaging

Three-dimensional (3-D) packaging is an emerging technology that vertically stacks and interconnects multiple materials, technologies, and functional devices to form highly integrated micro- and nanosystems. Such work in the third dimension will allow exten-

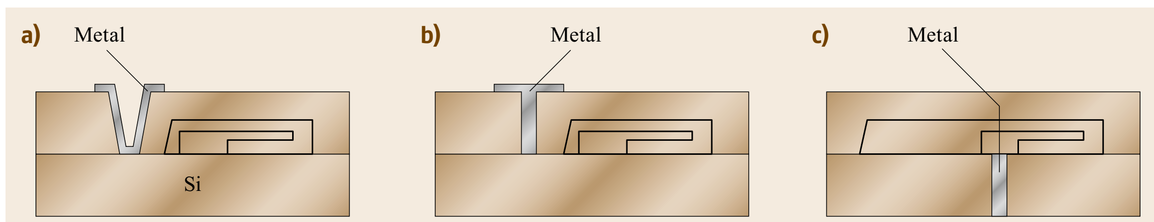

Fig. 43.22a–c Illustration of electrical feedthrough using a through-hole via in the wafer. **(a,b)** From top; **(c)** from bottom (after [43.103])

sion of Moore's law to higher density, functionality, and performance, as well as integration of more diverse materials and devices at lower cost. The potential benefits also include reduced power, small form factor, reduced packaging, and increased yield and reliability. It is recognized as an enabling technology for integration of MEMS, micro-opto-electro-mechanical systems (MOEMS), photonics, electronic ICs, and emerging NEMS.

Modern 3-D packaging technologies employ wafer-to-wafer joining, processing, and interconnection materials and components prepared using different processes. Typically they are classified into two categories: via-first approaches and via-last approaches. In via-first approaches, the vias establishing electrical (or alternatively optical) contacts between components on different substrates are defined during the bonding process. In contrast, in via-last approaches, the components are first bonded to each other, then vias to establish electrical (or alternatively optical) contacts between components on different substrates are defined. The advantages, limitations, and technological challenges of the via-first and via-last approaches are introduced in the following sections.

3-D Packaging by Via-First Approaches

Figure 43.23 shows the conceptual schemes of two major via-first 3-D packaging approaches. The bump bonding can be implemented by using, for example, solder bonding [43.120], eutectic bonding [43.121] or direct metal thermocompression bonding [43.122]. Typical dimensions of such bump-bonded metal vias are in the order of $100 \times 100\,\mu m^2$. At wafer level, it is challenging to obtain highly reliable processes for vias with dimensions below $20 \times 20\,\mu m^2$. In the technique shown in Fig. 43.23a, a completely processed and packaged MEMS device wafer containing metal bumps is bonded to a target wafer, typically a CMOS-based ASIC wafer. This technique is simply an extension of conventional chip-to-chip bump bonding to wafer-level bump bonding. Due to the minimum size of the metal bumps and the thickness of the wafer with the packaged MEMS devices, this technique allows only limited miniaturization and integration densities for the final system. In the technique shown in Fig. 43.23b, a partly processed MEMS wafer containing metal bumps is bonded to the target wafer. Thereafter, the components are further processed at wafer level to complete the MEMS devices using, e.g., etching and/or thinning processes. Although this technique allows only limited integration densities due to the minimum dimensions of the metal bumps, it has been proposed for a number of MEMS devices [43.123] and successfully implemented for commercial MEMS products [43.124].

The via-first 3-D packaging approach is being used for manufacture of gyroscopes [43.125], and combined three-axis accelerometers and three-axis gyroscopes integrated on a single chip. These devices are sold at very high volumes for consumer products such as motion controls in gaming. Taking the example of a gyroscope chip, the monocrystalline silicon capacitive gyroscope sensor and parts of the gyroscope package are prefabricated together, then bonded to the ASIC wafer that contains an etched cavity. Bonding and sealing is carried out directly to the top CMOS Al metal layer using an Al/Ge eutectic bonding process. Figure 43.24 shows a cross-sectional and top view of a gyroscope packaged using this approach [43.124].

3-D Packaging by Via-Last Approaches

In the technique shown in Fig. 43.25a, a completely processed and packaged MEMS device wafer is bonded to an ASIC wafer. Due to the thickness of the wafer containing the packaged MEMS devices, this technique allows only limited integration densities. In the techniques shown in Fig. 43.25b, a wafer containing the unpatterned MEMS device material(s) is bonded to the ASIC wafer. Thereafter, the handle wafer is released from the donor wafer. After the MEMS device material has been transferred to the ASIC wafer, it can be further processed and patterned. The vias between the devices and target wafer can then be formed. Finally, the sacrificial bond layer is removed by a selective etch. This technique has the advantage that accurate substrate-to-wafer alignment is not needed during the bonding process. The via and component positions on the target wafer are exclusively defined by the lithography and etching processes after bonding. Therefore, critical device dimensions and overlay accuracies in the nanometer range can be achieved, which is not possible with other techniques. The first MEMS device including fully functional CMOS ICs manufactured using very large-scale heterogeneous integration with a via-last approach was a 1-megapixel monocrystalline silicon micromirror array [43.126]. A polymer adhesive is used as the bonding layer, in combination with sputter-deposited aluminum vias [43.127], electroplated gold vias [43.128], or electroless-plated nickel vias [43.129]. Bonding with a polymer adhesive has the advantage that the MEMS device wafer and ASIC wafer can be bonded with very high yield and without any surface pretreatment or surface planarization. Planarized SiO_2 layers have also been proposed as an intermediate bonding layer for heterogeneous integration [43.130]. The tilting monocrystalline silicon mirrors are integrated on top of fully functional high-voltage CMOS drive electronics. The mirror array has resolution of 1 megapixel and pixel pitch of $16 \times 16\,\mu m^2$. The sil-

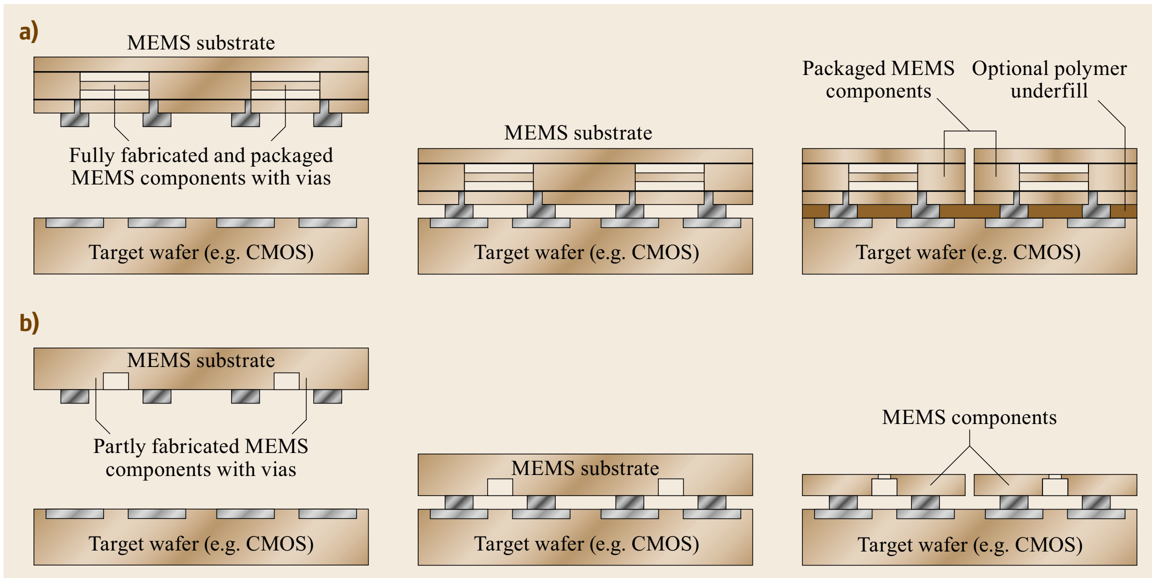

Fig. 43.23a,b Conceptual schemes of via-first 3-D packaging approaches. **(a)** Integration of fully processed MEMS components; **(b)** integration of partly processed and/or packaged MEMS components with subsequent wafer level processing (after [43.104])

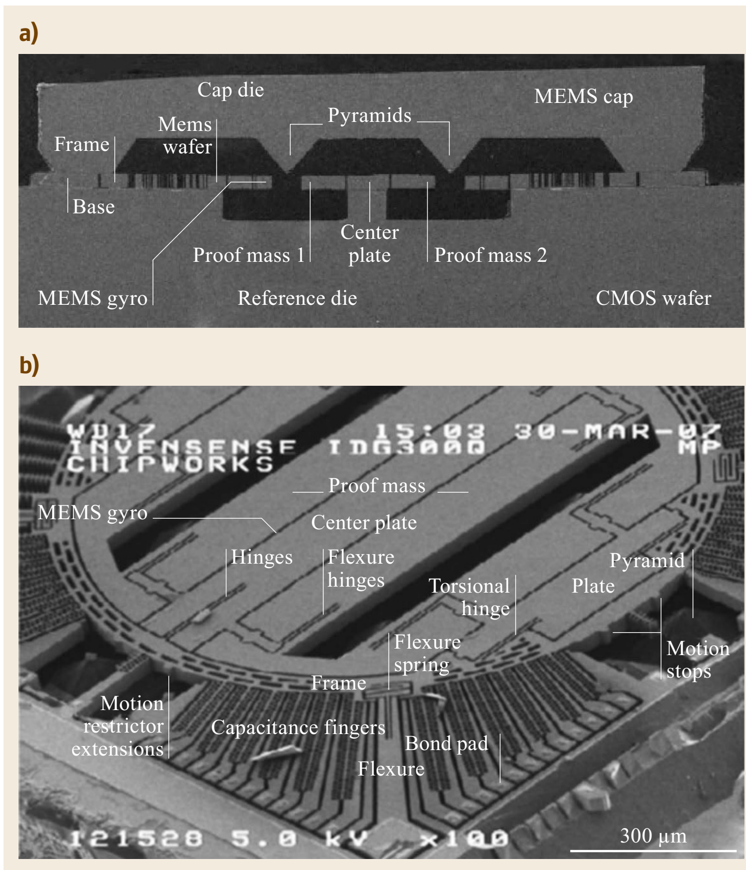

Fig. 43.24a,b Illustration of a gyroscope packaged with a via-first approach. **(a)** Cross-sectional view; **(b)** 3-D view (after [43.124], courtesy of Chipworks)

icon mirror membranes are 340 nm thick and have an extremely well-defined distance of 700 nm to the addressing electrodes on the underlying CMOS ICs. The mirror vias have diameter of 2 μm, and the torsional mirror hinges are 600 nm wide.

43.3.3 Polymer–MEMS Packaging

By using microheaters to provide heat locally for the bonding process, the global temperature can be significantly reduced to satisfy the strict low-temperature processing requirement for a variety of biomaterials and polymers. Polymeric materials are extensively utilized in microfluidic systems for applications in life sciences [43.131–133]. The advantages of polymer-MEMS include a broad range of choices of material properties, low raw material cost, and feasibility of mass production. To facilitate fabrication and application of polymer-MEMS, effective assembly and packaging processes are highly desired. In this section, two localized bonding and assembly schemes are introduced, employing soft thermoplastic materials with low glass-transition temperature as intermediate layers to demonstrate packaging of various systems, including polymer to silicon, polymer to glass, and polymer to polymer. The two packaging schemes are illustrated

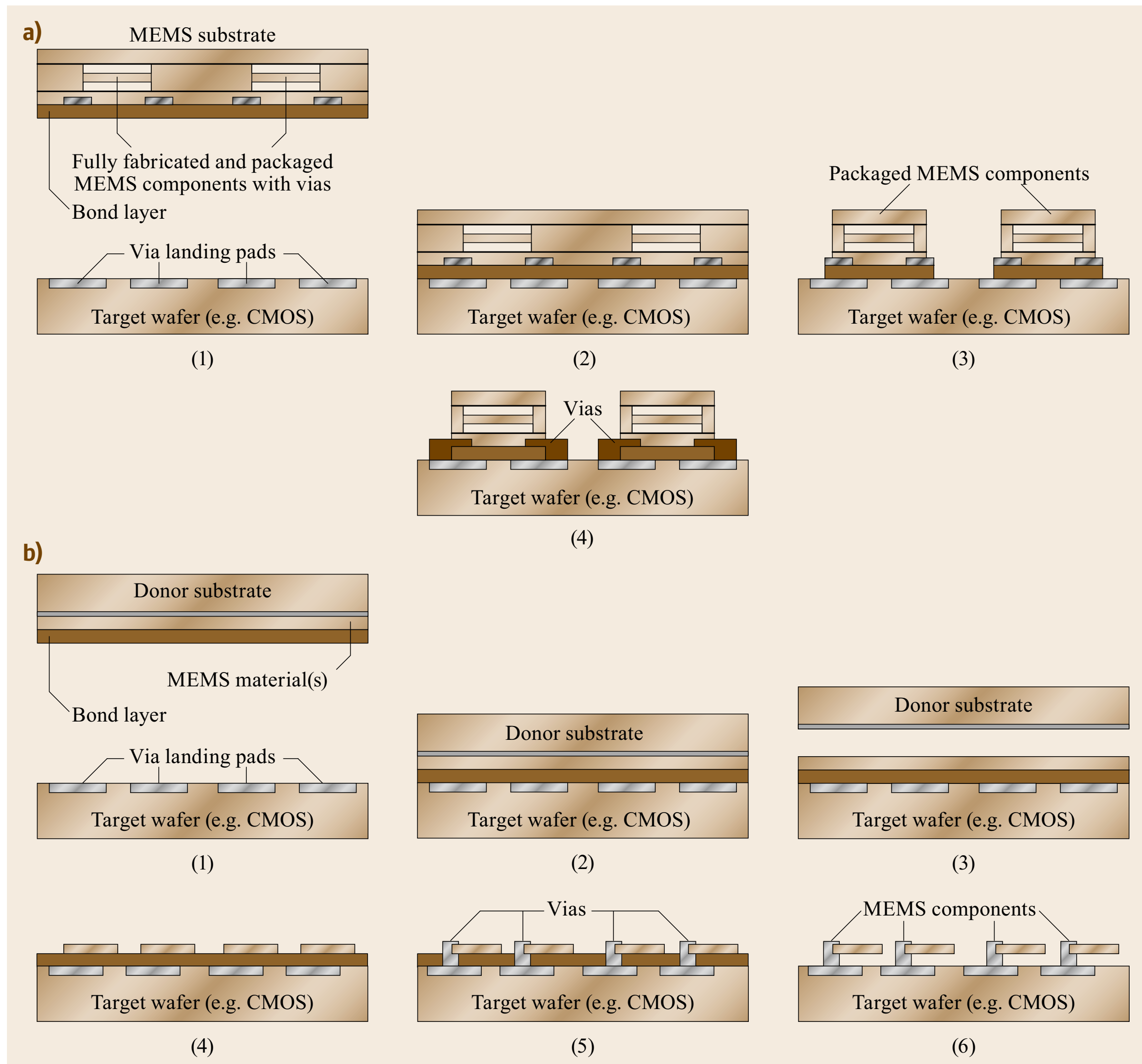

Fig. 43.25a,b Conceptual schemes of via-last 3-D packaging approaches. **(a)** Integration of fully processed and packaged MEMS components; **(b)** integration of MEMS material(s), release from donor wafer and subsequent processing of components (after [43.104])

in Fig. 43.26: (a) bonding by built-in-type heaters, and (b) bonding by external, reusable heaters.

A Mylar film (DuPont Teijin films) coated with a thermoplastic polyvinylidene chloride (PVDC) copolymer layer on one surface was bonded to either silicon, glass, or another polymeric substrate. The scheme with built-in microheaters is suitable for bonding thick polymeric materials with various types of substrate including silicon, glass, and polymer, because microheaters can easily provide the activation energy locally for bonding. Meanwhile, the scheme with external, reusable heaters is most suitable for bonding of thin polymer films to various substrates. Heat is transferred through the thin polymer film, and a heated zone is generated locally in the bonding interface where the bond is formed. In this case, it is preferable that the thin polymer film have two layers. The top layer should have high melting temperature to prevent bonding with the external reusable heaters, so that the heaters can be easily removed after completion of the bonding process and used repeatedly. Experimentally, aluminum wires of 30–70 μm width and 3 μm thickness were fabricated by a lift-off process and employed as the heating elements to form bonding loops of 1–2 mm in diameter on either silicon or glass substrates. Because of the small bonding area (less than $10^{-6}\,m^2$), about 0.4 N of force is sufficient to provide bonding pressure of 0.4 MPa. These aluminum heaters have resistance of approximately 0.8 Ω, and when voltages of 3.5 V are applied, about 15 W of power is generated locally to increase the temperature for bonding within about 0.25 s.

To test the quality of these bonding processes, several experiments were designed. In the first experiment, bonded systems were placed in a vacuum chamber and observed under an optical microscope. It was found that the top of the encapsulated chamber expanded to form a dome shape due to the 1 atm pressure difference across the membrane. The diameter of the bonding ring is 1.4 mm in this case, which corresponds to an effective area of $1.6\times10^{-6}\,m^2$, and the air permeability of Mylar is 8 cc/m^2 day atm. Based on a simplified approximation, it takes about 18 days for the air inside the cavity to diffuse out, and the membrane should return to flat. Figure 43.27 shows a SEM image of the result of Mylar bonded on PMMA. The dome shape can be observed as proof that a good seal was achieved. Afterwards, the polymer-to-polymer (Mylar-to-PMMA) bond was forcefully broken to examine the bonding interface under SEM (Fig. 43.28). It was observed that the bonding result was uniform, and part of the Mylar film was attached to the bonding substrate. Another experiment showed that direct encapsulation of water using localized heating can be achieved as a proof-of-concept demonstration of low-temperature processing. In this case, Mylar-to-PMMA bonding was performed with reusable heaters to encapsulate 0.18 μl of water in the cavity, as shown in Fig. 43.29. The close-up view at the top shows two small bubbles in the water-filled encapsulated chamber. These bubbles provide an easy way to verify the presence of water in the chamber. No leakage path can be identified, and water inside the package escapes mainly by evaporation and diffusion through the top Mylar membrane as well as the plastic substrate.

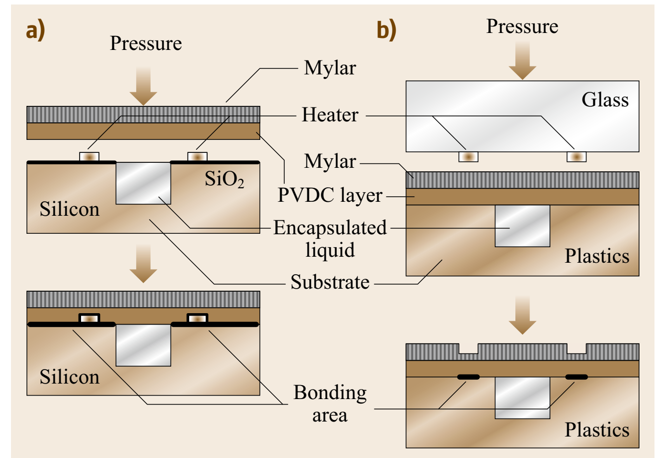

Fig. 43.26a,b Schematic illustration of polymer bonding processes in **(a)** built-in heater configuration and **(b)** reusable heater configuration

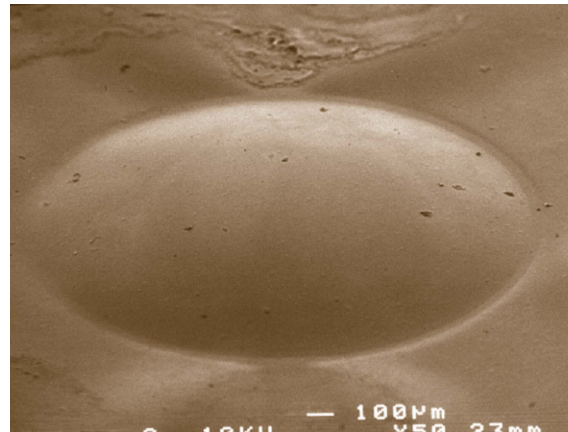

Fig. 43.27 SEM image of dome shape in Mylar membrane, demonstrating good sealing with poly(methyl methacrylate) (PMMA) (after [43.133])

In summary, among the tested bonding systems using built-in aluminum heaters, it is found that plastic-to-plastic bonding shows the highest bonding strength. In the bonding systems using silicon or glass as the

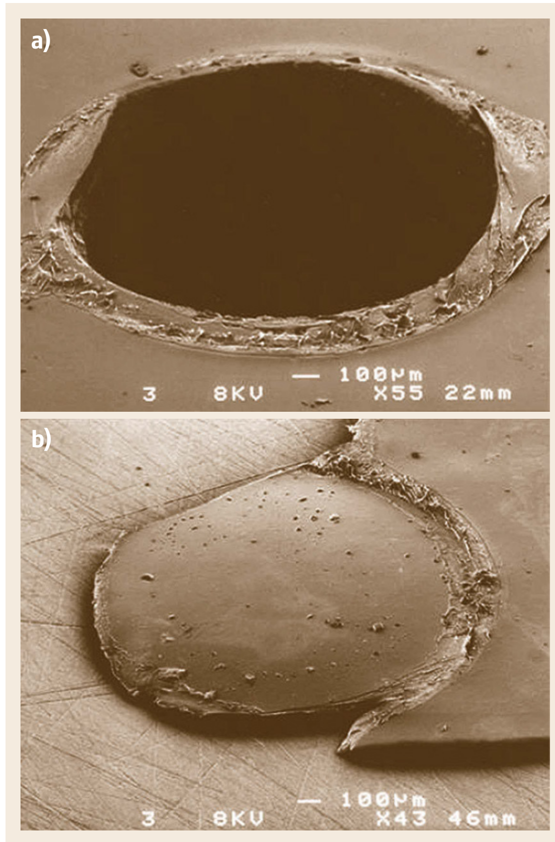

Fig. 43.28a,b SEM micrographs of bonding interface: **(a)** PMMA substrate, **(b)** Mylar layer (after [43.133])

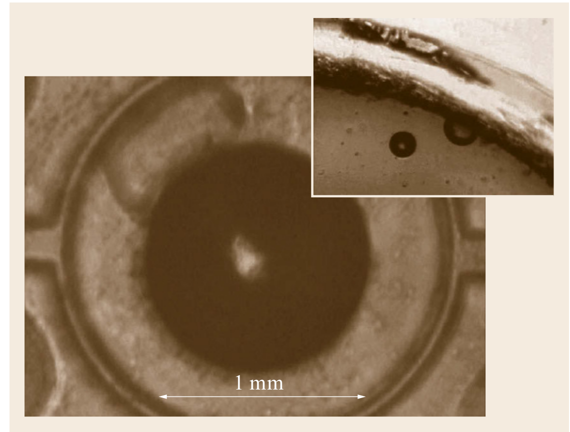

Fig. 43.29 Water encapsulation result (after [43.133])

bonding substrate, the bonding interface lies between the plastic and the aluminum heaters, and the bonding strength is lower than for plastic-to-plastic bonding but higher than that of plastic-to-silicon or plastic-to-glass bonds. Meanwhile, the plastic-to-plastic bonding process using reusable heaters shows the best bonding results as compared with plastic-to-silicon or plastic-to-glass systems. In the case of using external, reusable heaters for plastic-to-silicon and plastic-to-glass bonding systems, it is suggested that thin plastic films with (1) high adhesion chemistry with silicon and glass and (2) low melting temperature should be employed as the intermediate bonding layer to achieve high bonding quality.

43.4 Thermal Issues and Packaging Reliability

43.4.1 Thermal Issues in Packaging

The two key thermal issues related to MEMS packaging are:

- Heat dissipation from actuators and integrated circuitry components
- Thermal stress generated during the packaging process.

These two topics are discussed separately.

Heat Dissipation Issues

In an IC, heat dissipation becomes a serious problem as the size of transistors continues to shrink and their density on the chip keeps increase with advances in IC fabrication technology. The trend of packing increasing power into smaller packages has exacerbated thermal management challenges [43.134]. The electrical characteristics of transistors change with working temperature, so inefficient power dissipation that raises the working temperature can affect device performance. Present MEMS devices do not need high-power, high-performance microprocessors, so power dissipation is not a problem. Nevertheless, some functional components in packaged MEMS, such as biomaterials or laser diodes, are very sensitive to temperature variations. Several MEMS chemical sensors and other applications such as micro polymerase chain reaction (PCR) chambers for DNA replication actually require elevated temperature for operation, and microthermal platforms are built for these devices. Thermal management to maintain the working temperature of these chips for stable operation is still an essential packaging consideration. The geometrical complexity of MEMS resulting from packing various functional components into a tight space increases the difficulty of thermal

management. As the MEMS packaging integration process becomes more complex, fabrication constraints on the packaging process will have greater impact on the heterogeneous integration in front-end MEMS and IC processes; For example, a low temperature requirement for the packaging process generally limits the possible choice of materials in the back-end process. In general, conventional IC packaging employs a heat sink attached to the chip to remove heat. The heat sink is generally made of a copper or stainless-steel bar with an array of fin structures on one side for better natural or forced heat convection to dissipate heat to the environment. In addition to heat sinks, thermal vias, heat pipe cooling, immersion cooling, and thermoelectric cooling can also be used for effective heat removal. Because most MEMS packages still follow the typical IC packaging architecture, one promising thermal management method, viz. the heat pipe, is discussed for possible MEMS packaging applications.

A heat pipe is a sealed slender tube containing a wick structure and a working fluid, typically water for electronics cooling. It is composed of three sections: the evaporator section at one end, the condenser section at the other end, and an adiabatic section in the middle. In the evaporator section, heat is absorbed by the working fluid via phase transformation from liquid to vapor. In the condenser section, heat dissipates to the outside environment, and thus, the fluid returns to liquid phase. The vapor phase is in a high-pressure and high-temperature state, which forces the vapor to flow into the condenser section at a lower temperature. Once the vapor condenses and gives up its latent heat, the condensed fluid is then pumped back to the evaporator section by the capillary force developed in the wick structure. Therefore, the middle adiabatic section contains two phases: the vapor phase in the core region and the liquid phase in the wick, flowing in opposite directions and with no significant heat transfer between the fluid and the surrounding medium. Silicon has good thermal conductivity ($1.41\,\mathrm{W/(cm\,K)}$) and is easily micromachined to fabricate such heat pipes. Therefore, there is great potential for implementation of silicon micro heat pipes in IC and MEM packaging, and several approaches have been proposed on this topic [43.135–137].

Packaging-Induced Thermal Stresses

Thermal-based bonding processes have been used in MEMS packaging applications for many years, as described previously in this chapter. Thermal management is extremely important during the bonding process to avoid fracture of the substrate or MEMS devices themselves. Extremely high temperatures or rapid cooling conditions may result in damage and should be carefully evaluated both analytically and experimentally. There are many ways to provide heating energy, including electrical resistive heating, oven heating, or induction heating [43.100]. These bonding processes may be put into two categories: localized bonding, where heat is applied directly only to the adhesive material used to bond the package to the MEMS device, and global heating, where the entire system (MEMS device, adhesive, and packaging material) is heated to bond the materials, being the common approach for all MEMS packaging processes. Therefore, this section focuses on the thermal stress effects in MEMS packaging during heating and cooling procedures. The aluminum-to-glass bonding process using RTP is used as a specific example for the discussion of thermal stresses [43.92]. The bonding process heats up the packaging system to $750\,^{\circ}\mathrm{C}$ for $10\,\mathrm{s}$, then cools it back to room temperature. To simulate this process, an ANSYS program [43.138] was established to examine the shear stress due to coefficient of thermal expansion (CTE) variations in the bonding system as a result of temperature changes. The shear stress was recorded from the ANSYS analysis on the aluminum/Pyrex glass interface and the aluminum/silicon interface.

Two different models were analyzed. The first was for the quartz–aluminum–silicon bonding system, and the second was for the Pyrex glass–aluminum–silicon bonding system [43.139]. The results of the ANSYS analysis were then analyzed and compared with experimental observations. Figure 43.30 shows the ANSYS results for the Pyrex glass bonding system with aluminum solder width of $100\,\mu\mathrm{m}$; the maximum residual stress is $60\,\mathrm{MPa}$ in the glass, slightly lower than the fracture strength of Pyrex glass of $70\,\mathrm{MPa}$. It was discovered that increasing the aluminum width led to lower residual stresses. This likely occurred because the

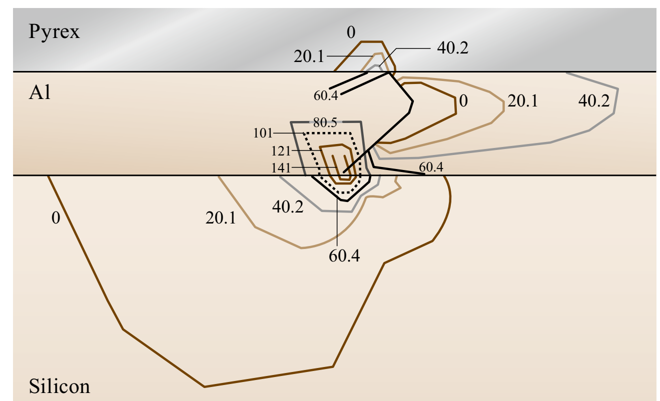

Fig. 43.30 Residual stress (GPa) for aluminum solder width of $100\,\mu\mathrm{m}$ in silicon–aluminum–glass bonding using RTP

length of the Pyrex glass, quartz, and silicon remained constant. As a result, it will always want to contract by the same amount for a constant temperature change, independent of the aluminum width. However, when increasing the aluminum width, the stress did not occur in such a concentrated area and therefore decreased; For example, the maximum residual stress analyzed from ANSYS in the Pyrex glass bonding system was 74.5, 58, and 60 GPa for aluminum width of 30, 50, and 100 μm, respectively [43.139]. Pyrex glass has documented strength of around 69 GPa [43.140]. Fracture should always occur for aluminum width of 30 μm or less, according to the ANSYS analysis. Fracture may occur sporadically at width of 50 or 100 μm, depending on the amount and magnitude of the flaws in the Pyrex glass. Experiments were carried out on the Pyrex glass bonding system with a width of 100 μm. The samples were heated up to 750 °C, then cooled down by taking them out of the oven. In all four experimental cases, small cracks were observed in the Pyrex glass, as shown in Fig. 43.31. These cracks may have occurred consistently for several reasons. First, they may be a result of handling the Pyrex glass before bonding. The Pyrex glass samples were kept in containers with each other, which may have resulted in abrasive contact and possibly caused flaws in the material. These flaws could result in reduced strength below the value of 69 GPa, so the predictions based on the ANSYS analysis could be correct. Second, it was observed that the cracks were small, only occurring tens of microns away from the aluminum and not propagating completely through the Pyrex glass. These cracks could be caused by the high stress applied, but the cracks did not reach a critical size and therefore did not propagate completely through the Pyrex glass. Therefore, the strength remained at the theoretical value of 69 GPa, and the Pyrex glass only partially cracked. Experimental analysis by *Chiao* and *Lin* [43.92] showed that fracture was not observed when using aluminum width greater than 150 μm. This is consistent with the results of the ANSYS analysis showing that, as the width of the aluminum is increased, the residual stress decreases.

ANSYS calculations were also carried out for the quartz bonding system, predicting maximum stress of 207, 117, and 100 GPa, for aluminum width of 30, 50, and 100 μm, respectively. All three of these stress values are much larger than the theoretical strength of quartz at 48 GPa, so fracture should always occur. Quartz has much higher coefficient of thermal expansion (CTE) than silicon, which explains this prediction. Experimentally, a quartz substrate was used to test silicon–aluminum–quartz bonding; the result is shown in Fig. 43.32. It was observed that cracks occurred all over the sample, causing serious damage to the quartz wafer. These cracks could be the failure mechanism of the hermetic package. Therefore, Pyrex glass was identified as a better bonding substrate than quartz.

The thermal stresses generated in the packaging process with quartz are much larger than for Pyrex glass, because of the different CTE mismatches in these two systems. Quartz has low CTE ($0.54\times10^{-6}\,K^{-1}$) compared with aluminum ($23\times10^{-6}\,K^{-1}$) or silicon ($3.5\times10^{-6}\,K^{-1}$). On the other hand, Pyrex glass has a CTE ($3.2\times10^{-6}\,K^{-1}$) much closer to those of silicon and aluminum, resulting in smaller stresses. The practical implications of the ANSYS results and the information presented above are that materials must be chosen carefully when carrying out bonding. To ensure that fracture will not occur, materials with CTE much higher or lower than that of silicon should not be used. This finding is a valuable feature of this particular packaging system and should benefit other packaging processes involving bonding of MEMS packaging, because it supports the prediction that Pyrex glass is an excellent material to bond with silicon in MEMS packaging, as long as sufficiently wide adhesive material is used.

43.4.2 Packaging Reliability

Packaging is one of the key issues to be addressed in evaluation of the reliability of MEMS products. Any

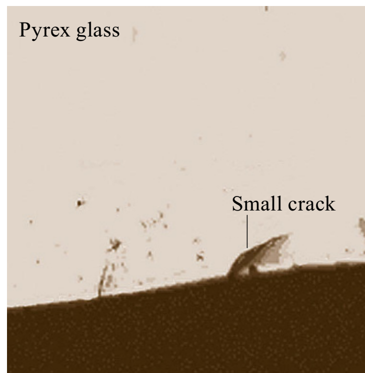

Fig. 43.31 Micrograph of experimental result for Pyrex glass–aluminum–silicon system. Small cracks can be observed

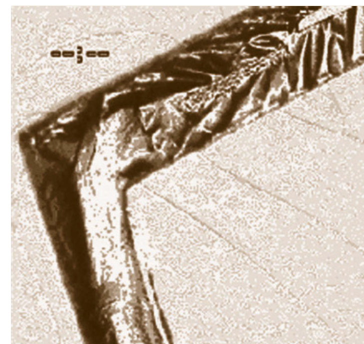

Fig. 43.32 Bonding result of the quartz–aluminum–silicon system; fracture can be observed

defects created during the sealing and packaging process may result in immediate device failure or may degrade device performance over time; For example, microaccelerometers that are used to deploy airbags in automobile safety applications require excellent reliability. If any leakage path is created during the sealing process at the two bonding interface, moisture may be able to enter the sealed microcavity and cause device failure over time. Thermal stress induced by the CTE mismatch is one of the main factors affecting packaging reliability. In fact, stress formation can occur not only during the packaging process but also during device operation. In particular, during device operation, the package will go through various temperature cycles because of environmental changes. Such temperature variation can cause expansion of packaging materials when constrained in the packaged assembly. As a result of such thermal mismatch, significant stresses are induced in the package and may finally cause device failure. In addition to thermal mismatch, corrosion, creep, fracture, fatigue crack initiation and propagation, and delamination of thin films are all possible factors that can cause failure of packaged devices [43.141]. These failure mechanisms can be prevented or deferred by using proper packaging designs; For instance, thermally induced strain inside the packaging material is generally below the tolerance of the material and cannot cause immediate catastrophic damage. However, cyclic loading can generate and accumulate stresses and eventually cause failure. Several common designs have been used in IC packaging to prolong device lifetime; For example, the strain in solder interconnects of BGA or flip-chip packaging can be effectively reduced by introducing a polymer underfill material between the chip and substrate for effective distribution of thermal stresses induced by CTE mismatch [43.142]. Such strain can be further reduced if excellent thermal paths are built around interconnects to diminish thermal stresses originated from the temperature gradient between the ambient and operation temperature. Delamination is another source of reliability problems, occurring at the interface between adjacent material layers. In MEMS, components made of dissimilar materials are commonly bonded together to provide specific functions. Delamination can result in electrical or mechanical failure of devices in the package, such as mechanically cracking through the electrical via wall to form an electrical open because of propagation of the delamination of the metal line from the dielectric layer or overheating of the die because of delamination of the die from the underlying layer to form a gap in the heat dissipation path. Because of the complex stress and thermal loading, geometry, and material properties of MEMS, development of packaging designs to increase reliability is very important and requires more extensive investigation.

Reliability testing is required before a new device can be delivered to the market. Test results can provide information for subsequent improvement of the packaging design and fabrication processes. Hence, the approach used to analyze failure data, known as *reliability metrology*, is very important in the packaging industry. This analysis method uses the mathematical tools of probability and statistical distributions to evaluate data, understand failure patterns, and identify sources of failure; For example, the failure density function is defined as the time derivative of the cumulative failure function

$$f(t) = \frac{\mathrm{d}F(t)}{\mathrm{d}t} \tag{43.1}$$

$$F(t) = \int_0^t f(s)\,\mathrm{d}s\,. \tag{43.2}$$

The cumulative failure function $F(t)$ is the fraction of a group of original devices that has failed at time t. The Weibull distribution function is one of the analytical mathematic models commonly used in packaging reliability evaluation to represent the failure density function [43.12].

$$f(t) = \frac{\beta}{\lambda}\left(\frac{t}{\lambda}\right)^{\beta-1}\exp\left[-\left(\frac{t}{\lambda}\right)^{\beta}\right], \tag{43.3}$$

where β and λ are the Weibull parameters. The parameter β is called the shape factor and measures how the failure frequency is distributed around the average lifetime. The parameter λ is called the lifetime parameter and indicates the time at which 63.2% of the devices have failed. By integrating both sides of the equation, $F(t)$ becomes

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\lambda}\right)^{\beta}\right]. \tag{43.4}$$

Using the Weibull distribution function with the two parameters extrapolated from experimental data, one can estimate the number of failures at any time during a test. Moreover, knowing the meaning and values of these parameters, one can compare two sets of test data; For example, higher λ indicates that a set of samples has longer lifetime. Because all such mathematical models are statistical approximations based on real experimental data, use of more testing samples can provide more accurate estimations.

43.4.3 Long-Term and Accelerated MEMS Packaging Tests

The ability to estimate the reliability or lifetime of a device provides valuable information for the manufacturer to maximize the profit margin by balancing the cost and quality of the product. Moreover, the warranty period given by the manufacturer has to be determined based on product reliability information. The reliability of MEMS packages is best characterized using long-term tests with statistical data analyses. However, it is very difficult to measure the reliability or lifetime of a device in a real-time fashion, because testing during a prolonged time period may be required to prompt many devices to fail. To evaluate the reliability of a device in a timely fashion, accelerated testing is normally conducted to speed up the device aging process and thus shorten the total testing time required. Accelerated testing, from the packaging and sealing point of view, is a testing method that emphasizes failure of the seal when foreign elements leak inside the microcavity, which may affect device performance. For a hermetic package, the lifetime of a MEMS device is essentially an estimation of the time required for water to penetrate into the package. For vacuum-encapsulated MEMS devices, in addition to water penetration through the seal, gas penetration or outgassing from within packaging materials such as the substrate, cap, and seal over time can degrade the vacuum level and thus device performance. Therefore, the lifetime of a vacuum-encapsulated MEMS package can be evaluated using the time for gas to evolve into the package from either the seal or device materials, whichever occurs first. Unfortunately, there are not many research publications that deal with such long-term and accelerated testing to evaluate MEMS packaging reliability. In the conventional IC packaging industry, reliability estimation is carried out using accelerated testing and statistical predictions [43.12]. Accelerated tests often utilize high temperature and high humidity, e.g., autoclave tests [43.143], to speed up corrosion of the sealing boundary and thereby accelerate package failure. The MEMS industry could use very similar accelerated tests to estimate the lifetime of a MEMS package, because the basic assumptions regarding the failure mode and humidity issues are similar to those for conventional IC packages. Several research groups have reported reliability studies on MEMS packages formed using different bonding methods and materials [43.93, 94, 144]. In this section, two MEMS packaging examples that aim to address long-term and accelerated testing are discussed.

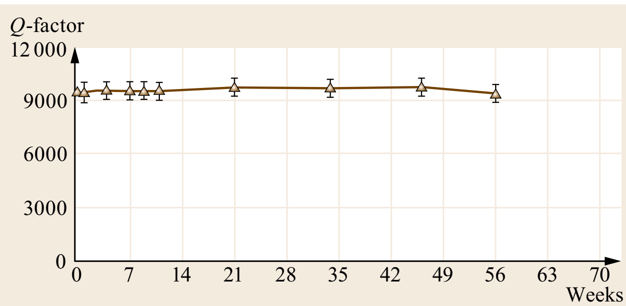

Fig. 43.33 Long-term measurement of encapsulated μ-resonators. No degradation of Q-factor is found after 56 weeks

Figure 43.33 shows long-term measurements of the Q factor of vacuum-packaged μ-resonators obtained using localized aluminum/silicon-to-glass bonding [43.93]. The vacuum encapsulation process is described in detail in Fig. 43.8. It was found that the vacuum package obtained by localized heating and bonding provided a stable vacuum environment for the μ-resonator with quality factor of 9600, showing no degradation over at least one year. Since the performance of high-Q μ-resonators is very sensitive to environmental pressure, as shown in Fig. 43.17, any leakage can be easily detected. The fact that this high Q value can be maintained for one year indicates that the packaging process was performed well and that both aluminum and Pyrex glass are suitable materials for use in vacuum packaging applications. According to a previous study of hermeticity in different materials, metal has lower permeability to moisture than other materials such as glass, epoxy, and silicon. With width of 1 μm, metal can effectively block moisture for more than 10 years [43.12]. In this vacuum packaging system, the bonding width is 30 μm, such that it can sufficiently block the diffusion process of moisture. On the other hand, the effects of diffusion of air molecules into these tiny cavities have not been studied extensively, and design guidelines for vacuum encapsulation are not clearly defined. Further investigations are needed in this area, and the example presented here serves as a good starting point.

On the other hand, accelerated testing involves placing a large number of samples in a harsh environment, such as elevated temperature, elevated pressure, and 100% humidity, to accelerate the corrosion process. Statistical failure data are then gathered and analyzed to predict the lifetime of packages under normal usage environment. As a result, the long-term reliability of the package can be predicted without going through true long-term tests. Unfortunately, accelerated testing is an area that has not been addressed in MEMS research papers. Although the MEMS industry must have done some extensive reliability tests, they do not publish the results, probably due to liability concerns. Among the

very limited publications, this section uses a specific MEMS packaging system that has gone through accelerated tests as an illustrative example [43.41].

The considered MEMS package was fabricated using RTP bonding, as described previously in this chapter. The goal of the accelerated testing was to examine the failure rate at the bonding interface. The accelerated test was started by placing the packaged samples into an autoclave chamber filled with high-temperature (130 °C) pressurized (2.7 atm) steam at 100% relative humidity for accelerated testing. Pressurized steam can penetrate small crevasses if any defect is present at the bonding interface [43.59]. The elevated temperature and humid environment speed up the corrosion process. A package was considered to have failed if water condensed or diffused into the package. The statistical data gathered from this accelerated test can be categorized as right-censored data [43.145]. Statistical failure data were gathered every 24 h by optical examination for a period of 864 h, during which new failures were seldom observed (therefore, right-censored on time axis). In practice, this method was easier and more economical to implement than other methods. Owing to the robustness of the samples, it was difficult to complete the tests to the point where all packages failed. The cumulative failure function $F(t)$ is defined as

$$F(t) = \frac{\text{Number of cumulative failures}}{\text{Number of samples, } N} , \qquad (43.5)$$

where N is the sample size at the beginning of the test. A package was considered to have failed if water condensed inside or diffused into the package; For example, water was found to diffuse into the cavity after 240 h of testing in Fig. 43.34. However, no leakage path could be identified under optical microscopy in this case. Figure 43.35 shows the function $F(t)$ (in %) plotted versus the logarithm of time. In general, most failures occurred in the first 96 h ($\ln(t) \approx 4.56$); this high number of early failures reflects a yield issue of the sealing process. Moreover, packages with smaller bonding width and larger bonding area showed higher failure percentages. Both statistical models, i. e., Weibull and lognormal [43.145], were used and compared to analyze the collected data to predict the lifetime of the packages, using the least-squares fit method to determine the best fitting model. It was found that the R^2, the coefficient of determination [43.145], values were generally in the range of 0.8 when using the lognormal model as compared with 0.5 when using the Weibull model. Therefore, the lognormal model was used to predict the lifetime of the packages.

Figure 43.36 shows the inverse standard normal distribution function versus ln(time). The maximum-

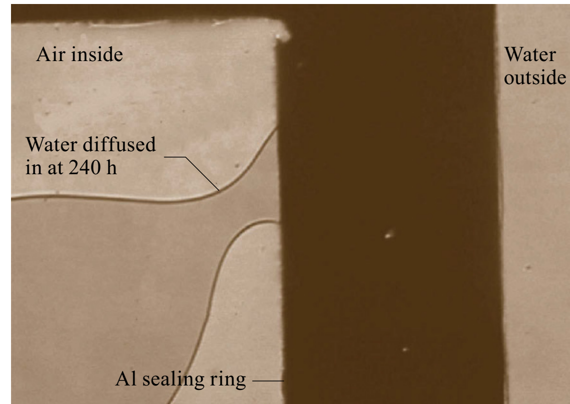

Fig. 43.34 A particular device that failed at 240 h of testing time

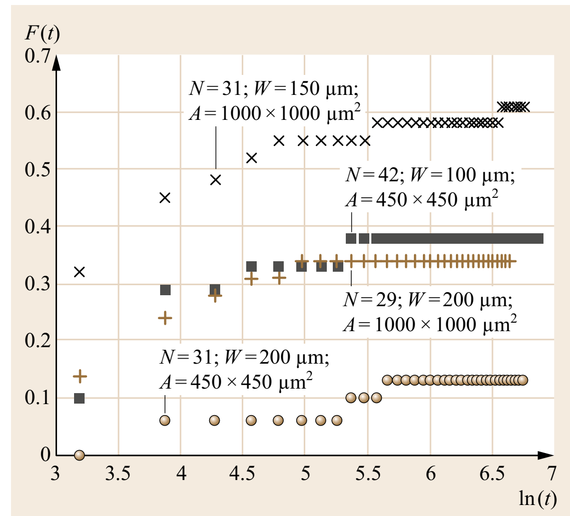

Fig. 43.35 Cumulative failure data

likelihood estimator (MLE) was then used to predict the mean, standard deviation, and mean time to failure (MTTF). Table 43.2 presents the MLE calculation results for the MTTF. The wide confidence interval results from the fact that only a small number of samples had failed by the end of the test. It was also observed that packages with larger bonding width and smaller bonding area had longer MTTF values. The lower bound of the MTTF provides the worst-case scenario; For example, only 4 out of 31 samples had failed by the end of the test in the case of ring width of 200 µm and sealing area of 450 × 450 µm^2. The MTTF predicts, in the worst-case scenario, a 90% chance that a package will fail in 0.57 years in the autoclave environment.

It is widely accepted that the acceleration factor (AF) for autoclave tests follows the Arrhenius equa-

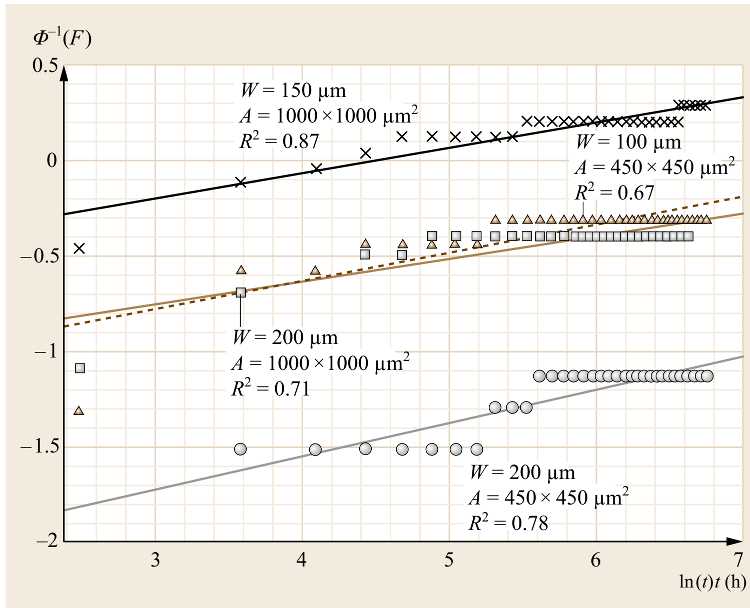

Fig. 43.36 Life data fitted by log-normal distribution. R^2 is the coefficient of determination

Table 43.2 Maximum-likelihood estimation of mean time to failure (MTTF)

MLE calculation results for MTTF[a]				
Bonding width, W (µm)	Area, A (µm^2)	MTTF		Worst case in jungle condition (years)
		UB (years)	LB (years)	
200	450 × 450	1.8×10^7	0.57	1700
100	450 × 450	5.3	0.10	300
200	1000 × 1000	6.5×10^3	0.09	270
150	1000 × 1000	0.50	0.017	50

[a] UB is the upper bound and LB is the lower bound of the 90% confidence interval, respectively. The MTTF LB times AF is the worst case MTTF used in jungle condition

tion [43.12] and can be modeled as

$$\mathrm{AF} = \frac{\left(\mathrm{RH}^{-n} \mathrm{e}^{\Delta E_\mathrm{a}/k_\mathrm{B}T}\right)_\mathrm{normal}}{\left(\mathrm{RH}^{-n} \mathrm{e}^{\Delta E_\mathrm{a}/k_\mathrm{B}T}\right)_\mathrm{accelerated}}, \qquad (43.6)$$

where RH is the relative humidity (85%, RH = 85), k_B is the Boltzmann constant, and T is the absolute temperature. The recommended value for n, an empirical constant, is 3.0 [43.146], while that for ΔE_a, the activation energy, is 0.9 eV for a plastic dip package and 0.997 eV for an anodically bonded glass-to-silicon package [43.59]. Using $\Delta E_\mathrm{a} = 0.9$ eV, an AF of about 3000 is estimated for the accelerated testing condition as compared with the jungle condition (35 °C, 1 atm, and 95% RH); the corresponding worst-case lifetime values in jungle condition are also listed in Table 43.2. The high values of estimated MTTF in jungle condition could be a result of overestimation of the AF because the plastic dip package may have lower AF compared with glass packages. Nevertheless, these data and analyses provide important guidelines in the area of accelerated testing of MEMS packages.

For vacuum-packaged MEMS devices, the lifetime can be evaluated by monitoring the quality factor of microresonators inside sealed cavities. Again, vacuum-packaged MEMS resonators obtained by aluminum-to-nitride bonding using RTP are discussed in detail here to illustrate the various factors involved in reliability. It was found that, under normal condition of room-temperature storage, the quality factor of resonators remained constant after 37 weeks, as shown in Fig. 43.37. Furthermore, the vacuum quality in harsh environment was characterized by placing a vacuum-encapsulated comb resonator into an autoclave chamber

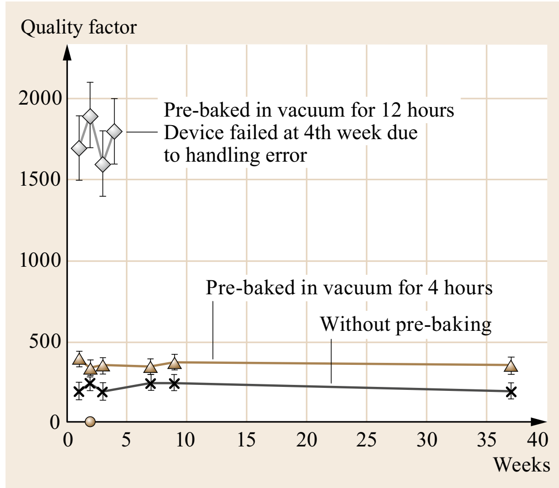

Fig. 43.37 Long-term stability tests to 37 weeks. The Q factor increased with prebaking time

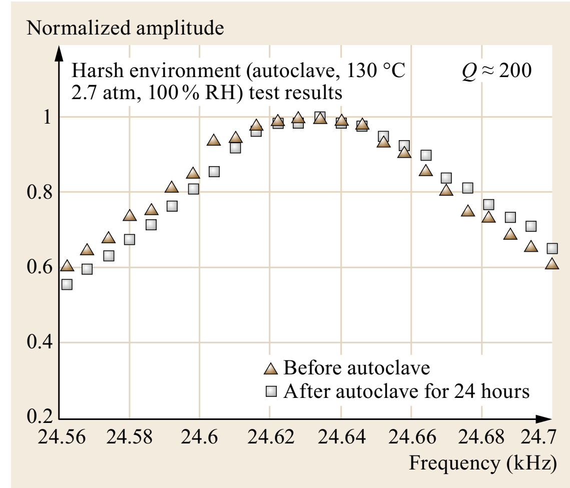

Fig. 43.38 Spectrum measured before and after accelerated testing for 24 h

(130 °C, 2.7 atm, and 100% RH) for accelerated testing. The result is shown in Fig. 43.38; the quality factor remained at 200 after 24 h in the autoclave testing chamber. Since the slight differences between the two spectra are within normal experimental errors, it can be concluded that the harsh environment in the test did not affect the vacuum seal.

To characterize the vacuum lifetime of the packages, two vacuum-packaged comb resonators were placed in the harsh environment for continuous testing for up to 1008 h; the results are summarized in Table 43.3. The quality factor of each package was measured in every 24 h interval, being found to remain at 400 and 200, respectively, before failure. The first packaged resonator with Q of 200 had aluminum sealing ring width of 75 μm and sealing area of $650 \times 650\,\mu m^2$. The second packaged micro resonator had Q value of 400 and aluminum sealing ring width of 200 μm and sealing area of $550 \times 550\,\mu m^2$. If the accelerated testing results on water penetration [43.94] are applied here for gas penetration as a measure of the vacuum

Table 43.3 Summary of accelerated testing results on two vacuum-packaged resonators

	Package 1	Package 2
Q	400	200
Time under testing (h)	> 1008	576
MTTF, lower bound (h)	769	149

sealing characteristics, the accelerated lifetime of the first and second packaged resonator would fall in the range of 0.017–0.1 years (149–876 h) and 0.09–0.57 years (769–4993 h), respectively. Experimentally, the first packaged resonator failed at 576 h into the test in the autoclave chamber. This corresponds well to the lifetime prediction from the previous work [43.94]. The second packaged resonator survived in the autoclave chamber for more than 1008 h (the device did not fail), and this result also verifies the prediction made from the previous work. However, note that these results are preliminary data, and more tests on more packaged devices should be conducted to enable meaningful statistical analyses.

43.5 Future Trends and Summary

In the past, development of MEMS packaging mainly originated from IC packaging advancement, because existing packaging techniques could significantly reduce the development cost of MEMS. However, it is expected that this situation will change very soon such that MEMS packaging approaches will assist IC packaging development. Recent progress in IC packaging has aimed to provide high I/O density and greater chip integration capability to meet needs for higher speed and higher data communication rates. To satisfy these requirements, several packaging concepts and techniques have been developed, including 3-D packaging, wafer-level packaging, BGA, and flip-chip technique. Although all of these concepts and methods can provide packages with greater I/O density, flexibility in terms of chip integration, and lower manufacturing cost for IC fabrication, they are still insufficient to provide solutions for future applications,

because of the increasing complexity and requirements of MEMS packaging. In contract, with the progress of MEMS fabrication technologies, several key processes such as deep reactive-ion etching (DRIE), wafer bonding, and thick photoresist processes [43.147] have been utilized for IC packaging fabrication. Therefore, technologies developed for MEMS fabrication can also assist development of new IC packaging approaches.

To address future needs for process integration, adaptive multichip module (MCM) [43.31] or 3-D packaging combined with vertical through-substrate interconnects [43.10, 148] are promising approaches for development of future MEMS packaging processes. Based on low-temperature flip-chip solder bonding technique, these packaging methods can provide greater flexibility in terms of device fabrication and packaging. Devices can be fabricated before they are integrated together to form microsystems, thereby dramatically reducing packaging costs. Vertical through-substrate interconnects can achieve higher I/O density as well as lower resistance, parasitic capacitance, and mutual inductance. Although this approach offers many possible advantages, technical challenges remain; For instance, metal is commonly used as the filler material inside vertical vias to form electrical interconnects, which can introduce large thermal mismatch with respect to silicon substrate and generate huge thermal stresses that cause packaging reliability problems. Moreover, filling materials into these high-aspect-ratio vias will be an interesting engineering challenge.

The future development of MEMS packaging depends on successful implementation of various unique techniques:

1. Development of mechanical, thermal, and electrical models for packaging designs and fabrication processes
2. Wafer-level, chip-scale packaging with low packaging cost and high yield
3. Effective testing techniques at wafer level to reduce testing costs
4. Device integration by vertical through interconnects as an interposer [43.1] to avoid thermal mismatch problems.

In addition to these approaches and challenges, there are many other possibilities that have not been listed but that also require dedicated investigation; For example, several key nanotechnologies have been introduced in previous chapters, but packaging solutions for such NEMS devices have not been addressed. Because it is feasible to use MEMS as a platform for NEMS fabrication, all the packaging issues discussed in this chapter apply directly to NEMS devices as well. On the other hand, nanotechnology may introduce new opportunities for MEMS/NEMS packaging applications by providing superior electrical, mechanical, and thermal properties [43.149–152]; For example, carbon nanotubes have very high thermal conductivity [43.151] and may be applicable to enhance thermal cooling effects for improved IC/MEMS/NEMS packaging applications.

In summary, this chapter has introduced MEMS packaging issues in the areas of fabrication, application, reliability, and future development. Design and modeling, material selection, process integration, and cost are main issues to be considered when developing a new MEMS packaging process.

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