

Photovoltaic Inverter Topologies for Grid Integration Applications

Tan Kheng Suan Freddy and Nasrudin Abd Rahim

Abstract For grid integration photovoltaic (PV) system, either compact high-frequency transformer or bulky low-frequency transformer is employed in the DC- or AC side of the PV inverter, respectively, to step up the low output voltage of the PV modules to the grid voltage. Galvanic isolation is provided and the safety is assured with the use of transformer. Because of the high cost and high loss of the transformer, the PV inverter becomes expensive and low efficient. To mitigate these problems, the transformer is removed from the PV inverter. The transformerless PV inverter is smaller, cheaper, and higher in efficiency. Various transformerless PV inverter topologies, with different circuit configuration and modulation techniques, have been developed recently. The operating principle and the converter structure are evaluated in this chapter. It is expected that the transformerless PV inverter would have great potential for future renewable generation and smart microgrid applications.

Keywords Photovoltaic (PV) inverters · Transformerless · Common-mode voltage (CMV) · Leakage current

1 Introduction

Photovoltaic (PV) energy has experienced remarkable growth in recent decades owing to the renewable energy policy, feed-in-tariff and cost reduction of the PV installation. According to the IEA-PVPS report, the cumulative capacity of installed

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PV reaches 177 GW by 2014, out of which the majority ($\sim 90\%$) is grid-connected system [1]. The increase demand of the PV installation, especially grid-connected PV system, indicates that there is a need for in-depth research and development.

Cost-effectiveness and efficiency are the most considered criteria for PV inverter design. Therefore, the PV inverters must be designed with high efficiency at minimum cost. Various types of PV inverters can be found in the market. For grid integration application, there are generally two types of PV inverters, i.e., with transformer and without transformer. The transformer used can be high-frequency transformer on the DC side or low-frequency transformer on the AC side of the inverter. In order to reduce the cost and to increase the efficiency, the recent technology is to remove the transformer from the PV inverter. The transformerless PV inverter becomes smaller, lighter, cheaper, and highly efficient [2–4].

Nevertheless, safety issue is the main concern of the transformerless PV inverter due to high leakage current. Without galvanic isolation, a direct path can be formed for the leakage current to flow from the PV arrays to the grid. When the PV arrays are grounded, stray capacitance is created. The fluctuating potential, also known as common-mode voltage (CMV), charges and discharges the stray capacitance which generates high leakage current. In order to assure the safety operation of the inverter, VDE 0126-1-1 [5] and IEC 60755 [6] standards recommend the use of a residual current monitor unit (RCMU) to monitor the leakage current of the transformerless PV inverter. According to the standards, the inverter must be disconnected within 0.3 s if the leakage current exceeds 300 mA. In addition to safety concern, the leakage current will degrade the performance of the PV inverter owing to the increased grid current ripples, losses, and electromagnetic interference (EMI).

In order to comply with the standards requirements, various transformerless PV inverter topologies have been introduced, with leakage current minimized by the means of galvanic isolation and CMV clamping methods. The galvanic isolation can be achieved via DC-decoupling or AC-decoupling, for isolation on the DC- or AC side of the PV inverter, respectively. Nonetheless, leakage current cannot be simply eliminated by galvanic isolation and modulation techniques, due to the presence of switches' junction capacitances and resonant circuit effects. Hence, CMV clamping method is employed in some topologies to completely eliminate the leakage current [7].

The aim of this chapter is to provide an overview of the recent PV inverter topologies. Several relevant transformerless PV inverters, with different converter structures and modulation techniques, are evaluated. The operation principle of the inverter topologies and leakage current reduction method are briefly investigated. The chapter is organized as follows: Sect. 2 provides an overview of PV configuration for grid integration. Common-mode behavior of the PV inverter is analyzed in Sect. 3. Section 4 describes the leakage current reduction method for transformerless application. The transformerless PV inverter topologies, with the circuit configuration and operating principle, are presented in Sect. 5. Finally, the chapter is concluded in Sect. 6.

2 Overview of PV Configuration for Grid Integration

Based on the state-of-the-art technology, the PV configuration can be classified into four categories: module, string, multi-string and central, as indicated in Fig. 1 [8]. Each configuration comprises a combination of series or/and paralleled PV modules, converters (DC–DC converters or/and DC–AC inverters), depending on the requirement of the system application.

2.1 Centralized Configuration

When a large number of PV modules are interfaced with a single three-phase inverter as shown in Fig. 1d, this configuration is termed as central inverter. The PV modules are connected into series (called strings) to achieve sufficiently high voltage. These PV strings are then made parallel (called arrays) to reach high power level. A blocking diode is connected in series with each PV string branch to avoid reverse current. Central inverter is widely installed in large-scale PV plant. Because of the centralized configuration (with single set of sensors, control platform, and monitoring unit), the central inverter becomes cost-effective for large-scale application. However, the simple configuration comes at a cost of high-level mismatch loss between the PV modules owing to the utilization of a common maximum power point tracking (MPPT) for the entire PV arrays. The power generation loss becomes apparent during the inverter outages. The expansion of the power plant is also difficult to be realized at centralized level.

The conventional central inverter topology is a two-level three-phase full-bridge converter, as indicated in Fig. 2. It is called two-level because it can apply only two voltage levels: the DC supply voltage and the reverse of that voltage. The two-level inverter consists of DC-link capacitors, full-bridge inverter (6 IGBTs) and filters. The central inverter is connected to medium voltage network via a transformer to step up the voltage from LV (e.g., 400 V) to MV level (e.g., 11 kV). To meet higher power requirement, the PV inverter industry, such as ABB PVS800 central inverter [9], introduces a parallel connection directly to the AC side, enabling power to be fed to the medium voltage network via a single transformer as illustrated in Fig. 3. This avoids the need of individual transformer for each central inverter, reducing the cost and space. Nevertheless, in systems where the DC side needs to be grounded, a separate transformer must be employed for galvanic isolation.

The demand of higher power central inverter (MW range) has been continuously increasing with the emerging large-scale PV plant. Although advanced semiconductors with higher nominal voltage and current capability are available, they are very relatively more expensive with high loss. On the other hand, the high-power central inverter is made possible with multilevel configuration. Because of its reduced voltage derivatives (dv/dt) and higher voltage operating capability, the

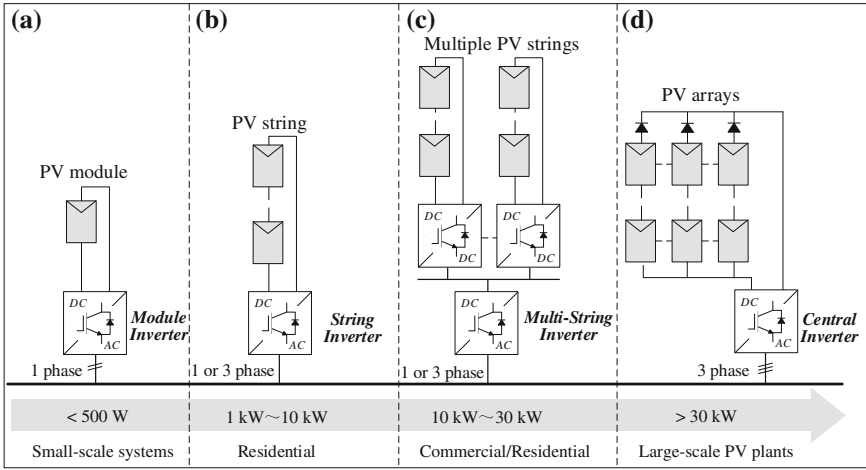


Fig. 1 Configuration of PV systems: **a** module inverter, **b** string inverter, **c** multi-string inverter, **d** central inverter [8]

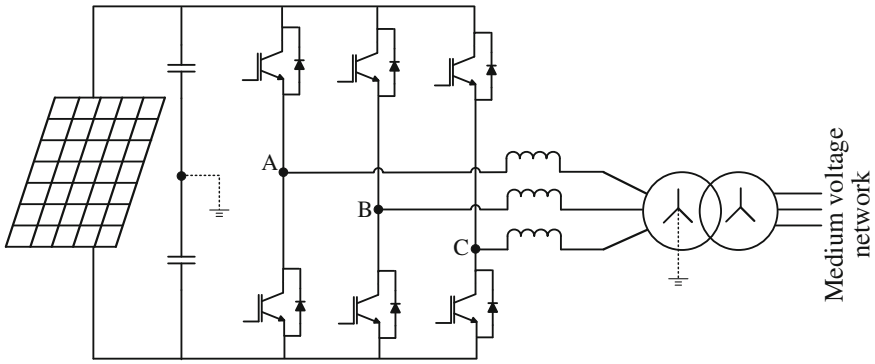
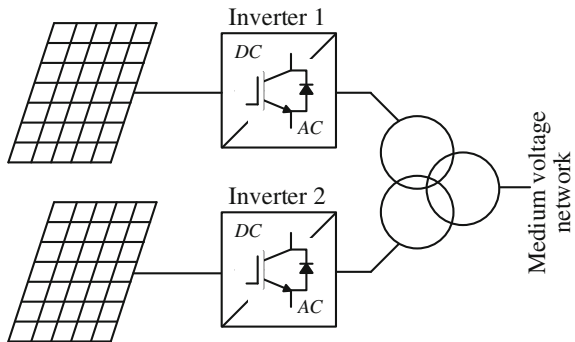


Fig. 2 Three-phase two-level centralized inverter configuration

Fig. 3 The parallel connection of two central inverter to MV network via a single transformer



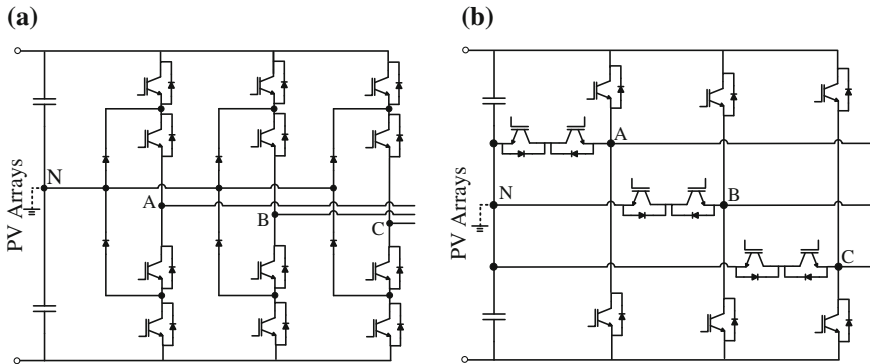


Fig. 4 Three-level central inverter: **a** NPC, **b** T-Type

multilevel converter becomes attractive for high power application. The multilevel converter generates increased level at output phase voltage, which leads to higher power quality and reduced switching loss. Nonetheless, the high power quality requires higher complexity of circuit configuration and the corresponding control, which leads to higher initial cost. The three-phase three-level neutral point clamped (3L-NPC) converter and the T-type (3L-T) converter are two widely used converter as shown in Fig. 4 [10]. The NPC and T-type converter modules have been commercialized by several manufacturers such as Semikron, Infineon and Fuji [11].

2.2 Module Configuration

Module inverter is also known as micro-inverter. In contrast to centralized configuration, each micro-inverter is attached to a single PV module, as shown in Fig. 1a. Because of the “one PV module one inverter concept,” the mismatch loss between the PV modules is completely eliminated, leading to higher energy yields. With module configuration, expansion and installation become an easy task. Micro-inverter certainly allows for a very high degree of flexibility, but it comes at an expense of higher upfront costs and greater service requirements. A large number of inverters are required for large-scale application. DC–DC converter is usually included in micro-inverter to boost the low voltage of the PV module to meet the grid requirement. High voltage amplification may shrink overall efficiency and increase price per watt. Although micro-inverters are typically used in low-power application, large-scale PV plant with micro-inverters is emerging. As shown in Fig. 5, Enphase (ENPH) installed a 2 MW solar project at Ontario, Canada’s Vine Fresh Produce, with 9000 Enphase[®] M215 micro-inverters [12].

Micro-inverters usually come with longer warranty up to 25 years, thanks to their effort to extend the lifespan of the capacitors. The first approach is to eliminate the use of electrolytic capacitors by Enecsys [13]. Enecsys 240 W micro-inverters



Fig. 5 A photo of 2.3 MW micro-inverter solar project at Ontario, Canada’s Vine Fresh Produce

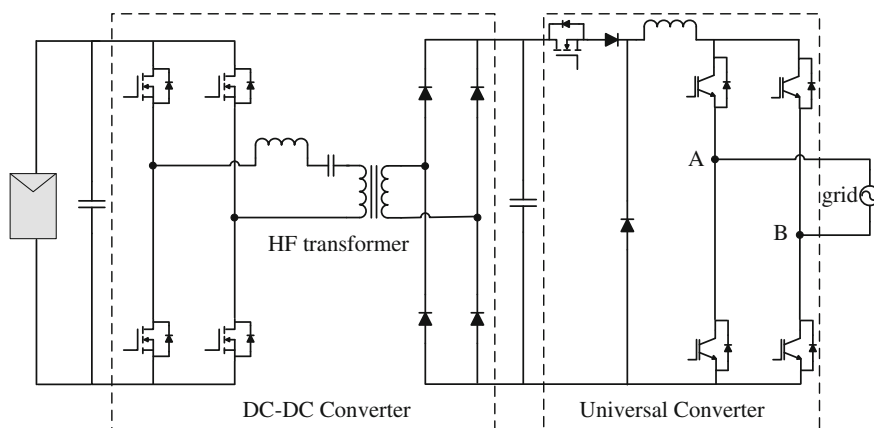


Fig. 6 Commercial Enecsys micro-inverter

are the first micro-inverters without electrolytic capacitors to achieve higher reliability. The micro-inverter configuration is shown in Fig. 6, which includes a DC–DC boost converter and a DC–AC inverter (universal converter). The DC–DC converter is made up of a resonant H-bridge, a high-frequency (HF) transformer, and a bridge rectifier. With buck, boost and buck–boost capability, the universal converter can operate with a wide range of input voltage, improving the power quality and the efficiency [10]. Without the use of electrolytic capacitors, the inverter has an operating life expectancy of greater than 25 years, matching that of solar PV modules. The second approach is the use of interleaved flyback converter. The Enphase micro-inverter configuration is shown in Fig. 7 [14]. The flyback

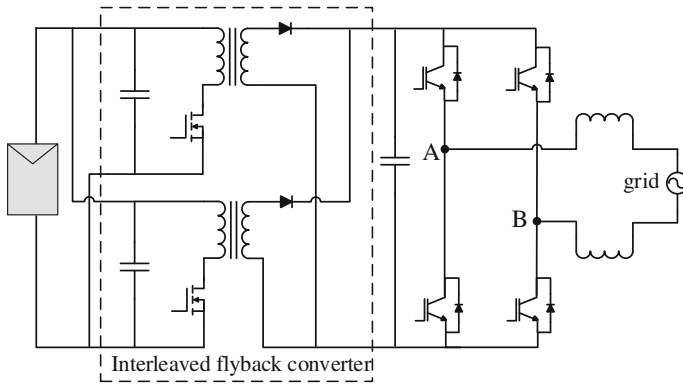


Fig. 7 Commercial Enphase micro-inverter

converter is connected in parallel, and modulated with interleaved PWM. Compared with the conventional flyback converter, interleaved topology requires smaller filter capacitors and smaller HF transformer, which offers higher power capability with greater life expectancy.

2.3 String Configuration

In string configuration, each inverter is attached to only one PV string, avoiding the use of blocking diode as shown in Fig. 1b. String inverter combines the advantages of simple structure central inverter and high-energy-yield micro-inverter. Higher energy yield is achieved with MPPT operating at string level, thereby reducing the mismatch loss between the PV modules as compared to centralized configuration. Since the configuration is made up of one PV string per inverter, the string inverter is usually designed for low power application, typically for residential rooftop application.

In the past, U.S. regulations dictated that all electrical systems must be grounded. For grounded PV system, galvanic isolation must be provided in order to avoid the leakage current. Galvanic isolation can be provided via HF transformer on the DC side or via LF transformer on the AC side as shown in Fig. 8 [15]. Besides isolation, transformer steps up the input voltage, which provides a wide range of input voltage. However, the transformer is bulky, heavy, and expensive. Even though significant size and weight reduction can be achieved with HF transformer, the use of transformer still reduces the efficiency of the entire PV system.

Since 2005, the National Electric Code update for allowing ungrounded system opens a huge market for transformerless technology. There are numerous types of string inverters available in the market, and only several will be covered here as shown in Fig. 9. The simplest transformerless string inverter is the full-bridge

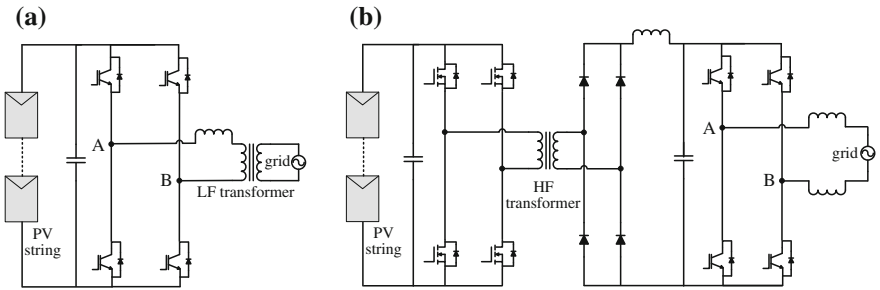


Fig. 8 String inverters with galvanic isolation: **a** with LF transformer, **b** with HF transformer

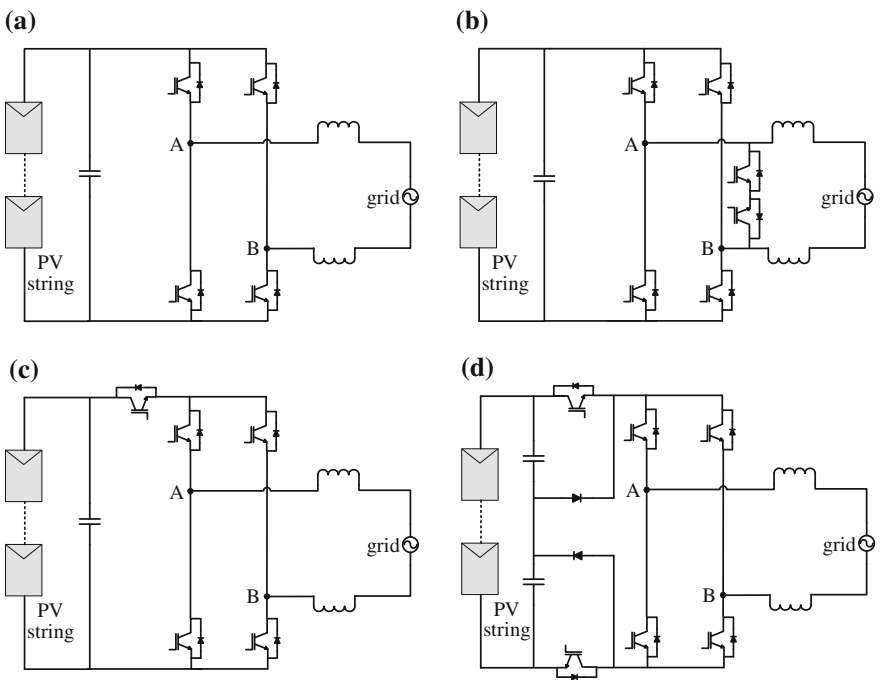


Fig. 9 Two-level string inverters: **a** full-bridge, **b** HERIC, **c** H5, **d** H6

topology as shown in Fig. 9a. The full-bridge topology is modulated by bipolar PWM in order to generate constant CMV, to eliminate the leakage current. Nonetheless, the two-level bipolar PWM doubles the voltage stress and current ripples across the filter inductors, reducing the efficiency of the PV system.

To achieve high efficiency, various inverter manufacturers have developed different circuit configuration with three-level unipolar PWM. The Sunway HERIC topology (Fig. 9b) [16] and the SMA H5 topology (Fig. 9c) [17] introduce DC decoupling and AC decoupling methods, respectively, to disconnect the PV string

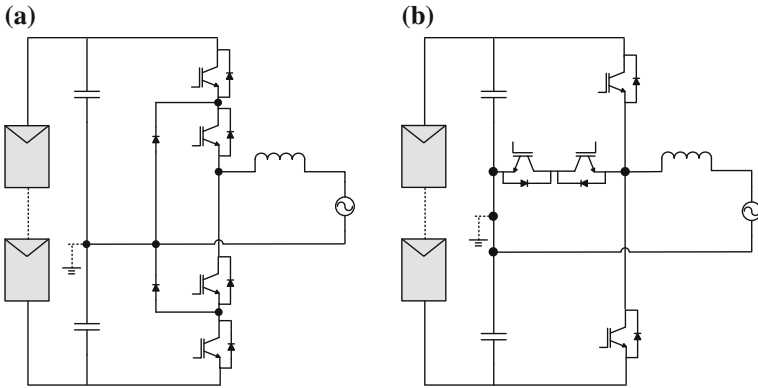


Fig. 10 Three-level string inverters: **a** NPC, **b** T-type

from the grid. The former provides lower conduction loss due to reduced semi-conductors in the conduction path. However, galvanic isolation alone cannot completely eliminate the leakage current due to the influence of switches' junction capacitances and parasitic parameters. Therefore, CMV clamping method is proposed in the H6 topology by Ingeteam [18] to completely eliminate the leakage current as shown in Fig. 9c. Two clamping diodes are added in addition to the DC decoupling switches to completely clamp the freewheeling path to half of the input voltage, $V_{DC}/2$.

The high-efficiency three-level inverter is also very suitable for transformerless application. With the neutral of the grid connected to the midpoint of the DC link capacitors as shown in Fig. 10, the high-frequency component of the CMV is eliminated in Danfoss T-type and Conergy NPC converters [19]. Without high-frequency CMV, leakage current is thoroughly eliminated. The low loss and high power quality characteristics make the three-level converter very attractive for large-scale applications. Despite the outstanding performances, the three-level configuration requires double input voltage as compared to that of the two-level inverter. As a result, DC-DC converter with high boost capability is required. Structure and control of the converter become complex with additional cost.

2.4 Multi-string Configuration

The multi-string inverter is the combination of central and string configurations as shown in Fig. 1d. Several PV strings with individual DC-DC converter (MPPT) are connected to a common inverter. It is the mainstream inverter today. While

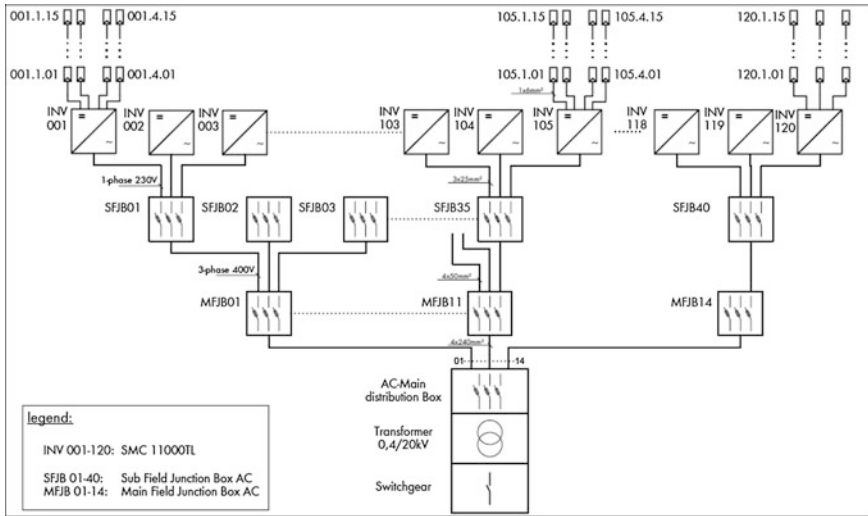


Fig. 11 Block diagram of a 1.2 MW PV plant with SMC 11000TL multi-string inverters

retaining the simple structure and cost-effective characteristic of the centralized configuration, the multi-string inverter minimizes the mismatch loss between the PV modules with each MPPT per PV string. Figure 11 shows a block diagram of 1.2 MW PV plant with single-phase transformerless multi-string SMA inverters [20]. Although multi-string configuration requires larger amount of inverters with higher investment cost, the ease of installation, commissioning, and maintenance are pushing the market toward the use of multi-string inverters in large-scale PV plants. Installing large central inverters requires advanced infrastructure for shipping and installation. Multi-string inverters come on standard palettes, simplifying and expediting shipping and other on-site logistics. With multi-string configuration, the PV plant can be easily expanded, with additional PV strings and inverters added to it without affecting the existing system structure.

Figure 12 presents the basic DC-DC converter structures for multi-string inverter. HF-based converter as indicated in Fig. 12a, provides a wide range of input voltage. It is suitable for applications in the countries where galvanic isolation is priority. This type of converter suffers from complexity of control and relative higher loss compared to boost converter shown in Fig. 12b. The boost converter is simple in structure and in control. Besides boosting the input voltage, it operates the MPPT. Multi-string inverter covers a wide range of topologies. All the discussed topologies, ranging from two-level to multilevel configurations, have the potential to be multi-string inverter. Both single- and three-phase inverters are available in the market.

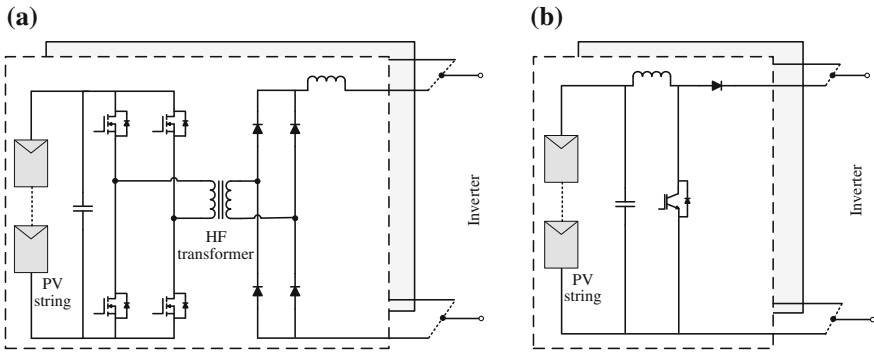


Fig. 12 DC-DC converters for multi-string inverter: **a** HF transformer-based converter, **b** boost converter

3 Common-Mode Behavior

The transformerless technology offers high-efficiency PV inverter at reduced cost. This explained why the PV inverter trend is moving toward transformerless topology. In order to understand the fundamental principle of the transformerless topology, the common-mode behavior will be analyzed here based on single-phase system. The similar common-mode behavior analysis can be extended to three-phase system, and thus the three-phase analysis will not be covered here.

When the transformer is removed from PV inverter, galvanic connection is formed between the PV arrays and the grid. This galvanic connection creates a leakage current path as shown in Fig. 12. When the CMV is produced by the inverter topology with corresponding pulse width modulation (PWM), the CMV charges and discharges the stray capacitance. As a result, leakage current is generated, flowing through the leakage current path between the PV arrays and the grid. In order to design a suitable transformerless PV inverter topology with reduced leakage current, the common-mode behavior must first be understood. A common-mode model circuit is derived here and simplified stage by stage to study the common-mode behavior of the transformerless PV inverter.

For transformerless inverter, a resonant circuit is formed as shown in Fig. 13. This resonant circuit includes the parasitic capacitance (C_{PV}), the filter inductors (L_1 and L_2), leakage current (I_L). Here, the power converter is represented by a block with four terminals to allow a general representation of various converter topologies. On the DC side, P and N are connected to the positive and negative terminal of the DC link respectively; while on the AC side, terminals A and B are connected to the single-phase grid via filter inductors [15].

From the view of point of grid, the power converter block as shown in Fig. 14 can be considered as voltage sources, generating into equivalent circuit which consists of V_{AN} and V_{BN} . Obviously, the leakage current is a function of V_{AN} , V_{BN} , grid voltage, L and C_{PV} . Since the grid is a low-frequency voltage source (50 or

Fig. 13 Resonant circuit for single-phase transformerless PV inverter

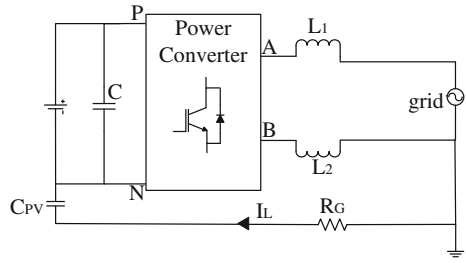


Fig. 14 Simplified resonant circuit for single-phase transformerless topology

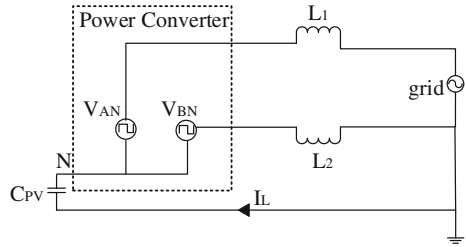
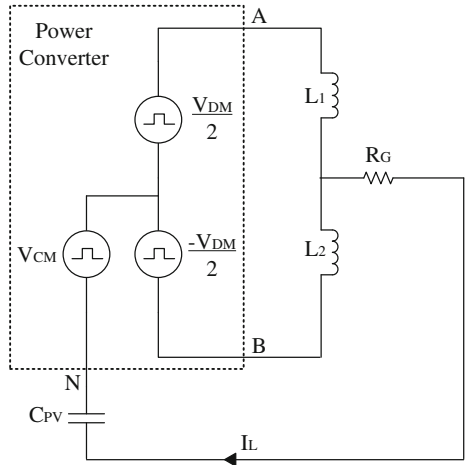


Fig. 15 Simplified resonant circuit for single-phase transformerless topology

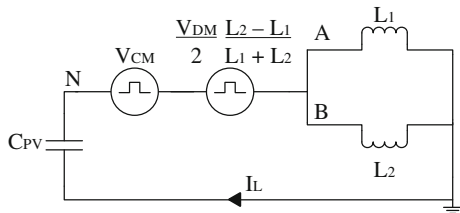


60 Hz), the impact on the common-mode model will be ignored here. Therefore, a simplified common-mode is obtained as shown in Fig. 15 by expressing voltages V_{AN} and V_{BN} as the functions of V_{CM} and V_{DM} .

The CMV (V_{CM}) and differential-mode voltage (V_{DM}) can be defined as

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

Fig. 16 The simplest resonant circuit for single-phase transformerless topology



$$V_{DM} = V_{AN} - V_{BN} \quad (2)$$

Rearranging (1) and (2), the output voltages can be expressed in terms of V_{CM} and V_{DM} as

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \quad (3)$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \quad (4)$$

Using (3) and (4) and considering only the common-mode components of the circuit, a simplified common-mode model can be obtained as in Fig. 15. The equivalent CMV (V_{ECM}) is defined as (5). Based on the derivation, the simplest common-mode model circuit can be obtained as indicated as Fig. 16.

$$V_{ECM} = V_{CM} + \frac{V_{DM} L_2 - L_1}{2 L_1 + L_2} \quad (5)$$

In order to avoid the influence of V_{DM} , two identical ($L_1 = L_2$) must be used. This also explains why the two filter inductors, i.e., one in line and the other in neutral, are always used in transformerless PV inverter instead of one inductor. Assuming identical inductors ($L_1 = L_2$) are used, the V_{ECM} is equal to V_{CM}

$$V_{ECM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (6)$$

According to the common-mode model analysis, it can be concluded that the leakage current is very much dependent of the CMV. If the CMV is varying at high frequency, the C_{PV} will be charged and discharged which leads to high leakage current flowing in the current path. On the other hand, the leakage current will be eliminated when the CMV is kept constant. Therefore, the converter structure and the modulation technique must be designed to generate constant CMV in order to eliminate the leakage current.

4 Leakage Current Reduction Methods

4.1 Galvanic Isolation

In transformerless PV inverter, the galvanic connection between the PV arrays and the grid allows leakage current to flow. The galvanic isolation can basically be categorized into DC decoupling and AC decoupling methods. For DC decoupling method, DC bypass switches are added on the DC side of the inverter to disconnect the PV arrays from the grid during the freewheeling period. However, the DC bypass branch, which consists of switches or diodes, is included in the conduction path as shown in Fig. 16. The output current flows through two switches and the two DC bypass branches during the conduction period. Hence, the conduction losses increase due to the increased number of semiconductors in the conduction path.

On the other hand, bypass branch can also be provided on the AC side of the inverter (i.e., AC decoupling method). This AC bypass branch functions as a freewheeling path which is completely isolated from the conduction path, as shown in Fig. 17. As a result, the output current flows through only two switches during the conduction period. In other words, topologies employing AC decoupling techniques are found to be higher in efficiency as compared to DC decoupling topologies.

One setback of galvanic isolation is that there is no way of controlling the CMV by PWM during the freewheeling period. Figures 18 and 19 show the operation modes of galvanic isolation topology which employs DC decoupling method (one DC bypass branch) during the positive half-cycle. As indicated in Fig. 18, during the conduction period, S_1 and S_4 conduct to generate the desired output voltage. At the same time, V_A is directly connected to V_{DC} and V_B is connected to the negative terminal (N) of the DC link. Hence, the CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \quad (7)$$

Fig. 17 Galvanic isolation topology via DC- or AC decoupling method

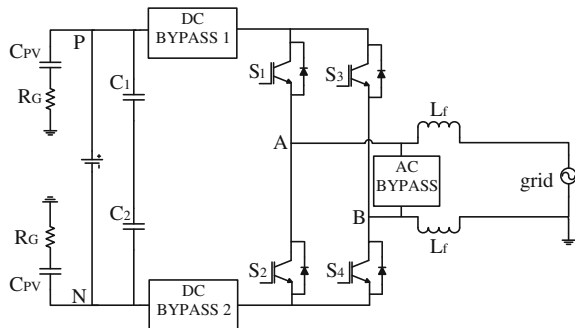


Fig. 18 Operation of DC decoupling topology in conduction mode

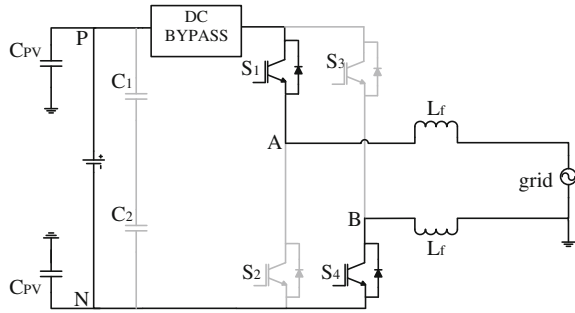
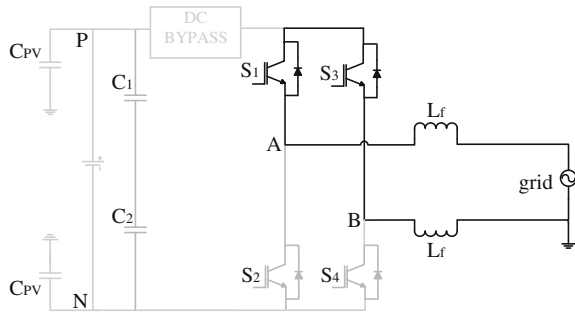


Fig. 19 Operation of DC-decoupling topology in freewheeling mode



Nevertheless, during the freewheeling period, the DC bypass switch disconnects the DC link from the grid. Point A and point B are isolated from the DC link, and V_A and V_B are floating with respect to the DC link as shown in Fig. 19. The CMV during this period of time is not determined by the switching state, but instead, is oscillating with amplitude depending on the parasitic parameters and the switches' junction capacitances of the corresponding topology. As a result, leakage current can still flow during freewheeling period. The same is the case for converters using AC decoupling method. The analysis shows that the leakage current cannot be completely eliminated with the galvanic isolation topology alone.

4.2 CMV Clamping

With galvanic isolation method alone, the leakage current is not completely eliminated as explained in the previous section. The CMV in these topologies cannot be manipulated via PWM due to the parasitic parameters of the resonant circuit. In order to generate constant CMV, clamping branch is introduced [15], as shown in Fig. 20. Generally, the clamping branch consists of diodes or switches and a capacitor divider which ensures the freewheeling path is clamped to the half of the input voltage ($V_{DC}/2$). With the combined effect of galvanic isolation and CMV clamping, leakage current is completely eliminated.

Fig. 20 CMV clamping topology

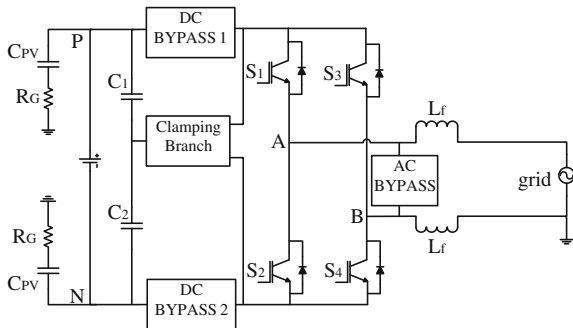


Fig. 21 Operation of DC decoupling topology with CMV clamping branch in conduction mode

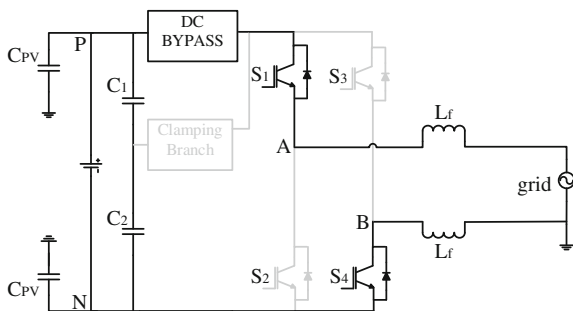


Figure 21 illustrates the conduction mode of CMV clamping topology which employs DC decoupling method during the positive half-cycle. S_1 and S_4 conduct to generate the desired output voltage. At the same time, V_A is directly connected to V_{DC} and V_B is connected to the negative terminal (N) of the dc-link. Thus, the CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \quad (8)$$

In the freewheeling mode, the DC bypass switch disconnects the DC link from the grid. At this moment, the clamping branch operates, as shown in Fig. 22, so that point A and point B are clamped to $V_{DC}/2$. The CMV reads

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2} \left(\frac{V_{DC}}{2} + \frac{V_{DC}}{2} \right) = \frac{V_{DC}}{2} \quad (9)$$

The CMV clamping branch ensures the complete clamping of the freewheeling path to constant. As a result, the leakage current is completely eliminated. It is worth noting that the CMV branch is employed with DC- or AC decoupling branch for leakage current reduction. The latter provides lower losses due to the reduced switch count in conduction path as explained earlier.

5 Transformerless PV Inverter Topologies

5.1 Full-Bridge Topology

Full-bridge topology is widely used for various applications due to the simplicity of design and low cost. The full-bridge structure consists of four switches, S_1 – S_4 , as shown in Fig. 23. Conventionally, the full-bridge topology is modulated by bipolar modulation for transformerless application.

Each pair of the diagonal switches, i.e., S_1, S_4 and S_2, S_3 , is operated simultaneously at switching frequency during the positive and negative half-cycle respectively. Current flows through the corresponding pair of diagonal switches to generate the desired output voltage. Bipolar modulation is also known as two-level modulation. As shown in Fig. 24, it generates two-level output voltage, i.e., $+V_{DC}$ and $-V_{DC}$. In every switching transition, the voltage changes across the inductor by twice of input voltage, $2V_{DC}$. This doubles the voltage stress, current ripple and loss across the filter inductors. Thus, the overall efficiency is reduced. Larger filter inductors are required to compensate the high PWM ripple which leads to higher cost.

With bipolar modulation technique, the CMV is constant as illustrated in Fig. 25. The leakage current is completely eliminated. The results show that bipolar modulation is suitable for transformerless PV inverter applications at the expense of reduced system efficiency.

Fig. 22 Operation of DC decoupling topology with CMV clamping branch in freewheeling mode

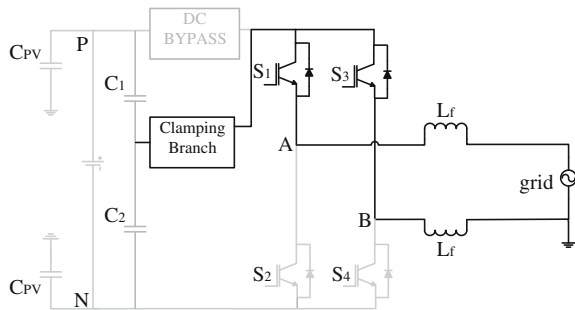
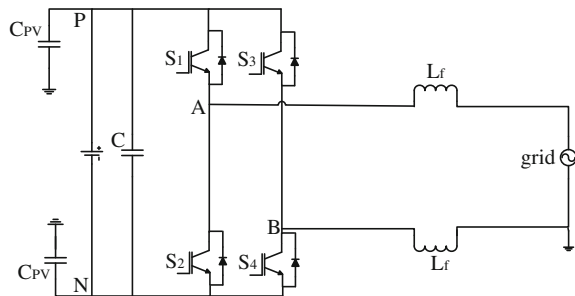


Fig. 23 Full-bridge topology



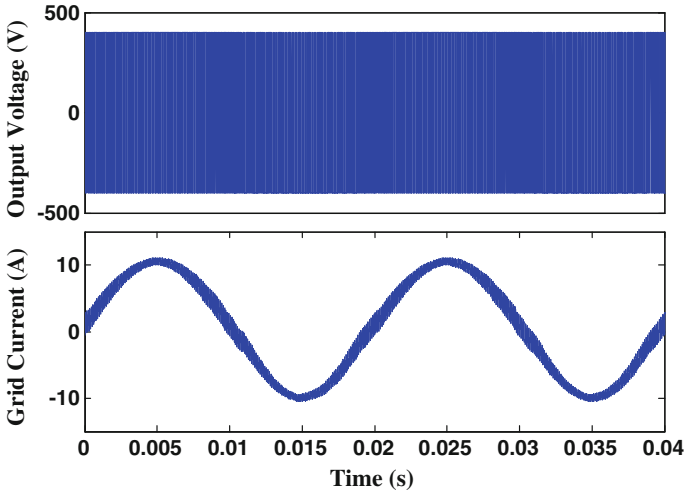


Fig. 24 Output voltage (*top*) and grid current (*bottom*) for bipolar modulation

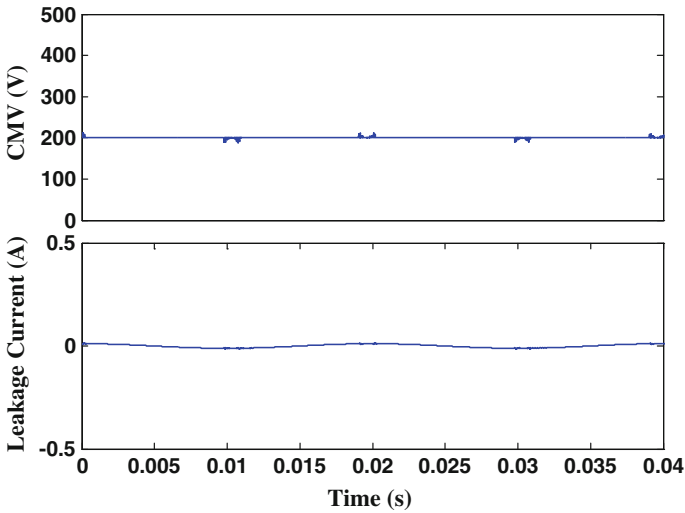


Fig. 25 CMV (*top*) and leakage current (*bottom*) for bipolar modulation

5.2 H5 Topology

H5 inverter [17] is patented by SMA. Given that a total of five switches are utilized, this topology is referred to as H5 inverter. A DC bypass switch, S_5 , is added in the input DC side of the conventional full-bridge inverter structure as shown in Fig. 26.

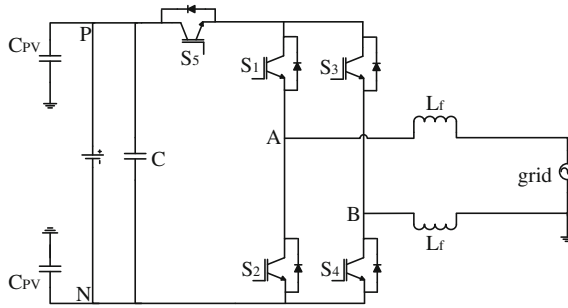


Fig. 26 H5 topology

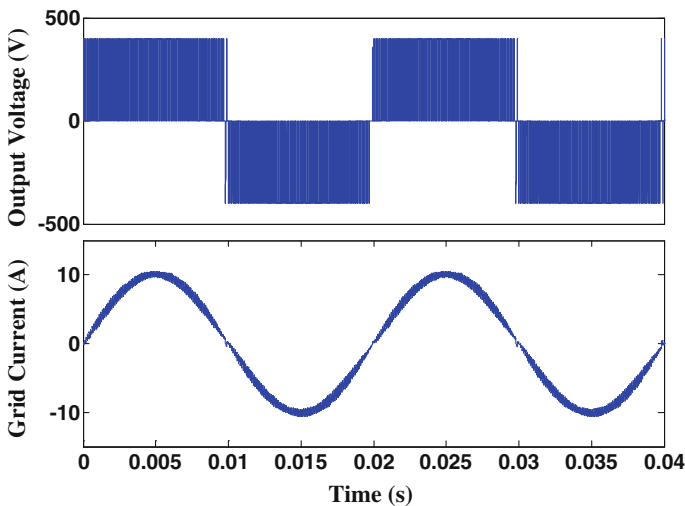


Fig. 27 Output voltage (*top*) and grid current (*bottom*) for H5 topology

The introduction of the Dc bypass switch is to provide galvanic isolation to disconnect the leakage current path during the freewheeling period.

The upper pair of switches S_1 and S_3 is operated at grid frequency while the lower pair of switches S_2 and S_4 is operated at switching frequency. During the conduction period of positive half-cycle, S_1 , S_4 and S_5 are ON to generate the desired output voltage. As compared to bipolar modulation, the grid current ripples are smaller due to unipolar output voltage as presented in Fig. 27. Current flows through S_5 , S_1 , grid, and S_4 . During the freewheeling period of positive half-cycle, S_4 and S_5 are OFF, disconnecting the PV from the grid. Current freewheels through S_1 and the anti-parallel diode of S_3 .

On the other hand, S_2 , S_3 , and S_5 are ON to generate the desired output voltage during the conduction period of negative half-cycle. Current flows through S_5 , S_3 , grid, and S_2 . During the freewheeling period of negative half-cycle, S_2 and S_5 are

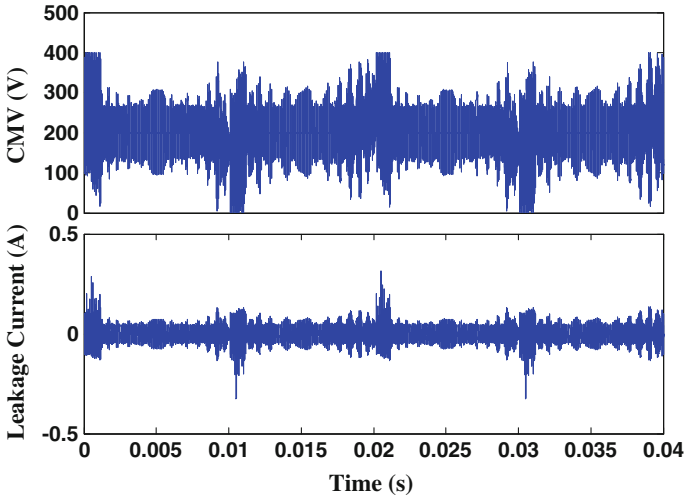


Fig. 28 CMV (*top*) and leakage current (*bottom*) for H5 topology

OFF, disconnecting the PV from the grid. Current freewheels through S_3 and the anti-parallel diode of S_1 .

With the galvanic isolation of H5 inverter, leakage current path is disconnected. Nonetheless, the CMV is not constant. Large oscillation with magnitude up to 400 V is observed in Fig. 28. As explained in Sect. 4.1, V_A and V_B are isolated from the dc-link during the freewheeling period when S_5 is OFF. V_A and V_B are floating with respect to the dc-link during the freewheeling period. The CMV is oscillating with amplitude depending on the parasitic parameters. The leakage current can still flow due to the charging and discharging of the stray capacitances by the CMV.

5.3 HERIC Topology

The patented Highly Efficient and Reliable Inverter Concept (HERIC) inverter by Sunway, [16] is well known with its high-efficiency performance. A freewheeling path (S_5 and S_6) is added to the output AC side of conventional full-bridge inverter structure as shown in Fig. 29. Despite the low-loss AC-decoupling topology, the freewheeling switches are operated only at grid frequency. This reduces the switching loss significantly.

Each pair of the diagonal switches, i.e., S_1, S_4 and S_2, S_3 , is operated simultaneously at switching frequency during the positive and negative half-cycle respectively. Current flows through the corresponding pair of diagonal switches to generate the unipolar output voltage and sinusoidal grid current as shown in Fig. 30. On the other hand, the freewheeling switches, S_5 and S_6 , are ON

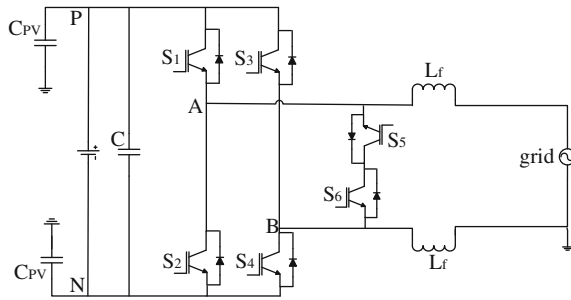


Fig. 29 HERIC topology

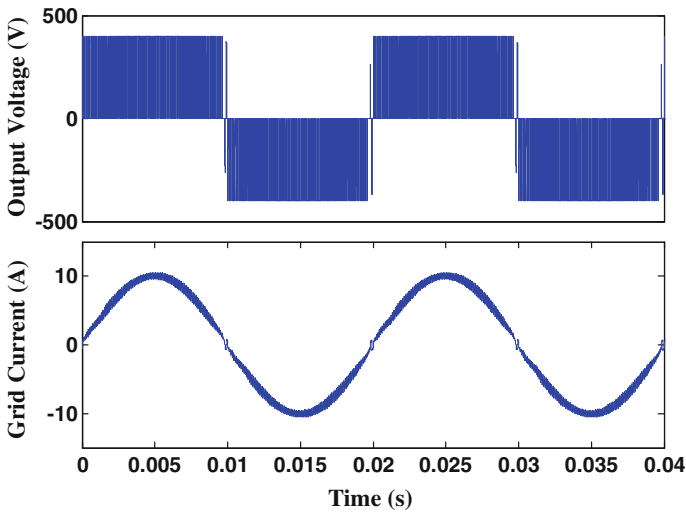


Fig. 30 Output voltage (*top*) and grid current (*bottom*) for HERIC topology

throughout the negative and positive half-cycle respectively. During the free-wheeling period of positive half-cycle, current freewheels through S_5 , the anti-parallel diode of S_6 and the grid; and through S_6 , the anti-parallel diode of S_5 and the grid during the freewheeling period of negative half-cycle.

Galvanic isolation is provided via the freewheeling path. Similar to H5 topology, the CMV is not constant and large oscillation is observed in Fig. 31. The CMV is oscillating with amplitude depending on the parasitic parameters of the resonant circuit. As illustrated in Fig. 31, the leakage current is generated owing to the charging and discharging of the stray capacitances by the CMV.

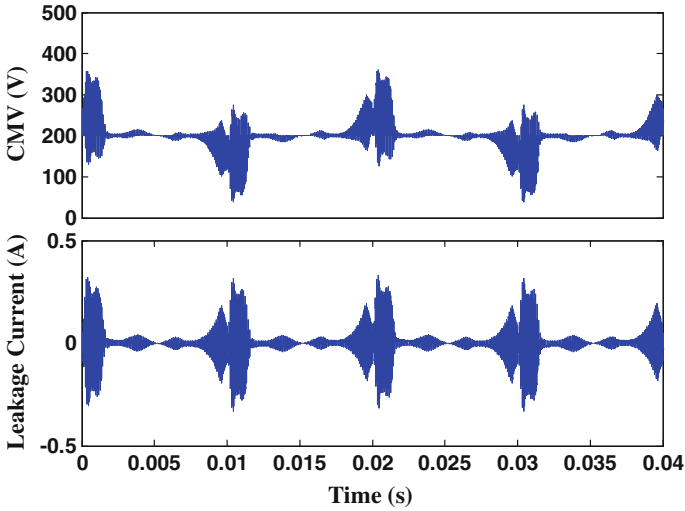
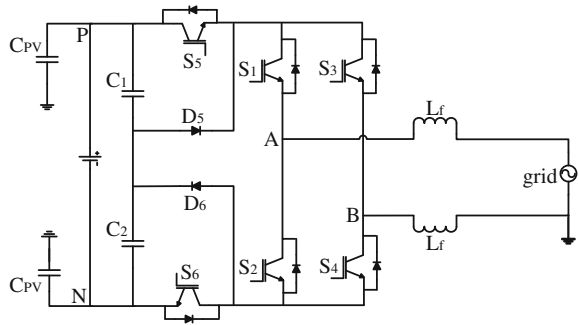


Fig. 31 CMV (*top*) and leakage current (*bottom*) for HERIC topology

Fig. 32 H6 topology



5.4 H6 Topology

H5 and HERIC focus only on providing galvanic isolation while neglecting the effect of the CMV. As a matter of fact, the CMV of these topologies is still floating due to the influence of switches’ junction capacitances and parasitic parameters. This issue is mitigated by the clamping branch of H6 topology [18]. Two DC bypass switches, S_5 and S_6 and two clamping diodes, D_5 and D_6 , are added to the conventional full-bridge inverter as presented in Fig. 32.

Throughout the positive half-cycle, S_1 and S_4 are ON. S_5 and S_6 commute simultaneously at switching frequency while S_2 and S_3 commute together but complementarily to S_5 and S_6 . Current flows through S_5 , S_1 , S_4 , and S_6 to generate

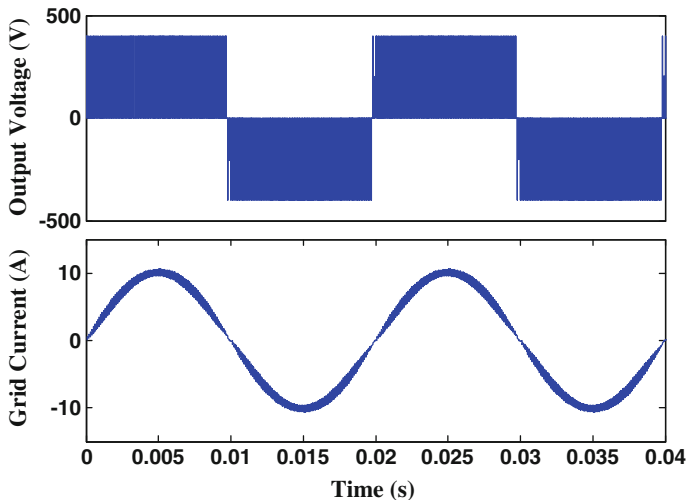


Fig. 33 Output voltage (*top*) and grid current (*bottom*) for H6 topology

the desired output voltage as shown in Fig. 33. Similarly, S_2 and S_3 are ON throughout the negative half-cycle. S_5 and S_6 commute simultaneously at switching frequency while S_1 and S_4 commute together but complementarily to S_5 and S_6 . During the freewheeling period of negative half-cycle, S_5 and S_6 are OFF and S_1 and S_4 are ON.

During the freewheeling period of positive half-cycle, S_5 and S_6 are OFF and S_2 and S_3 are ON. Therefore, freewheeling current finds its path in two ways, i.e., S_1 and the anti-parallel diode of S_3 ; S_4 and the anti-parallel diode of S_2 . At this moment, the clamping diodes clamp the freewheeling path completely to constant, $V_{DC}/2$. Freewheeling current finds its path in two ways, i.e., S_3 and the anti-parallel diode of S_1 , and S_2 and the anti-parallel diode of S_4 . The PV is disconnected from grid by the use dc-bypass switches, S_5 and S_6 . At this moment, the clamping diodes (D_5 and D_6) clamp the freewheeling path completely to constant at $V_{DC}/2$.

With implementation of the clamping diodes, the CMV is clamped to the constant, and thus the leakage current is eliminated as indicated in Fig. 34. Nevertheless, H6 topology suffers from high conduction losses as the bypass switches have been added into the conduction path.

5.5 oH5 Topology

Similar to H6, oH5 topology [21] is designed with CMV clamping branch. A DC bypass switch S_5 and a clamping switch S_6 are added into the conventional

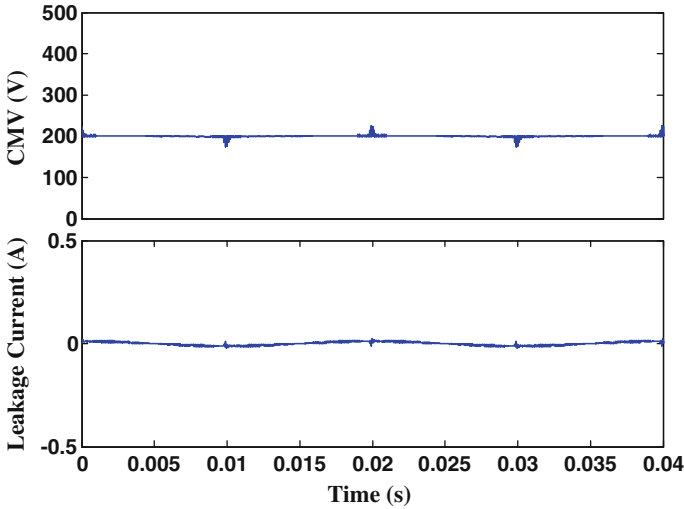
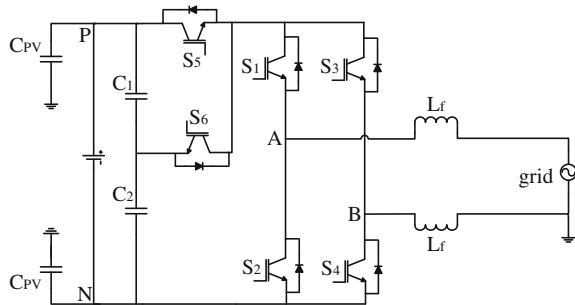


Fig. 34 CMV (*top*) and leakage current (*bottom*) for H6 topology

Fig. 35 oH5 topology



full-bridge inverter structure as shown in Fig. 35. The voltage divider is made up of two capacitors.

Throughout the positive half-cycle, S_1 is ON. S_4 and S_5 commutate simultaneously at switching frequency but complementarily to S_3 and S_6 . During the conduction period of positive half-cycle, current flows through S_1 , S_4 and S_5 to generate the desired output voltage as shown in Fig. 36. On the other hand, S_3 is ON throughout the negative half-cycle. S_2 and S_5 commutate simultaneously at switching frequency but complementarily to S_1 and S_6 . During the conduction period of negative half-cycle, current flows through S_2 , S_3 and S_5 to generate the desired output voltage.

The current freewheels through S_1 and anti-parallel diode of S_3 during the freewheeling period of positive half-cycle. At this moment, the clamping switch, S_6 , is ON to clamp the freewheeling path completely to constant at $V_{DC}/2$. The current freewheels through S_3 and anti-parallel diode of S_1 during the freewheeling period.

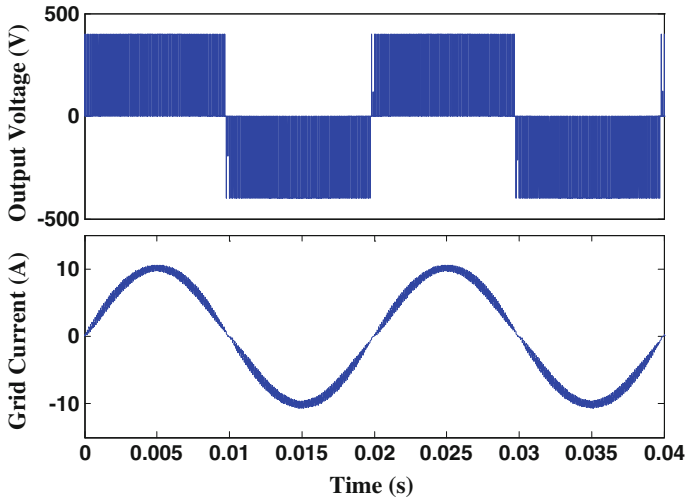


Fig. 36 Output voltage (*top*) and grid current (*bottom*) for oH5 topology

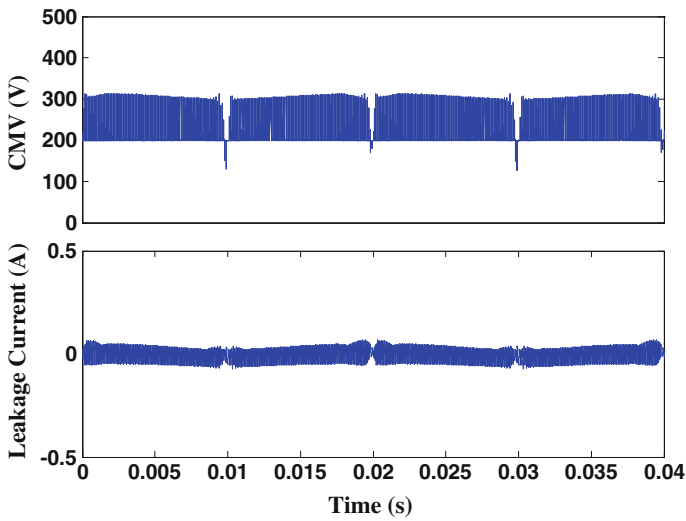


Fig. 37 CMV (*top*) and leakage current (*bottom*) for oH5 topology

Similarly, the freewheeling path is not floating but is being clamped to constant at $V_{DC}/2$ via S_6 .

With the clamping switch, the CMV is clamped completely to the constant and the leakage current is eliminated. Despite constant CMV, spikes are still observed as shown in Fig. 37. The occurrence of these spikes is the result of dead time

between S_5 and S_6 . Similar to H6 topology, oH5 topology suffers from high conduction losses as the bypass switches have been added into the conduction path.

5.6 HBZVR-D Topology

HBZVR-D inverter [15] is designed with an ac bidirectional freewheeling path and a CMV clamping branch as shown in Fig. 38. The bidirectional freewheeling path consists of a switch, S_5 , and a full-bridge rectifier (D_1 – D_4). Diodes D_5 and D_6 form the clamping branch of the freewheeling path. The voltage divider is made up of two capacitors.

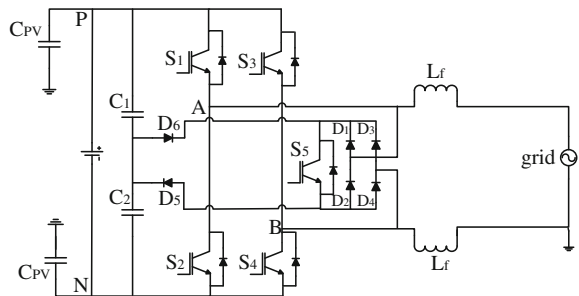
Each pair of the diagonal switches, i.e., S_1, S_4 and S_2, S_3 , is operated simultaneously at switching frequency during the positive and negative half-cycle respectively. Current flows through the corresponding pair of diagonal switches to generate the desired unipolar voltage as shown in Fig. 39. On the other hand, S_5 , is ON during the freewheeling period. Current freewheels through D_2 and D_3 , and, D_1 and D_4 during the positive and negative half-cycle respectively. At the same time, D_5 or D_6 conducts and clamps the CMV to constant, $V_{DC}/2$, as presented in Fig. 40. The leakage current is completely eliminated.

The clamping branch of HBZVR-D ensures the complete clamping of CMV to $V_{DC}/2$ during the freewheeling period. It is well noted that the output current flows through only two switches in every conduction period. This explains why HBZVR-D has relatively higher efficiency than those of DC decoupling topologies. HBZVR-D combines the advantages of the low-loss AC decoupling method and the complete leakage current elimination of the CMV clamping method.

6 Loss Analysis

Figure 41 presents the loss distribution for various topologies. Conventional bipolar modulation yields the highest total loss due to its two-level modulation technique. H5 and oH5 add one DC bypass switch, whereas H6 adds two DC bypass switches

Fig. 38 HBZVR-D topology



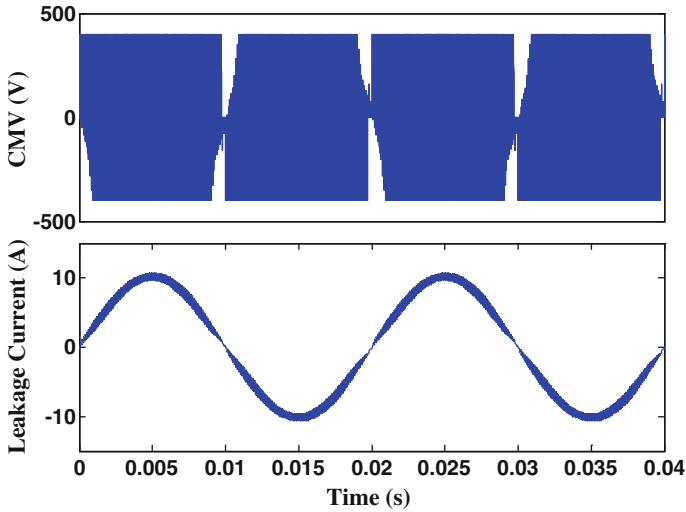


Fig. 39 Output voltage (*top*) and grid current (*bottom*) for HBZVR-D topology

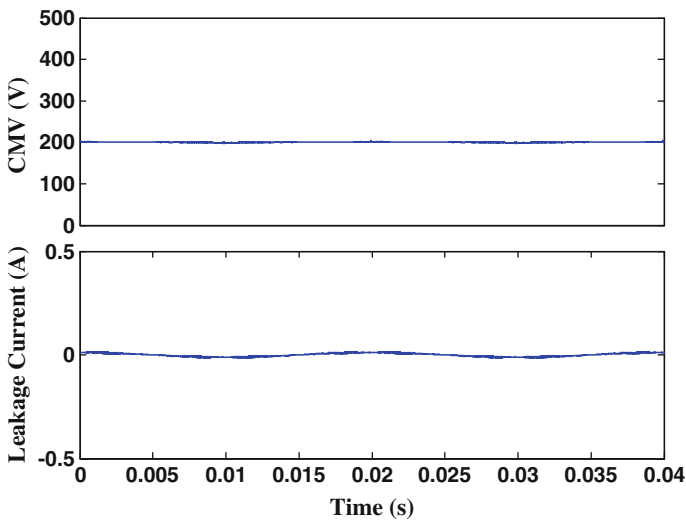


Fig. 40 CMV (*top*) and leakage current (*bottom*) for HBZVR-D topology

and diodes into the conduction path. This explains why all the DC decoupling topologies (H5, oH5, and H6) have higher (conduction) loss as compared to the AC-decoupling topologies (HERIC, and HBZVR-D). H6 topology yields the highest device losses due to excessive components that are added into the conduction path. As expected, HERIC topology has the lowest device losses.

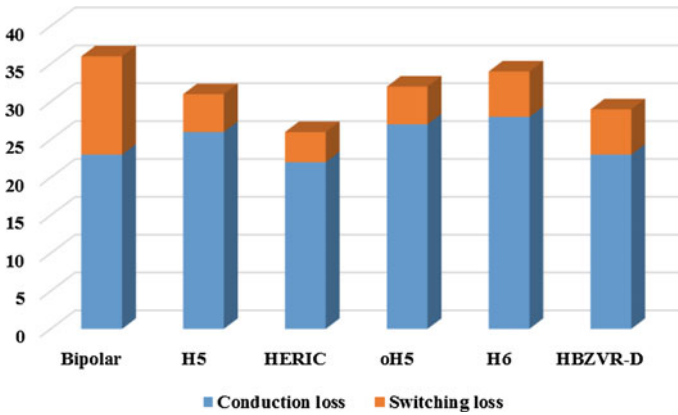


Fig. 41 Loss distribution of various topologies at 1 kW

HBZVR-D has slightly higher losses than HERIC but they are still much lower than those of the DC decoupling family. Obviously, the conduction losses are the main contributor as shown in Fig. 41. The results show that ac-decoupling family outperforms DC-decoupling family in terms of loss.

7 Summary

This chapter provides a comprehensive overview of the PV inverter topologies for grid integration applications. The state-of-the-art PV configurations with several commercial PV inverter topologies are presented. The common-mode behavior are discussed in detail to provide the principle operation of the transformerless PV inverter technologies. The performance of the transformerless PV inverters is investigated.

Today, the PV market is driven by the cost and the efficiency. To meet these requirements, the researchers and manufacturers are continuously looking for new power converters and new semiconductor technology. The high-power-quality and high-efficiency multilevel converter has gained attention from the industries. For semiconductor technology, the wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN) outperforms the conventional silicon (Si) material. The SiC MOSFET can operate at high frequency at very low loss, which is very suitable for high-efficiency applications. Although the production cost of the wide bandgap materials are still high, it is expected these materials with the multilevel converters will be widely used in the future.

References

1. International Energy Agency Photovoltaic Power System Program (2014) Trends 2014 in photovoltaic applications: survey report of selected IEA countries between 1992 and 2013, report
2. Suan FTK, Rahim NA, Hew WP (2011) Modeling, analysis and control of various types of transformerless grid connected PV inverters. In: Proceedings of 2011 IEEE first international conference on clean energy and technology (CET), 27–29 June 2011, Kuala Lumpur, Malaysia, pp 51–56
3. Suan FTK, Rahim NA, Hew WP (2013) Three-phase transformerless grid-connected photovoltaic inverter to reduce leakage currents. In: Proceedings of 2013 IEEE international conference on clean energy and technology (CEAT), 18–20 Nov 2013, Langkawi, Malaysia, pp 277–280
4. Islam MR, Guo YG, Zhu JG (2014) Multilevel converters for step-up transformer-less direct grid integration of renewable generation units with medium voltage smart microgrids. In: Large scale renewable power generation: advances in technologies for generation, transmission and storage. Springer, Berlin, pp 127–149
5. VDE, Automatic Disconnection Device between a Generator and the Public Low-Voltage Grid (2005) DIN Electrotechnical Standard DIN VDE 0126-1-1, Standard
6. International Electrotechnical Commission (2011) Safety of power converters for use in photovoltaic power systems—Part 2: particular requirements for inverters, IEC 62109-2 Ed. 1, Standard
7. Freddy TKS, Rahim NA, Hew WP, Che HS (2015) Modulation techniques to reduce leakage current in three-phase transformerless H7 photovoltaic inverter. IEEE Trans Ind Electron 62 (1):322–331
8. Yang YH (2013) Advanced control strategies to enable a more wide-scale adoption of single-phase photovoltaic systems. Dissertation, Aalborg University
9. ASEA Brown Boveri (ABB) Solar photovoltaic central inverter (online). Available at: <http://www.abb.com>. Accessed on 1 Nov 2015
10. Islam MR, Guo YG, Zhu JG (2014) Power converters for small- to large-scale photovoltaic power plants. In: Power converters for medium voltage networks. Springer, Berlin, pp 17–49
11. Samir K, Bin W, Haitham AR, Frede B (2014) Photovoltaic energy conversion systems. In: Power electronics for renewable energy systems, transportation and industrial applications. Wiley, Chichester, pp 160–198
12. Bennett (2013) Enphase system deployed in 2.3 MW agricultural installation in Canada. Enphase Energy, Inc. <http://newsroom.enphase.com/releasedetail.cfm?releaseid=784444>. Accessed 1 Nov 2005
13. Garrity P (2013) Solar photovoltaic power conditioning units. US Patent 8391031 B2
14. Fornage M (2010) Method and apparatus for converting direct current to alternating current. US Patent 7796412 B2
15. Freddy TKS, Rahim NA, Hew WP, Che HS (2014) Comparison and analysis of single-phase transformerless grid-connected PV inverters. IEEE Trans Power Electron 29(10):5358–5369
16. Schmidt H, Siedle C, Ketterer J (2005) DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current. US Patent 2005/0174817 A1
17. Victor M, Greizer F, Bremicker S, Hubier U (2005) Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage. US Patent 2005/0286281 A1
18. Senosiain RG, Calahorra JC, Palomo LM, Taberna JL, Gorpide PS (2009) Single-phase inverter circuit to condition and transform direct current electric power into alternating current electric power. US Patent 2009/0316458 A1
19. Teodorescu R, Liserre M, Rodriguez P (2011) Photovoltaic inverter structures. In: Grid converters for photovoltaic and wind power systems. Wiley, Chichester, pp 5–29

20. SMA (2009) Decentralized inverter technology in large-scale PV plants, technical information, BL-DezWT-UEN103511
21. Xiao H, Xie S, Chen Y, Huang R (2011) An optimized transformerless photovoltaic grid-connected inverter. *IEEE Trans Ind Electron* 58(5):1887–1895