10 Gbps Current Mode Logic I/O Buffer

Akhil Rathore[1] and Chetan D. Parikh[2]

[1] Dhirubhai Ambani Institue of Information and Communication Technology, Gandhinagar, India
[2] Institute of ICT, Ahmedabad University, Ahmedabad, India
chetan.parikh@ahduni.edu.in

Abstract. A new architecture for a high speed CML buffer is presented. The buffer is designed for OC-192/STM-64 applications to be used in the limiting amplifier which is a critical block in optical communication systems. OC-192/STM-64 works around 10Gbps. The proposed architecture is also more efficient in terms of area.

1 Introduction

In high speed serial links and optical communication, buffers create a bottleneck. In such systems, Current- mode logic (CML) buffers [1] are commonly used. Using current as the signaling variable rather than voltage, allows for low voltage swings between the high and low digital levels. Systematic design procedures for CML buffers have been reported by Heydari and Mohanvelu [1] and by Green and Singh [3]. In conventional CML buffers inductive peaking [1] is used to enhance bandwidth but it requires monolithic inductors, which needs a large silicon area. Current architectures of output buffers use f_T doublers and inductive peaking together and can obtain data rates of up to 10 Gbps, but these also require a large silicon area [3]. The conventional CML buffer suffers from the Miller effect which degrades high frequency operation.

This paper presents a new architecture which avoids miller effect and works around 10 Gbps in a 0.18 μ m CMOS technology. It requires less chip area and power than existing architectures. The contents of the paper are as follows: Section 2 describes the conventional CML buffer, its operation and its limitations at high frequencies. Sections 3 and 4 describe the proposed architecture, its working and the various design issues. In section 5 simulation results are shown and section 6 concludes this paper.

2 CML Buffer

This section describes the basics of a conventional CML buffer, its advantages, and its limitations at high frequencies. The various design issues related to a CML buffer are discussed in [1, 3, 4].

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2.1 Overview

Figure 1 shows the basic CML buffer. It consists of a differential pair with two NMOS transistors, which act as switches. When the differential input ($V_{IN+} - V_{IN-}$) varies from 0 to V_{DD}, the output in each branch varies from V_{DD} to ($V_{DD} - I_{SS}R_D/2$), or vice versa. Thus, the differential output voltage swing achieved is $I_{ss}R_D$. Low switching noise, higher common mode rejection due to differential architecture & low swing signaling make CML an attractive choice for high frequency applications.

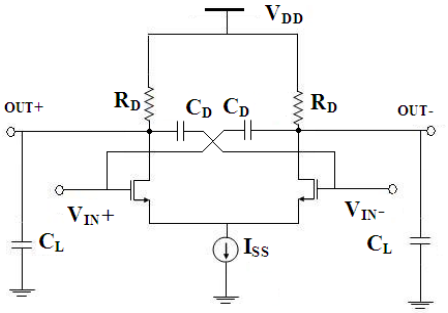

Fig. 1. Conventional CML Buffer

2.2 Limitations of a CML Buffer at High Frequencies

Figure 2 shows the half circuit diagram of the CML buffer which is a standard common-source amplifier.

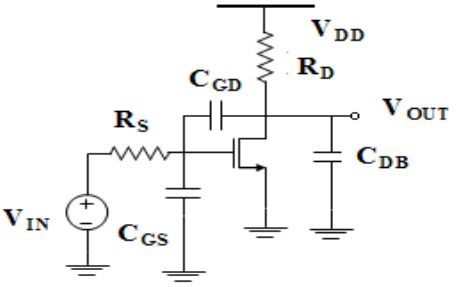

Fig. 2. Half circuit of CML buffer buffer

The dominant pole (ω_{p1}), and the first non-dominant pole (ω_{p2}) of this circuit are given approximately by

$$\omega_{p1} = 1 / [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_{D(} C_{GD} + C_{DB})] . \quad (1)$$

$$\omega_{p2} = \frac{R_S (1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D (C_{GD} + C_{DB})}{R_S R_{D(} C_{GD} C_{DB +} C_{GD} C_{DB +} C_{GD} C_{DB})} . \quad (2)$$

Due to the Miller effect, the gate-drain capacitance (C_{GD}) contributes significantly to the frequency response (through the term $R_s g_m R_D C_{GD}$ in the denominator of Eqn. (1). Also, the transfer function exhibits a zero given by $\omega_Z = g_m/C_{GD,}$ located in right half plane. C_{GD} creates a feed forward path from the input to the output at high frequencies, causing distortion in the output.

3 Proposed Architecture

The above mentioned issues because of miller capacitance can be resolved if source coupled pair is used instead of common source amplifier in half circuit. This architecture not only avoids input-output coupling, but also reduces the input capacitance, thereby increasing the maximum frequency of operation. Figure 4 shows the proposed architecture, which is two source coupled (or differential) amplifiers connected to provide a differential input and a differential output. One of the inputs of each differential amplifier (gates of M_2 and M_3) are connected to a 'dc' voltage, while to the other (Gates of M1 and M4), the differential input signals are applied. The outputs are taken at the drains of M2 and M3. When used as a buffer, for the case when the input voltage of M_1 goes high, M_2 is turned off, the entire tail current switches to M_1, and the output voltage at the drain of M_2 becomes V_{DD}. Simultaneously, the input at the gate of M_4 will go low, thus turning off M4, and the entire tail current of that differential pair flows through M_3, causing the drain of M_3 to be at ($V_{DD} - I_{SS}R_D$). Thus the differential output voltage of the circuit will be $I_{SS}R_D$.

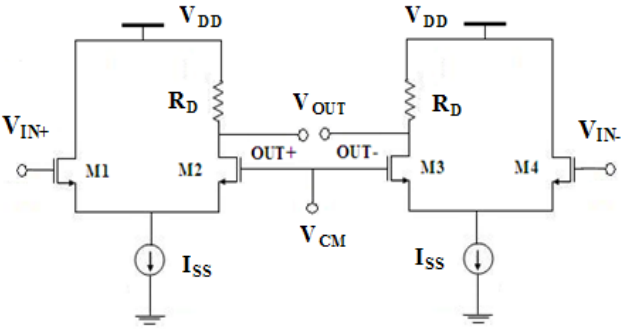

Fig. 3. Proposed Architecture

For this architecture approximate expressions for the dominant pole (ω_{p1}), and the first non-dominant pole (ω_{p2}), for a differential input voltage, are found to be:

$$\omega_{p1} = 1/[(R_s + R_D)C_{GD} + (R_s + 1/g_m)0.5\, C_{GS} + R_D\, C_{DB})] \quad . \tag{3}$$

$$\omega_{p2} = 1/K\,[R_s\, R_D\,(C_{GD}\, C_{DB} + C_{GD}\, C_{DB} + C_{GD}\, C_{DB})] \, . \tag{4}$$

Where, $K = (C_{GD}\, C_{DB} + C_{GD}\, C_{GS} + C_{GS}\, C_{DB})\,(R_s + 1/g_m)\, R_D + (R_D/g_m)$

$(C_{DB} + C_{GD} + C_{GS})\,(C_{DB} + C_{GD} + C_{GS3} + C_{DB3}) +$
$R_D\,[R_s\, C_{GD}\,(C_{GD} + C_{DB}) + C_{DS}\, C_{DS/}\, g_m)] \, .$

where R_S is the resistance of the voltage sources (not shown in the figure) connected at the inputs, the transconductance, and the capacitances are for the transistors M_1 and M_2 (which are assumed to be identical), unless there is a subscript "3" in the name, in which case they refer to the transistor M_3.Comparison of Eqns. (1) and (3) shows that the proposed architecture has a much higher dominant pole frequency, compared to the conventional CML buffer, Moreover, due to the source-coupled configuration of the former, two gate-source capacitances (C_{GS}) are seen in series by the input terminal, thus reducing this capacitance by a factor of 2 in the dominant pole expression.

4 Design Issues

The load resistor R is determined by impedance matching requirements (being typically between $50\,\Omega$ and $100\,\Omega$) and was taken to be $75\,\Omega$. For a given voltage swing (V_{SWING}), the current I_{SS} is given by $I_{SS} = V_{SWING}/R_D$.
For the entire tail current to flow only in one branch [1],

$$0.5V_{in} > [\, 2I_{SS}L / \mu CoxW \,]^{1/2} \, . \tag{5}$$

from which W_1 can be calculated. Also, for keeping the current source in saturation,

$$V_{CM} - V_{GS} > V_{BIAS} - V_T \, . \tag{6}$$

which yields,

$$W_1 > 2I_{SS}L / \mu CoxW(\, V_{CM} - V_{BIAS})^{\,2} \, . \tag{7}$$

W_1 then must be chosen to satisfy both Eqns. (5) and (7).

5 Simulation Results

The proposed circuit was designed in MOSIS 180nm CMOS technology [5] and simulated with Cadence Spectre. The supply voltage used was 1.8 V, with a common-mode dc voltage (V_{CM} in Fig. 3) of 1.2 V. At high speed the effect of package and transmission line parasitics must also be considered for off-chip loads. The package model was taken from Maxim's 3840 10-Gbps equalizer [6], and the transmission line model of Spectre was used .

Figure 4 shows the differential output of the buffer before package, for differential input of 10 GHz. The output shows a differential peak to peak of about 800 mV. Fig 5(b) shows the output of the buffer at offchip load(R_0C_0) as shown in Fig5(a)

Table 1 shows the different parameter values obtained from Fig. 4 and Figure 5 shows the output waveform for the same inputs at the off-chip load (includes effect of package and transmission line) which is 600 mV differential peak to peak.

Table 2 shows the rise and fall times obtained at the driver output, after the package and at the off-chip load.

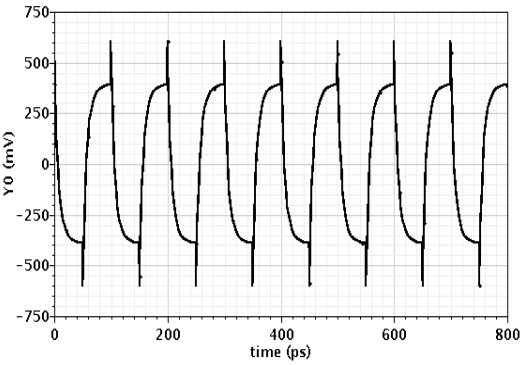

Fig. 4. Differential output at the output of buffer line

Table 1. Summary of buffer performance at the driver output

Parameter	Value
Rise time (T_r)	13.82s
Fall Time (T_f)	18ps
V_{OH}	1.78V
V_{OL}	1.39V
Vswing(single ended)	0.39V
Power dissipiation	22.32mW

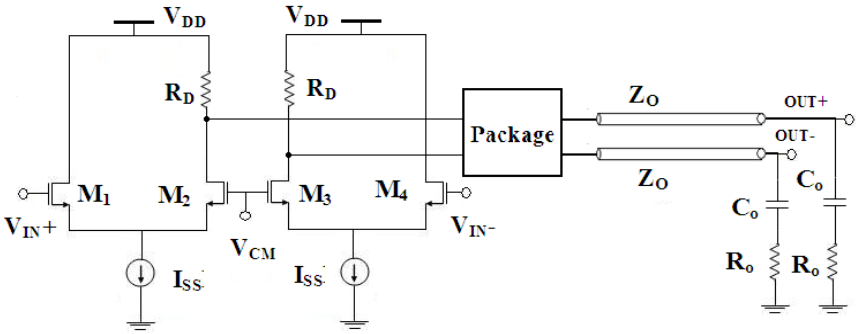

Fig. 5(a). Complete Schematic of output buffer with package and transmission line output at offchip load

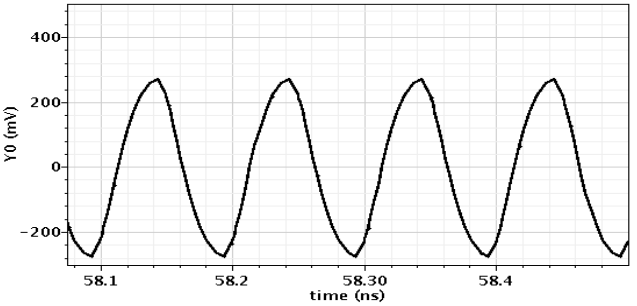

Fig. 5(b). Differential Output at off chip load

Table 2. Rise and Fall times at various point in the system

	At Driver	After Package	At off chip load
Rise time (T_r)	13.82ps	26.45ps	29.4ps
Fall Time (T_f)	18ps	28.32ps	28.4ps

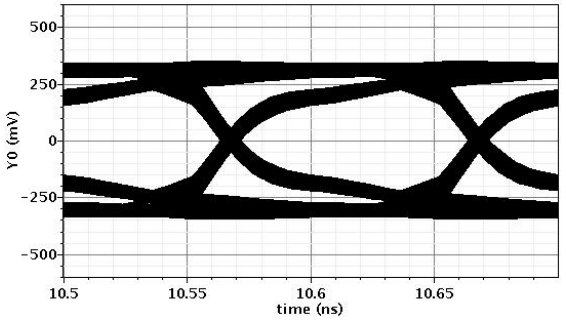

Fig. 6. Eye diagram of output for a 10 Gbps pseudo-random bit sequence input

At the off-chip load, an eye diagram is simulated using a pseudo-random bit sequence (2^5 -1) as input. Figure 6 shows the eye diagram obtained. Peak to peak jitter is calculated to be 4.95 ps, and an eye opening of ±125 mV which is quite acceptable for the OC-192 application.

6 Conclusion

A new high-speed CMOS buffer is proposed that can work at up to 10 Gbps, without the need of an inductive peaking architecture, thus saving on valuable chip area. The power consumption is comparable to previously reported work [7].

References

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