A Novel Input Capacitance Modeling Methodology for Nano-Scale VLSI Standard Cell Library Characterization

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Abstract. As the technology scales to 55nm and below, the traditional modeling methodology of input capacitance results in high deviation between the back-annotated delay values and the measured delay in Silicon. To reduce such a high deviation, novel modeling methodologies of input capacitance have been proposed in this paper. The proposed model have been used across different process and technology nodes using different test cases and back-annotated delay values were shown to have good agreement with the measured delay in Silicon. The proposal can be used to understand the device behavior; and based on device behavior; the methodology can be used to model the input cap accurately.

Keywords: pin capacitance, input cap, hspice, silicon, correlation.

1 Introduction

In this paper we talked about the basic method of improving the Silicon Vs STA (Static Timing Analysis) correlation [6]. As technology advances, the integration scale is shooting up. The timing constraint of a design has become very critical hence the redundant design margin need to be reduced to get better performance. To close any design, STA is the only viable method for chip-level timing analysis and therefore its accuracy should be of up most important.

There are many factors that affect the accuracy of STA. Among them, the input capacitance modeling of logic gates is an important factor because a significant amount of load capacitance is still occupied by the input capacitances of gates except for interconnects dominated sections such as clock trees and busses. In STA, the input capacitance of a gate is modeled as a lumped capacitance. There are a few papers that explain the importance of the capacitance modeling [1]–[4]. However, no paper has justified about choosing Max cap or average cap. Also, no paper has studied the input capacitance variation across different bias condition of PMOS and NMOS device. Also, although Synopsys Siliconsmart for library characterization measure input capacitance different input slew and output load condition [5], it is common to measure capacitance from 20% to 80% rise of input-signal. And among all measured

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value of cap, the Siliconsmart picks the max or min or average capacitance in a timing library. In case of max-cap, the STA can predict the longest delay without optimism so that we can safely check set-up constraints. On the other hand, if we want to analyze the shortest-path delay, the resulting timing is overestimated and there is a possibility of existing shorter delays, which will lead to hold violations.

In case of average-cap, the STA can predict the longest delay with some optimism in critical path; which can cause silicon failure. This paper talked about how to reduced pessimism and optimism in input pin capacitance measurement.

1.1 Input Pin Capacitance: HSPICE vs STA

STA reads input pin capacitance from the Liberty to calculate corresponding output delay and slew. As the liberty has only one static value of input pin capacitance, STA takes total FO cap and uses it to map the delay. In general Liberty takes average value of input pin capacitance calculated across different condition (from 20% to 80% input slew). As FO increase, the inaccuracy gets multiplied. To evaluate the discrepancy between actual gate cap and the gate cap seen by STA, an experiment is done on RO shown in Figure 1, it is found that the input-cap at nodes net1, net2, net3, … is always more than the input pin capacitance calculated by STA at these nets. This gives basic reason of miscorrelation of HSPICE vs STA.

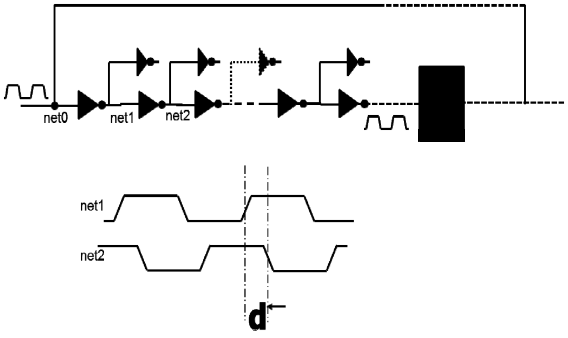

Fig. 1.

Figure 5 show input pin capacitance measured at each nets of the circuit shown in Figure 1. The capacitance in Liberty [5], which is based on average capacitance across different input slew and output load, is always less than the capacitance estimated by HSPICE simulation. SiliconSmart, the characterization tool, have option to choose range of integration for input pin cap. Default range is 20-80. However, for given range, the tool calculates the input pin capacitance for combination of slew/load.

1.2 Variation in Input Pin Capacitance

To study the input pin capacitance very closely, we have devised a method to estimate the instantaneous capacitance at each instance of input rise/fall. Figure 2 shows the

instantaneous capacitance at each voltage level of input slew, the plot is done across different input slew. The graph shows input pin capacitance variation more than 2X. It is a challenge to estimate one unique capacitance for Liberty file for a given cell.

To understand the behavior of input capacitance, we came up with new terms called Capacitance range which is described in next section.

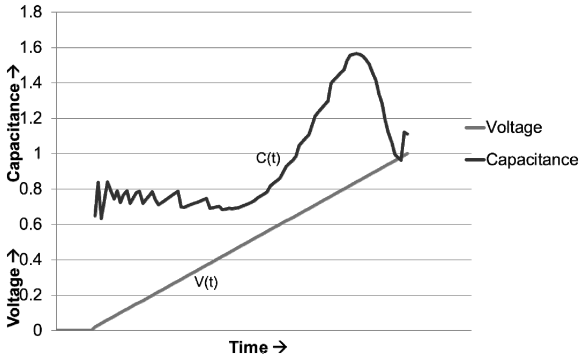

Fig. 2.

1.3 Capacitance Range

Capacitance range is the Capacitance calculated at different range of input slew. It starts from mid-point of input slew for very small range Δ, (50-Δ/2)% to (50+Δ/2)% and ends at the full range 0 to 100%. The Figure 4, shows input ramp(Aqua color), Instantaneous Cap (light Black), and capacitance range(dotted curve).

Ideally, input pin capacitance should be constant across different range of input slew, however, in reality, the cap changes with different range of input cap.

$$C = \frac{\int_{t_1}^{t_2} C(t)\,dt}{t_2 - t_1}$$

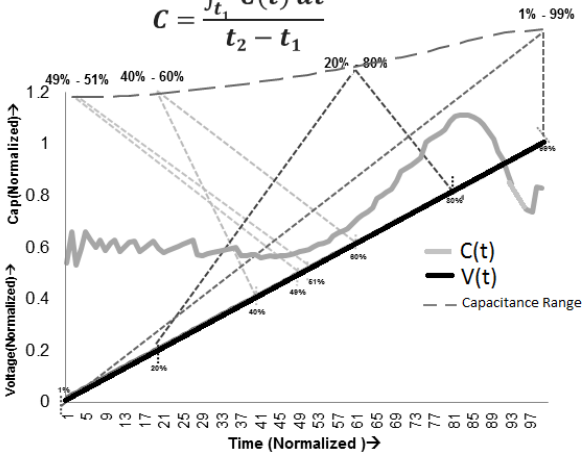

Fig. 3.

2 Limiting Capacitance (LC)

Figure 4 shows different range cap curve at different output load.

LC cap is coming out to be the best estimation of input cap. Correlation data shows LC cap correlates much better than traditional input cap.

Table 1 is the correlation result (Tradition Cap vs LC). Negative correlation number shows that STA is faster than HSPICE simulation. The Liberty with LC capacitance gives out very accurate correlation than the Liberty with traditional capacitance.

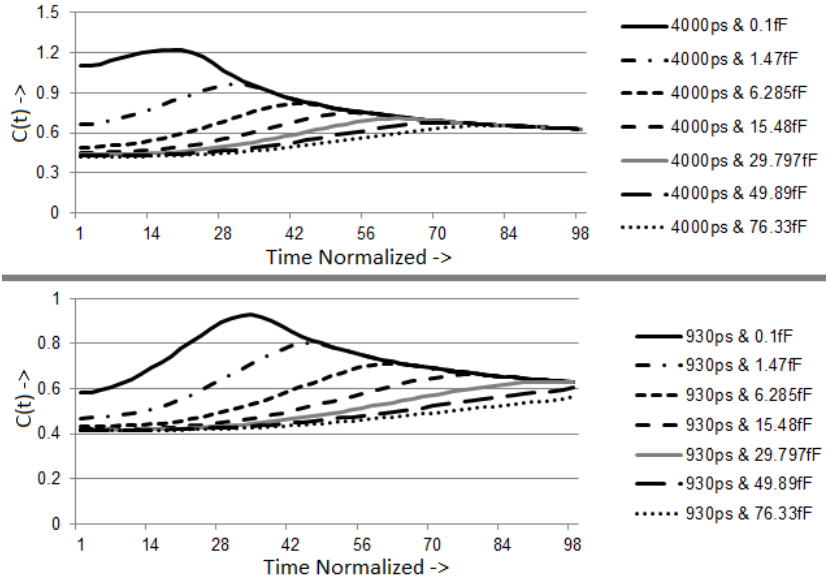

Fig. 4.

	net0	net1	net2	net3	net4	net5	net6	net7	net8
Slew Rise (ps)	75.58	96.62	96.83	96.79	96.83	96.79	96.79	96.79	96.75
Slew Fall (ps)	79.48	93.68	94.40	94.13	94.41	94.41	94.41	94.41	94.38
Average Cap(fF) 20% to 80%	6.04	6.05	6.04	6.04	6.04	6.04	6.04	6.05	6.04
Average Cap(fF) 0% to 100%	6.93	7.06	7.01	7.01	6.99	6.99	6.96	7.04	6.98
CAP from dotLib	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5

Fig. 5.

TEST CASE	Regular Liberty (NLDM/CCS)		LC Liberty (NLDM/CCSN)	
	STA nldm to spice	STA ccsn to spice	STA nldm to spice	STA ccsn to spice
INV CHAIN	-15%	-22%	2%	2%
BUF CHAIN	1%	-8%	3%	3%
DLY CHAIN	-2%	-2%	1%	1%

Fig. 6.

3 Conclusions

This paper discusses a method to model the gate input capacitance for accurate STA. For static timing analysis, we have to model the gate input capacitance, which gives the best characteristic of a given gate. Siliconsmart derives the equivalent capacitance by integrating over the full transition range or 20-80 transition range of the applied input signal. Conventionally, average of all input pin capacitance considered for all input slew and output load condition. However, this capacitance is less than the actual capacitance. Also, in some cases of traditional method, the capacitance is the maximum capacitance across all input slew/load; and it results pessimistic delay. The pessimistic delay estimation is reasonable for checking setup time constrains, but it can cause hold violation.

The proposed method derives the characteristic capacitance of logic gate and gives the most optimum input cap of the given gate. The result shows good correlation using LC Liberty Vs Traditional Liberty.

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