Impact of Fin Width and Graded Channel Doping on the Performance of 22nm SOI FinFET

Jose Joseph and Rajendra Patrikar

Department of Electronics Engineering
Visvesvaraya National Institute of Technology, Nagpur-440010
josejosephpala@gmail.com, rmpatrikar@ece.vnit.ac.in

Abstract. The potential impact of fin width and graded channel doping on the analog performance of 22nm n-channel FinFET are studied using well calibrated 3D TCAD simulations. It is ascertained that for FinFETs, lesser the fin width, better the characteristics. But limitations in lithography process curb the fin width to be scaled beyond 10nm. Stability of the fins patterned beyond 10nm width is to be viewed with suspected eyes. It is observed that Graded doping of the channel will improve threshold voltage and hence the ratio of I_{on} to I_{off} will also increase, which is desired for enhanced performance in analog applications.

Keywords: FinFET, graded doping, fin width, TCAD.

1 Introduction

FinFET is one of the emerging CMOS devices that use an ingenious architecture allowing better control over short-channel effects (SCE) with the aid of 3D geometry [1]. The use of metal gates help to adjust the threshold voltage and prevents gate depletion and dopant penetration that frequently appear in the conventional polysilicon gate architecture [2]. Traditionally, fin channel is selected as undoped to avoid the device mismatches.

Pertaining to electrostatic integrity of FinFETs, the ratio of the minimum gate length to the minimum fin width should be larger than 1.5 [3]. Therefore, it could be said that the minimum feature size in FinFET technology is the fin width, not the gate length [4]. Narrow fin width devices exhibits better immunity to SCEs and reduced Subthreshold slope [5]. The absence of body contact for the SOI FinFET puts limitations for threshold voltage tuning and can be accomplished either by complicated gate metal work function engineering or by channel doping [6]. Doped-channel FinFETs are suitable for system-on-chip applications requiring multiple threshold voltages on the same die [7]. In this paper, we try to analyze the performance variations of 22nm FinFET subjected to different fin widths and graded doping conditions. Critical device attributes like I_{on}, I_{off}, V_T, DIBL, Subthreshold slope etc. are investigated as a function of fin width and graded doping conditions.

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2 Device Structure and Simulations

A novel 22nm FinFET was simulated using well calibrated Sentaurus TCAD 3D simulations. The device structure was formed with the aid of Sentaurus Structure Editor in the TCAD package [10]. Device parameters chosen for simulation are as given in Table 1. In industry standard <100> Si wafers, mesa etch results in <110> fin side walls. Since the mobility in <100> plane and <110> plane are different, a double gate operation has been ensured by keeping a thick oxide layer of 20nm the top surface of the fin [8]. Hence the structure becomes double gate and the problem of different current conduction and mobility on two crystallographic planes were solved.

Table 1. Nomenclature and values of the parameters used in the simulated device

Parameter	Value	Parameter	Value
Gate Length	22nm	Side oxide thickness	1.1nm
Fin Height	40nm	Top oxide thickness	20nm
S/D Extension	40nm	S/D extension doping	1E+19 cm^{-3}
S/D HDD length	50nm	S/D HDD doping	2 E+20 cm^{-3}
S/D HDD width	56nm	Gate metal thickness	20nm

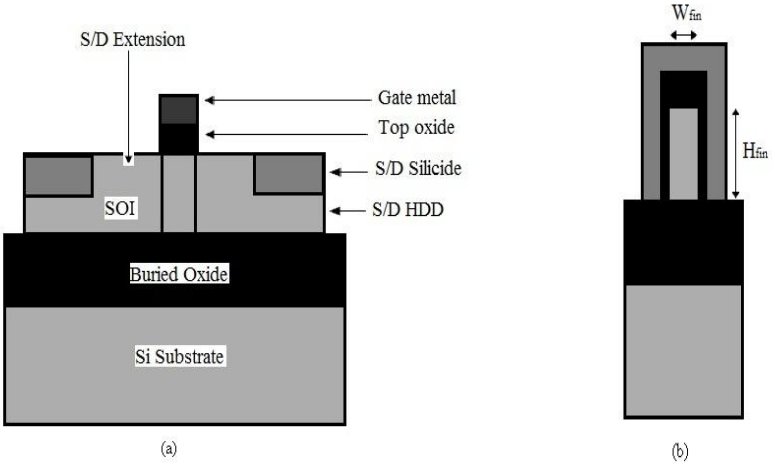

Fig. 1. FinFET structure used in simulations: (a) cross section along the length of channel and (b) cross section along the width of the channel

The gate metal work function is selected as 4.5eV and resistivity as 5.44E-6 Ω.cm, which corresponds to the material properties of Tungsten [9]. To improve the speed of the device, S/D silicides with resistivity of 2E-6 Ω.cm are employed. In spite of their positive impact on the speed of the device, silicides provide high temperature stability and excellent process compatibility with standard Si technology. Heavily doped

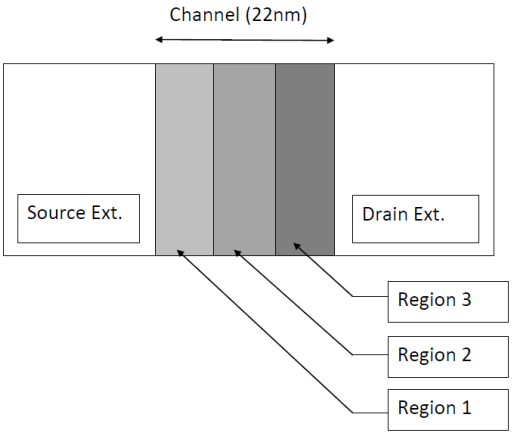

Fig. 2. 2-D Schematic diagram of graded doping profile used for simulations

Source/Drain (HDD) and abrupt box shaped Source/Drain extensions have been defined analytically. Device cross sections along the length and width of the fin are illustrated schematically in Fig. 1(a) and Fig. 1(b) respectively.

Fig.2 portrays the doping profile selected for graded doping simulations. The channel is partitioned into 3 regions of equal length. Simulations were carried out by assigning heavy doping near to source and gradually reducing to drain and vice versa. The results of these simulations were compared with those of constant channel doping of 1E+16.

Mobility models including doping dependence, high-field saturation (velocity saturation), and transverse field dependence are specified for all the simulations. '*BandGapNarrowing (OldSlotboom)*' is the silicon bandgap narrowing model which is employed for determining the intrinsic carrier concentration [10]. Drift-Diffusion equations coupled with Continuity and Poisson's equations were solved for the device structure shown in Fig.1, using Sentaurus Device from the TCAD package.

3 Results and Discussion

3.1 Impact of Fin Width

Width of the fin has been varied from 10nm to 16nm in steps of 2nm, keeping all the other device parameters constant. For the simulations in this section, undoped channel is selected. As expected the devices with lower fin widths are exhibiting reduced SCEs, but reducing the fin width increases the S/D resistance, which as shown in Fig. 3, leads to the reduction of normalized drain current.

It can be noted from Fig. 4 that the ratio of I_{on} to I_{off} is decreasing as we increase the fin width. When the width of fin is increased from 10nm to 16nm, approximately two orders of decrease in magnitude for I_{on}/I_{off} have been observed and it will affect the performance of FinFET for analog applications. Threshold voltage was also decreasing as we increase the fin width. Similar variations for threshold voltage is demonstrated in [15] for higher fin width devices.

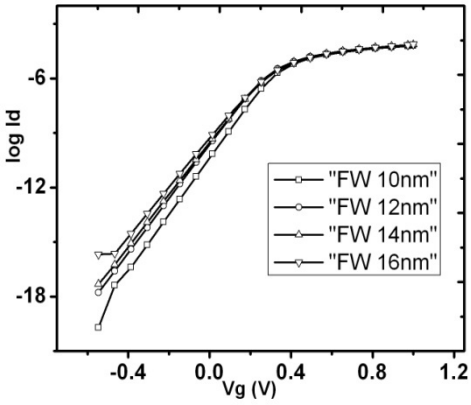

Fig. 3. Log I_d versus V_g curves for different fin widths

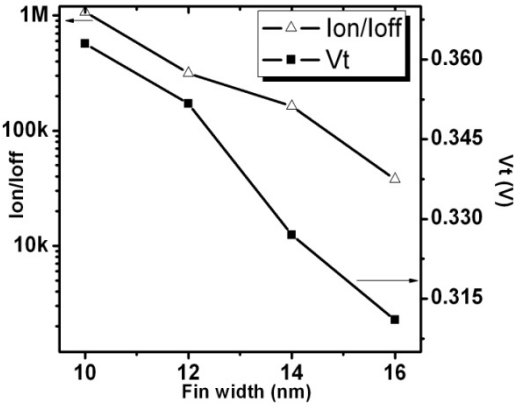

Fig. 4. Variation of I_{on}/I_{off} and threshold voltage with respect to fin width

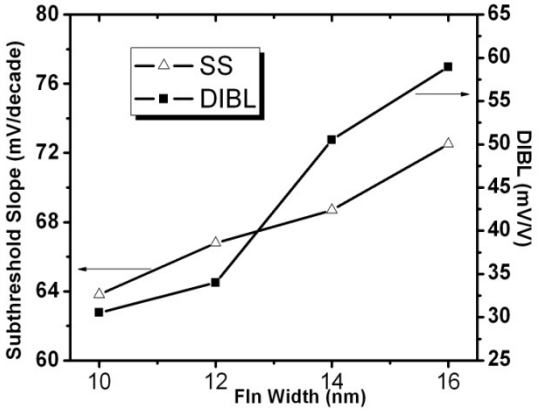

Fig. 5. Fluctuation of Subthreshold slope and DIBL with fin width

As shown in Fig. 5, Subthreshold slope increases linearly whereas DIBL was found increasing in discontinuous steps. Both these trends testify that for better performance, one should keep the fin width as low as possible. AC small signal simulation at 50GHz reveals that gate capacitance C_{gg} increases linearly as we augment the fin width. Transconductance will also build up with the fin width as shown in Fig. 6.

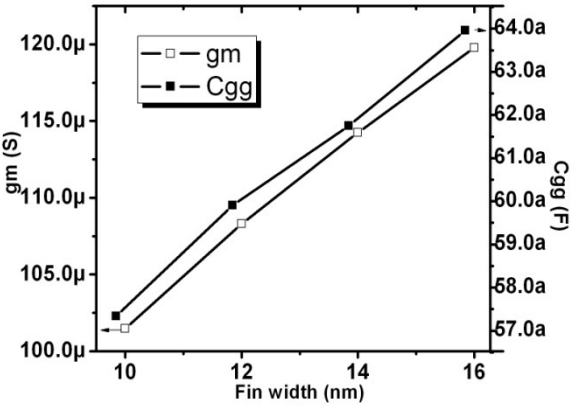

Fig. 6. Effect of fin width on transconductance and gate capacitance

All the parameter variations observed here are in closer agreement with those proposed in [11] for long channel devices devices.

3.2 Impact of Graded Channel Doping

Asymmetric channel devices have been studied thoroughly by many authors [12] [13]. In all those works, the channel is divided into two regions and heavy doping is assigned near to Source allowing the channel region near Drain to act as a Lightly Doped Drain (LDD). In this work, we, for the first time, investigated the performance variation of 22nm FinFET under two different graded channel conditions. Table 2 shows the doping profiles selected for these simulations.

Comparison of I_d-V_g characteristics for constant doping with GC1 and GC2 is elucidated in Fig. 7. It is to be noted that in this section, constant doping refers to a Boron channel doping of value 1E16 cm-3, unless otherwise specified.

Table 2. Graded channel profiles selected for simulations

Nomenclature	Region 1	Region 2	Region 3
GC1	1E18 cm^{-3}	1E16 cm^{-3}	1E14cm^{-3}
GC2	1E14 cm^{-3}	1E16cm^{-3}	1E18cm^{-3}

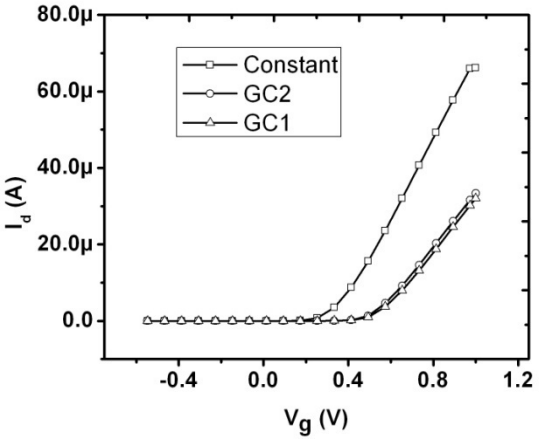

Fig. 7. Id-Vg characteristics of constant and graded doping

The variation of different device performance parameters with respect to channel doping type are listed in Table 3. Because of the higher impurity scattering in graded channel device, the conduction current in the Subthreshold region will come down and hence threshold voltage will rise. Remarkable reduction in I_{off} is also observed in both GC1 and GC2.

Table 3. Device performance parameters with different doping types

Doping Type	V_T (V)	**SS** (mV/decade)	I_{on}/I_{off}	**gm** (S)	C_{gg} (F)
Constant	0.351	66.79	3.15E5	1.082E-4	5.990E-17
GC1	0.564	62.89	2.28E8	7.210E-5	5.203E-17
GC2	0.549	63.51	1.95E8	7.239E-5	5.274E-17

It can be certified that for deep sub-micron technology nodes, GC1 offers advantages in analog performance than GC2, which is in closer agreement with the work explained for long channel SOI devices in [13]. Employing lesser doping near the Drain reduces the electric field and hence the total number of carriers generated by impact ionization will also be reduced. Since the channel is too short, the confinement of doping to the regions as depicted in Fig. 2 cannot be guaranteed as such in actual fabrication scenario and the device may tend to behave like a heavily doped one which puts limitation in adopting channel engineering for the deep sub-micron technology nodes. AC simulations at 50GHz show that gate capacitance C_{gg} is lowest for GC1 than GC2 or constant doping conditions.

It is also worth noting that the effect of GC1 on the transconductance is not so prominent. Since transconductance has a direct dependency on the mobility of carriers, variation in mobility is also negligible. On the other hand, the ratio of I_{on} to I_{off} is increasing by two orders of magnitude which is a striking advantage of the graded channel devices for analog applications.

4 Conclusion

Performance variation of 22nm n-channel FinFET subjected to different fin widths and channel graded doping have been analyzed in this work. For better performance, one needs to scale the fin width down to 10nm or lesser, taking the stability of the as formed fin into consideration. Graded doping in the channel helps one to improve the performance of FinFET for analog applications.

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