An Improved g_m/I_D Methodology for Ultra-Low-Power Nano-Scale CMOS OTA Design

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Abstract. This paper presents an improved g_m/I_D methodology for the design of low-power CMOS operational transconductance amplifier (OTA) circuit using nano-scale CMOS technology. This methodology takes into considerations the dependence of the Early voltage parameter with the bias points of a nano-scale MOS transistor. With such considerations, the DC voltage gain of the circuit can be controlled by adjusting the bias points of the transistors and keeping the channel length constant. The advantage of the improved methodology over the traditional methodology has been discussed and illustrated with simulation results.

Keywords: Nano-scale, g_m/I_D, Early Voltage, DIBL, OTA.

1 Introduction

The design of integrated circuits with ultra-low power dissipation is becoming an essential requirement considering the fact that most of the present day applications are battery operated [1]. In addition, with the scaling of transistor dimensions in nano-scale CMOS technology, it is becoming important to design with low supply voltage for better reliability of the integrated circuits. The main drawback associated with the scaling of supply voltage with technology generation is that the threshold voltage of MOS transistors do not scale as such with technology generation. Therefore, the design of nano-scale analog circuits with scaled supply voltage, is although an essential requirement, is extremely challenging. In the design of analog integrated circuits, the step of selecting device sizes and biases is crucial to enhance the final performance, power, and yield of the circuits. The g_m/I_D methodology [2,3] enables the designers to fix currents and transistors widths of CMOS analog circuits so as to meet specifications such as gain-bandwidth while optimizing attributes like low power and small area. The sizing method takes advantage of the transconductance g_m to drain current I_D ratio and makes use of either 'semi-empirical' data or compact models. The traditional g_m/I_D methodology does not explicitly consider the dependence of the Early voltage parameter upon the operating bias points of the transistor [4]. The Early voltage parameter is considered to be constant depending upon the chosen channel length of the transistor. Therefore, the gain specification is tried

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to be satisfied by biasing the transistors in the weak inversion region and varying the channel length. But this in many cases, increase the area of the circuit.

This paper presents an improved g_m/I_D methodology where the explicit dependence of the Early voltage parameter on the operating bias points is taken into considerations. It has been shown through simulation results that this parameter significantly depends upon the drain bias for nano-scale MOS transistors. This is because of the combined effects of the channel length modulation and drain induced barrier lowering phenomenon. This dependence is utilized to obtain the desired gain, keeping the channel length constant. Thus the total area of the circuit is not unnecessarily increased. The bias voltages of the input transistors are determined automatically rather than to find out through trial and error method as done for the traditional methodology.

2 The Traditional g_m/I_D Methodology

The g_m/I_D based circuit sizing procedure is based on the relation between the ratio of the transconductance over dc current g_m/I_D and the normalized current $I_N = I_D/(W/L)$. The relation between the g_m/I_D parameter with the operating region of the transistor may be written as follows

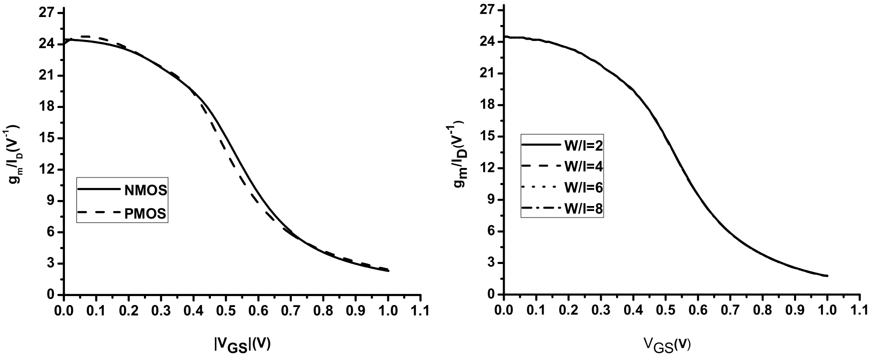
$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial (\ln I_D)}{\partial V_{GS}} = \frac{\partial \left\{ \ln \left[\frac{I_{DS}}{\left(\frac{W}{L}\right)} \right] \right\}}{\partial V_{GS}} \tag{1}$$

The maximum value of the g_m/I_D ratio is observed to be in the weak inversion region and the value decreases as the operating point moves toward strong inversion when V_{GS} is increased as shown in Fig. 1(a) It may be noted that the relationship between the g_m/I_D ratio and V_{GS} is independent of the transistor sizes. Therefore, this relationship is a unique characteristic for all transistors of the same type (n-channel MOS or p-channel MOS) in a given batch. This is shown in Fig. 1(b). The universal characteristic of the g_m/I_D versus I_N curve (shown in Fig. 2) is used to determine the aspect ratio of a transistor, which is then subsequently used to determine the channel width, assuming a fixed value of the channel length.

For a MOS transistor, the magnitude of the intrinsic voltage gain is given by

$$A_v = g_m r_0 = \left(\frac{g_m}{I_D}\right)(I_D r_0) = \left(\frac{g_m}{I_D}\right) V_A \tag{2}$$

where V_A is referred to as the Early voltage of the transistor. Assuming V_A to be constant for a particular channel length of a transistor, the intrinsic gain is determined by the g_m/I_D ratio. Therefore, the intrinsic gain of a MOS transistor is maximum in the weak inversion region and reduces as the operating point moves towards the strong inversion region. Therefore, an important guideline to get high gain for a MOS transistor, is to bias the transistor in the weak inversion region with as low V_{GS} as possible. Under weak inversion region very small



(a) Variation of g_m/I_D for n-channel and p-channel MOS transistor.

(b) Variation of g_m/I_D with different aspect ratio.

Fig. 1. Variation of g_m/I_D

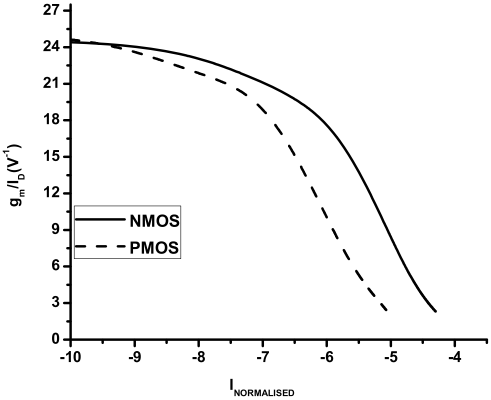


Fig. 2. Variation of g_m/I_D with normalized current

amount of drain current flows, which implies small amount of power dissipation. Therefore, by biasing the MOS transistor in the weak inversion region, it is possible to obtain high gain with very small power dissipation.

2.1 Shortcoming of the Traditional Methodology

An important shortcoming of the traditional g_m/I_D methodology is that it does not explicitly considered the dependence of the Early voltage V_A on the operating bias points (V_{DS}, V_{GS}) of the transistor. The Early voltage is considered to be constant depending upon the channel length. However, for nano-scale MOS transistors, the Early voltage is found to be significantly dependent upon the bias voltages. The intrinsic gain of a MOS transistor is dependent upon the Early voltage, which in turn can be controlled by the operating bias points.

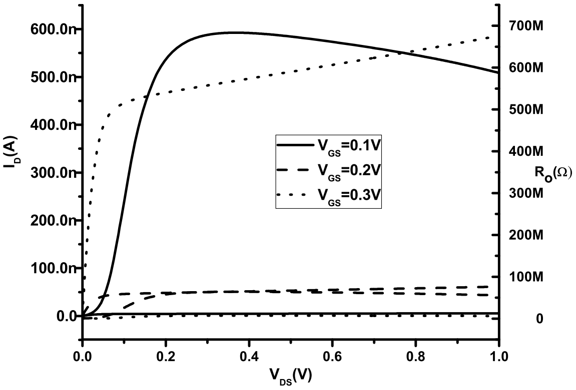


Fig. 3. Variation of drain current and output resistance with drain bias

Therefore, it is possible to control the gain of a MOS transistor within a moderate limit by controlling the bias points keeping the channel length constant.

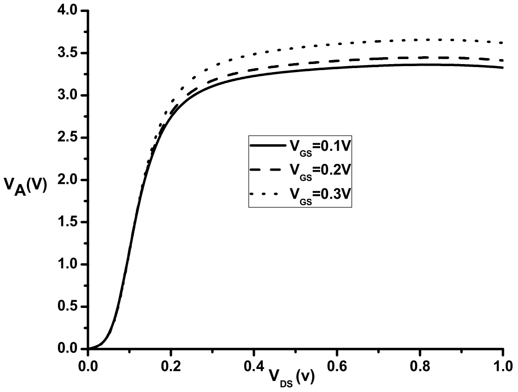


Fig. 4. Variation of Early Voltage with drain bias

3 The Improved g_m/I_D Methodology

This section presents the improved g_m/I_D methodology. The study of the variations of the Early voltage is discussed in the following sub-section, followed the description of the methodology.

3.1 Variations of the Early Voltage with the Operating Bias Points

The variations of the drain current and output resistance with the drain bias of an n-channel MOS transistor operating in the weak inversion region is shown in Fig. 3. It is observed that as the drain bias is increased beyond the saturation value, the drain current increases with drain bias. Therefore, the output resistance values reduce with drain bias. The physical causes are the channel length modulation effect and the DIBL phenomenon [5,6]. For scaled MOS transistor, the threshold voltage of a MOS transistor reduces as the drain bias is increased. This is referred to as the DIBL phenomenon. However, as the gate bias is increases the fall of output resistance is somewhat less. This is because with the increase of gate bias, the gate achieves better control and due to carrier mobility degradation effect, the magnitude of the drain current is reduced. This physics of the scaled MOS transistor has significant impact on the Early voltage of the MOS transistor which is defined as

$$V_A = \frac{I_D}{\left(\frac{\partial I_D}{\partial V_{DS}}\right)} \tag{3}$$

The variations of the Early voltage with drain bias for different V_{GS} are shown in Fig. 4. It is observed that for scaled MOS transistor, the Early voltage does not remain constant with the operating bias points. Selection of suitable drain voltage is therefore, extremely important. In addition, the magnitude of the Early voltage also depends upon the gate bias to some extent. This characteristics of the Early voltage needs to be incorporated within the design procedure. This is discussed in the next section.

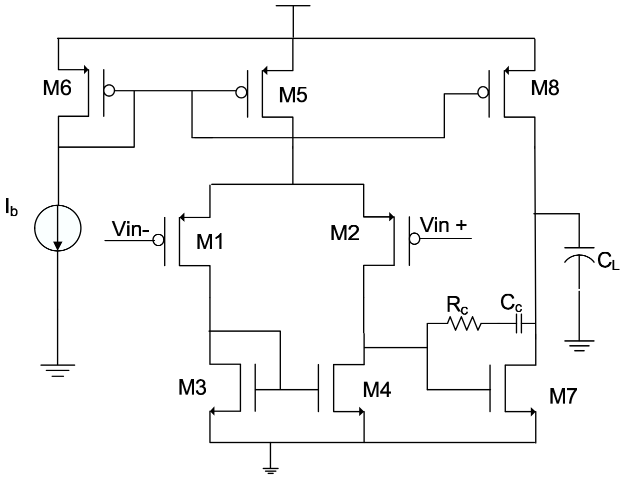


Fig. 5. Two-stage Miller OTA Circuit

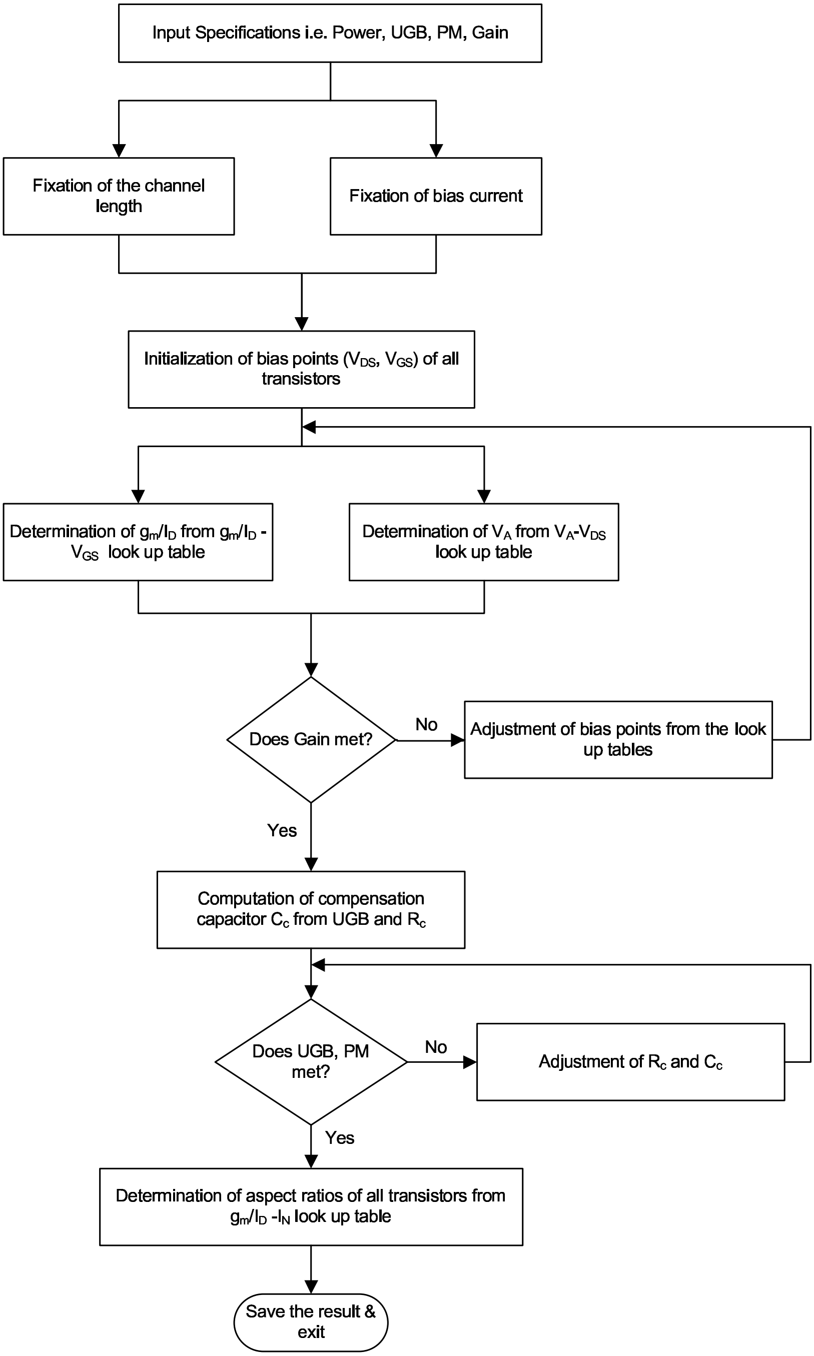


Fig. 6. Flow chart of the improved g_m/I_D methodology

3.2 Improved g_m/I_D Methodology

The chosen two stage Miller OTA circuit is shown in Fig.5. Considering the dependence of the Early voltage parameter V_A on the operating bias conditions of the MOS transistor, the improved g_m/I_D methodology for the design of a nano-scale CMOS OTA circuit is shown in Fig. 6. The input specifications are the desired gain, bandwidth, phase margin and power consumption of the circuit. Depending upon the magnitude of the desired gain, the channel length of the MOS transistors are to be fixed. For moderate gain $\simeq 60dB$, the channel length may be considered to be 100nm. However, if larger gain is required, the channel length needs to be increased. The bias current is fixed depending upon the power consumption requirement of the circuit. The design process starts with initialization of bias points for all the transistors such that these operate in the weak inversion region and the total potential drop across any branch of the circuit, starting from the supply to the ground does not exceed the supply voltage. The g_m/I_D and the Early voltage parameter V_A of each transistor are computed from the corresponding look up tables. Since the g_m/I_D and the drain current I_D of each transistor are known, the corresponding g_ms are computed.In order to satisfy the desired gain, the bias voltages are adjusted and the procedure is iterated until the desired gain is achieved. Next the compensation capacitor C_c and the nulling resistor R_c are determined as follows [7]

$$C_c = \frac{g_{m1}}{2\pi UGB} \tag{4}$$

$$R_c = \frac{1}{g_{m7}} \frac{C_c + C_L}{C_c} \tag{5}$$

In order to achieve the desired gain bandwidth and the phase margin, the values of the compensation capacitor and the nulling resistor are adjusted. Once all the desired specification are met and the g_m/I_D and I_D of all transistors are known, the corresponding aspect ratios are determined.

The major advantages of the present g_m/I_D methodology over the traditional methodology are as follows

1. The dependence of the Early voltage parameter on the operating bias points of the transistor are considered in the design process. This is utilized to obtain the desired gain, keeping the channel length constant. Thus the total area of the circuit is not unnecessarily increased.
2. The bias voltages of the input transistors are determined automatically rather than to find out through trial and error method as done for the traditional methodology.

4 Results and Discussion

The desired specifications are (1) gain $A_v > 60dB$, (2) $UGB > 45KHz$, (3) $PM > 55^0$ and (4) power dissipation $P < 350nW$. The chosen CMOS technology is 45-nm with supply voltage of 1V. The circuits are simulated with BSIM4 compact model [8] and PTM model parameters [9] under HSPICE simulation environment.

The OTA circuit with the desired specifications is designed with the traditional methodology as well our methodology for comparison purpose. The SPICE simulation results as obtained from the traditional methodology are summarized in Table. 1.

Table 1. Simulation results for design by the traditional methodology L=100nm

Parameters	Specifications	Traditional
A_v	$> 60dB$	41.4dB
UGB	$> 45KHz$	56KHz
PM	$> 55^0$	86^0
CMRR		72dB
ICMR		0.065 V to 0.9 V
PSRR		80.4 dB @ (0.01 to 200)Hz
Slew rate		25V/ms
P	$< 350nW$	299nW

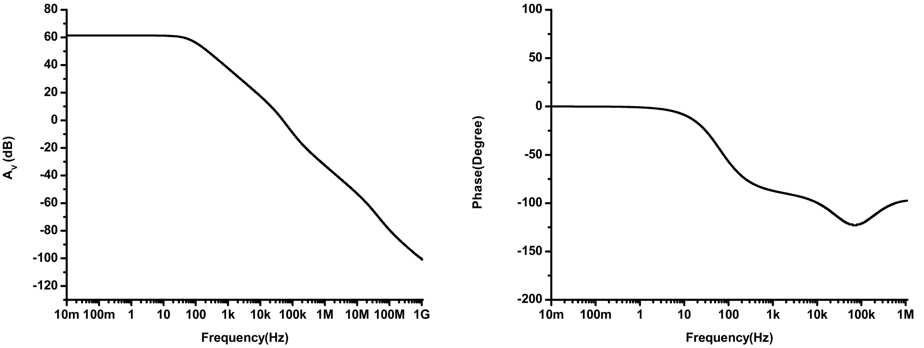
Table 2. Simulation results for design by our methodology in two iterations L=100nm

Parameters	1^{st} iterations	2^{nd} iterations
A_v	56.2dB	61.4dB
UGB	54KHz	50.4KHz
PM	60^0	60^0

Table 3. Simulation results for design by our methodology L=100nm

Parameters	Specifications	Our Method
A_v	$> 60dB$	61.4dB
UGB	$> 45KHz$	50.4KHz
PM	$> 55^0$	60^0
CMRR		67.7dB
ICMR		0.05 V to 1 V
PSRR		84 dB @ (0.01 to 200)Hz
Slew rate		29V/ms
P	$< 350nW$	299nW

It is observed that the desired gain could not be achieved with the traditional methodology considering the channel length to be 100nm. The traditional methodology under this circumstance demands increase of the channel length, which means increase of the consumed area.



(a) Gain Plot of the design with our methodology..

(b) Phase Plot of the design with our methodology.

Fig. 7. Gain and Phase Plot

The OTA circuit is designed for the same specification and the channel length using the present methodology. The specifications are satisfied with two iterations. For these two iterations, the results are summarized in Table. 2. The AC analysis plots for the design with our methodology are shown in Fig.7(a), 7(b). The final simulation results are tabulated in Table. 3. It is observed that the design with our methodology satisfies all the desired specifications even at the channel length of 100nm.

5 Conclusion

The traditional g_m/I_D methodology does not consider the variations of the Early voltage of the transistor with the operating bias points. The Early voltage is kept constant for a particular channel length. However, in the nano-scale domain, the Early voltage significantly depends upon the drain bias due to the combined effects of channel length modulation and DIBL phenomenon. This has been extensively studied in the present work in the 45-nm CMOS technology. By taking this variation of the Early voltage with the operating bias points, into considerations an improved g_m/I_D methodology has been proposed. The methodology has been demonstrated with a numerical results.

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