Resistive Sensor Interfacing

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Abstract. This chapter has the aim to give a complete overview on the first analog front-ends, describing some circuit and system solutions for the design of electronic interfaces suitable for resistive sensors showing different variation ranges: small, as in dedicated-application GMR sensors; wide, especially referred to GMR sensing devices whose baseline is unknown. After a description of the main interface parameters, the authors present several solutions, most of which do not require any calibration. These solutions are different according to the entity of resistive sensor variations, can utilize either AC or DC excitation voltages for the employed sensor and are developed in Voltage-Mode (VM, which considers the use of either the Operational Amplifier (OA) or the Operational Transconductance Amplifier (OTA) as main active block) as well as in Current-Mode (CM) approach (being in this case the Second Generation Current Conveyor (CCII) the active device). The described interfaces can be easily fabricated both as prototype boards, for a fast characterization, and as integrated circuits, also using modern microelectronics design techniques, in a standard CMOS technology with Low Voltage (LV) and Low Power (LP) characteristics, especially when designed for portable applications and instrumentation. Moreover, thanks to their reduced sizes in terms of chip area, the proposed solutions are suitable for being used for sensor arrays applications, where a number of sensors is employed, as in portable systems, to detect different environmental parameters.

1 Sensors and Electronics

Introduction on Signal Conditioning

A measurement sensor system is typically formed by a number of active and/or passive blocks, as shown in Figure 1, able to reveal and quantify physical/chemical phenomenon variations by means of a sensing element named sensor. In particular, the latter has to be processed by a suitable analog signal conditioning circuit, named interface, which allows to readout of the information coming from the sensor so providing a suitable output signal easy to display or to elaborate through an analog-to-digital converter (ADC) processing element. On the other hand, through an electronic interface, it is possible to detect any measurand variation as an electrical quantity which can be furtherly processed by means of a Personal Computer (PC), a microcontroller (μC), a microprocessor (μP), and so on.

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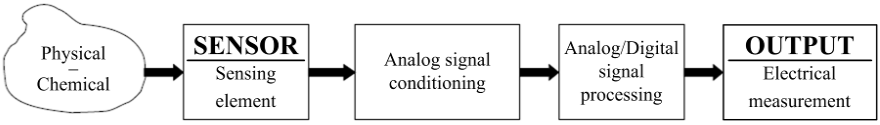

Fig. 1. Block scheme of a measurement system composed by sensor, signal conditioning and processing circuits

The need of novel sensors and related electronic interfaces showing small dimensions and the capability of working with reduced both supply voltages (Low-Voltage, LV) and power consumption (Low-Power, LP), especially in portable applications, is in a continuous growth. In particular, when both sensor and electronic circuitry for its interfacing, which have to be developed in a suitable integrated technology (*e.g.*, a standard CMOS), can be also combined into only one chip, it is possible to implement the so-called "Smart Sensor" [1-4].

Clearly, as stated above, sensors and electronic interfaces are a sub-set of measurement systems and, therefore, their performance should be expressed through suitable parameters, which will be listed and detailed in the next Paragraph. In this sense, the design or the use of an electronic interface is strictly related to the problem of the detection and quantification of the physical/chemical measurand. More in general, the measurement corresponds to a comparison of the measurand with a reference quantity (which, ideally, is a constant value coming from theoretical calculations).

The measurement equipment must be as "ideal" as possible, so to avoid the introduction of errors. This means that the perturbation introduced by the measurement action should be negligible for the desired level of accuracy (otherwise impedance loading effects must always be taken into account and properly evaluated). Therefore, in practice, some preliminary simulations are necessary for a more detailed analysis of the circuit behaviour.

Another important concept is the linear time-invariance of the sensor system, related to its transfer function. The latter, in practical cases, may be only approximately constant within a determined range of frequencies, called bandwidth. All the non-ideal systems have a limited speed and, therefore, have a finite bandwidth. Since that non-ideal systems are slowly time-variant, typically the time-invariance hypothesis is possible.

Let us now give more details about the interfacing of resistive sensors. Generally, sensors that behave as pure resistors as well as those sensing elements which do not bear an alternating voltage (*i.e.*, an AC excitation signal), since they give bad responses and lower lifetimes, can be biased through a constant voltage value (*i.e.*, a DC excitation signal), especially when, for several specific applications, it is also possible to neglect the effect of their parasitic components (*e.g.*, parasitic capacitance). On the contrary, in some application fields, these parasitics have to be known so to have a more complete information about the sensor [3-7].

Nevertheless, when the sensor can be modelled through a resistance, whose baseline is known and/or can be estimate, and that, in particular, varies into a reduced range (generally few percent but, however, not more than two-three decades, see next Paragraphs and Sections) and/or its baseline is known (*e.g.*, previously evaluated), the

Resistance-to-Voltage (*R-V*) conversion can be utilized for the resistive sensing interfacing [7-14]. Typically, this technique applies a constant voltage as sensor excitation so to measure the change of conductivity of the resistive sensing element. In this case, the simpler electronic interfaces, which perform the *R-V* conversion, are both the voltage divider and its "fully differential" version, known as Wheatstone bridge. Drawbacks of this approach are the very reduced signal level (typically comparable to the noise level) and the limitations due to the saturation (limited by supply voltage) of employed devices [7,10,15-18].

Therefore, if larger variations of sensor resistive values occur (see next Paragraphs and Sections) and/or, more in particular, the sensing element baseline is unknown and/or unpredictable, it is preferable to perform the Resistance-to-Time (*R-T*) conversion, where the "time" is often the period of a repetitive (i.e., periodic) waveform [7-18]. In this sense, more in detail, considering the state of the art of the manufacturing, the sensor resistance value may vary also across several decades, being normally the combination of three variable components: the nominal baseline, the deviation from this nominal baseline (due to ageing, working temperature, operating condition, etc.) and the resistive sensing element variation due to the physical/chemical phenomenon to be revealed. Since each contribution can be in the order of one-two decades, wide range sensors have to be considered (*e.g.*, in GMR sensors the starting values can be very different, varying from few Ω up to hundreds of kΩ). Typically, an *R-T* approach is based on an oscillator architecture which exploits the sensor as resistive element to be excited by a switched voltage (i.e., the AC excitation voltage). In this case, the simpler electronic interface which operates an *R-T* conversion is formed by a basic square wave generator, whose output voltage period *T* is directly dependent on the sensor resistance value.

This kind of solution allows both to avoid the use of high-resolution pico-ammeters, scaling factors, switches, etc., and to employ the same output periodic waveform to provide the AC-excitation to the sensor.

Moreover, since this type of wide range sensor signal conditioners covers several magnitude decades, it does not require any calibration procedure and/or manual settings (i.e., the so-called "uncalibrated" system) and its frequency output (i.e., "digitalized" output signal) offers a number of benefits compared to voltage output circuits, such as improved noise immunity (*e.g.*, offsets, frequency disturbs, etc.), easiness in multiplexing, insulation, signal processing, and so on. Unfortunately, sometimes these interfaces can show higher errors in sensor resistance estimation, when compared to *R-V* (*e.g.*, bridge-based) solutions; therefore, active elements must be accurately designed with good performances, especially in terms of time responses (*e.g.*, high Slew-Rate, SR, values) and low voltage and current offsets.

However, in the literature, different solutions for wide range resistive sensor interfaces which perform *R-V* conversion are also available. Some of them utilize amplifiers with scaling factors, but their drawbacks are related to the need of high-resolution ADCs and the difficult calibration procedures which are required when the sensor baseline is unknown. On the contrary, new recent approaches, considering "uncalibrated" interfaces always operating the *R-V* conversion, have been proposed in the

literature so that, especially when the resistive sensor baseline or its variation changes for different decades (also up to 5-6 or more), better estimation characteristics are ensured.

Active Blocks Main Basic Concepts: OA and CCII

The name of the "*Operational Amplifier*" was originally adopted for a series of high performance DC amplifiers used in analog computers. These amplifiers were used to perform mathematical operations applicable to analog computation such as summation, scaling, subtraction, integration, etc. [19-21].

In practice, an OA is a DC-coupled high-gained electronic voltage amplifier showing a differential input and a single-ended output. It produces an output voltage that represents the difference between the two input terminals, multiplied by the gain *A*. Since this active block has been designed for use in a feedback loop, ideally it shows the following characteristics: an infinite input impedance (i.e., no current flows into the input terminals); a zero output impedance (i.e., it can drive any load impedance to any voltage); an infinite open-loop voltage gain *A*; no bandwidth limitations; a zero output voltage for a null input voltage difference (i.e., zero voltage offset). As a consequence, without any negative feedback, the OA would act like a comparator of its inputs.

The OA can be internally implemented by different cascaded stages, such as a differential input to single output amplifier, a high gain stage with Miller capacitive compensation, a voltage buffer providing a high output current and a low output impedance.

Nowadays, the applications of OAs have become very widely diversified, in both linear and non-linear applications, such as: single-input single-ended voltage amplifier, differential voltage instrumentation amplifier, integrator, differentiator, comparator, voltage follower, ADC, DAC, etc.

Nevertheless, interfacing a sensor system with a voltage amplifier, based on OA, requires the matching between the sensor/signal conditioning output with the amplifier input. In general, sensors can provide either a single-ended or differential output. In the first case, all the inputs are referenced to system ground. Differential signals provide a positive and a negative signal with the positive output referenced to the negative one. In addition, it is important to consider also that a common-mode signal refers to a common voltage, with the same magnitude and phase that appears on both differential inputs of an amplifier. On the contrary, the Common-Mode Rejection Ratio (CMRR), generally defined as the ratio between the differential voltage gain versus the common-mode voltage gain, is specified for fully-differential inputs and describes the amplifier capability to reject a common-mode signal.

Starting from these considerations, it is possible to introduce the following three common input structures related to single-ended or differential output sensors: single-ended, pseudo-differential or fully-differential voltage amplifiers. Obviously, there are trade-offs with each structure that should be considered. In addition, consider that if the analog signal-conditioning circuitry is used between the sensor and next digital processing sub-system (*e.g.*, an ADC), this circuitry can affect, for example, the digital block input structure choice.

Anyway, the simplest method to be considered is to use a single-ended amplifier when measuring single-ended signals. In this case, all the signals are referenced to a common ground and each channel is connected to a specific input pin. It must be highlighted that the analog ground pin is shared between all inputs. Because of its behavior, the single-ended amplifier suffers DC offset and noise in the signal paths; those effects can decrease the dynamic range of the input signal, unless using suitable conditioning circuits, so single-ended input structures are best employed when the signal source and amplifier are close one each other (*e.g.*, on the same PCB/chip, so that signal traces can be kept as short as possible).

Differential input amplifiers can offer a performance improvement because measure the difference between the "positive" and "negative" terminals of a sensor. Obviously, it is still possible to use the differential amplifier to measure single-ended signals by connecting one input terminal to analog ground (*e.g.*, typically the inverting one is preferred so to do not affect signal phase). Fully-differential inputs offer the best performance in rejecting DC and dynamic common-mode voltages. Moreover, another advantage in the use of differential signals is the capability to extend the amplifier dynamic range. In fact, because the two differential inputs can be also 180° phase shifted, differential inputs amplifier have two times the full-scale input voltage level, so they have a superior DC and AC common-mode rejection and a higher Signal-to-Noise Ratio (SNR). As drawback, in noisy environments, it is possible that coupled-noise could cause the differential inputs to exceed the amplifier allowable input voltage range (in this cases it is sufficient to reduce the input signal range to avoid the amplifier input stage saturation). However, it is important to select a fully-differential input amplifier when dynamic time-varying signals occur and dynamic common-mode rejection is mandatory.

In a floating differential system, ideally and supposing that the sensor and the next amplifier stage are isolated one each other, common-mode voltages beyond electrical supplies can exist, provided that the differential voltage does not exceed the amplifier maximum input range. One way to do it is to employ separate voltage supplies with galvanically isolated grounds. As long as isolation between the grounds exists, the amplifier block only detects the differential voltage between its differential inputs and the sensor can be regarded as floating. Thus, pseudo-differential inputs are similar to fully-differential inputs since they separate signal ground from the amplifier ground, allowing the reduction of only the DC common-mode voltages. However, unlike fully-differential inputs, they have a little effect on dynamic common-mode noise (they do not provide AC common-mode rejection). Pseudo-differential inputs are applied when biased (to an arbitrary DC level) sensors are employed.

Concerning integrated applications, the Current-Mode (CM) approach can be also considered as a possible alternative to traditional Voltage-Mode (VM) circuits to obtain high performance architectures, especially for LV LP applications, because the designer deals with current levels for circuit operation instead of voltage signals. In this manner, as well known, CM circuits, which are able to overcome the limitation of the constant Gain-Bandwidth (GBW) product and the trade-off between speed and bandwidth, typical of OA, provide others possible suitable choices. In particular, CM

topologies improve integrated circuit performances in terms of SR and Bandwidth (*BW*), through the development and the use of a suitable "*Second Generation Current Conveyors*" (CCII), which represent the main basic building active blocks in the CM design [22,23]. Typically, CCII-based circuit topologies have a low operating supply voltage, related to the drain-source (saturation) voltage required by the biasing transistors, which has to be minimised so to reduce the circuit total supply voltage. However, a basic well-known CM circuit is the Current-Feedback Operational Amplifier (CFOA). This circuit, if compared to the traditional voltage active block OA, shows a constant bandwidth with respect to the closed-loop gain. This makes it of primary importance in the design of modern *ICs*; in addition, the first stage of CFOA is exactly a Current Conveyor. The only commercially available CCII is the AD844 by Analog Devices which, even if it is a CFOA with very a high slew-rate and a wide bandwidth, is heavily utilized in discrete component prototype PCB implementations of CCII-based circuits, among which also sensor interface topologies. On the contrary, several CCII solutions presented in the literature are based on a differential pair followed by a class-AB output stage. This alternative approach can be also considered particularly useful to different GMR sensor-based applications which employ a current biasing instead of that, more traditionally, based on a voltage [7,9,11-14].

More in particular, the CCII is a three terminal active block that operates, simultaneously, as both voltage and current buffer between its terminals. Moreover, it has a low impedance (ideally zero) current input (*X* node, which is, at the same time, also a voltage output). On the contrary, the other voltage input terminal (*Y* node) shows a high impedance (ideally infinite), while the last terminal (*Z* node) shows also a high impedance level (ideally infinite) resulting an output current node. In this way, currents flowing at *X* and *Z* nodes are always equal in magnitude (the current flowing at *X* node is "conveyed" to the current output *Z* node), while if a voltage is applied to *Y* node, the same voltage will appear at *X* node. In particular, for what concerns the current direction, when the current at *Z* node goes in the same direction of that flowing in *X* node, we can refer to the *CCII+*; otherwise, in case of opposite current flow directions, one has to speak about the *CCII–*. Obviously, also for this active block, parasitic impedances are the main drawback that affects the CCII ideal behavior and, sometimes, its utilization in typical analog applications. Their kind and value mainly depend on the CCII internal topology, developed at transistor level. In fact, due to non-ideal behavior of CCII, the *X* node voltage not exactly equal that at *Y* node as well as the current flowing into *Z* terminal can be slightly different from that of the *X* node. Therefore, the two CCII parameters which represent the ideally-unitary voltage and current gains are α and β, respectively.

2 The Main Parameters of Sensor Electronic Interfaces

In the analysis and characterization of circuits and systems for signal conditioning coming from sensors, it is opportune to evaluate the performances given by the sensor and the interface also under different operating conditions [2-7].

In this sense, the following main parameters, typically referred to a sensor, have to be considered for evaluating performances and characteristics of a more complete front-end:

- ***Sensitivity*:** It is the variation of output electrical parameter with respect to the sensor variation, corresponding to a measurand variation. It represents the relationship (i.e., the transfer function) between the output electrical signal and the sensing element. An interface shows a high sensitivity when, for the same sensor variation, to be revealed, corresponds a larger variation of the generated electrical signal. Generally, sensitivity value depends on the operating point and on the electronic system setting.
- ***Resolution*:** Mathematically given by the ratio of the output noise level with respect to the interface sensitivity value, it is the minimum detectable measurand value that can be determined under the condition of unitary SNR, that is smallest variation of the sensor appreciable by the interface which provides a detectable output variation. Resolution is definitively the most important characteristic in sensor applications; numerically speaking, it must be minimized. A system with a very low resolution value is typically mentioned as a "high-resolution system". Sensitivity and resolution must be evaluated in the typical variation range of the sensor parameter where, possibly, have to be constant or linear; in this case their value does not depend on the operating point.

Moreover, other important interface parameters are the following:

- ***Linearity*:** Proportionality between input and output signals, concerning the interface response curve, which correlates the generated output signal with respect to the sensor parameter variations. For small sensor variation, linearity is always ensured.
- ***Repeatability*:** Capability to provide the same performances after repeated utilizations, when applied consecutively and under the same conditions.
- ***Accuracy*:** Agreement of the output values with a standard reference (*e.g.*, ideal characteristic, theoretical calculation, etc.). Accuracy is closely related to precision, also called reproducibility. As a consequence, accuracy is related typically to percentage relative error between ideal (or expected) and generated values, as shown in Figure 2.
- ***Precision*:** Capability to give output signals with similar values, for different and repeated measurements, when the same sensor value is applied (i.e., repeatability in the same measurement conditions).
- ***Reproducibility*:** Repeatability obtained under different measurement conditions (*e.g.*, in different times and/or places).
- ***Stability*:** Capability of a system to provide the same characteristics over a relatively long period of time (time-invariability).
- ***Drift*:** Slow and statistically unpredictable temporal variation of interface characteristics, related to electronic circuits, due to aging, operating temperature and/or other effects.
- ***Hysteresis*:** Difference among the output signal values, generated by the interface in correspondence of the same sensor variation range, achieved a first time for increasing values and a second time for decreasing values of the sensor parameter.

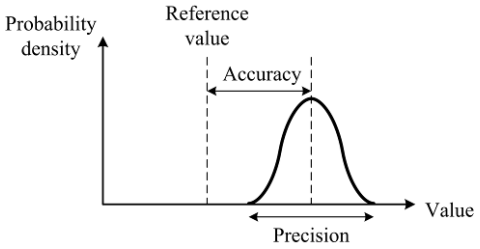

Fig. 2. Accuracy and precision definitions and their relationship

Furthermore, output signals coming from sensors, typically, have the following characteristics: low-level values, relatively slow sensing parameter variations and the need of initial calibration for long-term drift (it means they generally can be considered time-variant) and temperature dependence. For these reasons, in order reduce measuring errors, the design and the use of suitable low-noise low-offset analog electronic interfaces with low parasitic transistors and impedances, and compensation techniques (offset and *1/f* noise reduction by auto-zero circuits, chopper circuits and dynamic element matching) are essential [19-21,24,25]. In this sense, another important feature to be considered is the electrical impedance of the sensor, which determines also the frequency measurement range.

In the following we will present a review of the main resistive sensor analog interfaces, suitable both for the integration on chip in a standard CMOS technology, also with LV LP electronic characteristics, and, in particular, for GMR sensor applications. We have chosen to classify them according to the amount of resistive variations and/or values, and then, considering the kind of sensor excitation (DC, AC), describing both Voltage-Mode and Current-Mode solutions [3].

3 Small Range Resistive Sensor Interfaces

DC Excited Sensor Interface Solutions

Voltage Divider and Wheatstone Bridges: When the resistive sensing element varies into a reduced range (about one-two decades, or less), a simple resistive voltage divider circuit, operating an *R-V* conversion, can be utilized as first and simple analog interface [3,19]. More in detail, considering Figure 3 and, as an example, if a DC supply voltage V_{IN} is applied to drive the sensing element R_{SENS} and utilizing a reference load resistance R_{REF}, the output voltage V_{OUT} can be revealed and processed instantaneously, so to determine the sensor resistance value.

As a consequence, from the voltage divider, changes of the sensor resistance R_{SENS} can be evaluated, once R_{REF} and V_{IN} are known, by measuring the circuit output voltage V_{OUT}, as follows:

$$V_{OUT} = \left(\frac{R_{SENS}}{R_{REF} + R_{SENS}} \right) V_{IN}, \tag{1}$$

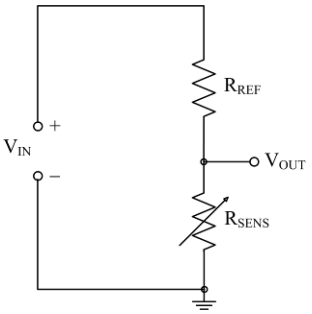

Fig. 3. The voltage divider as resistive sensor interface circuit (V_{IN} = circuit excitation voltage; R_{REF} = reference load resistance; V_{OUT} = circuit output voltage; R_{SENS} = sensing element)

from which:

$$R_{SENS} = R_{REF}\left(\frac{V_{OUT}}{V_{IN} - V_{OUT}}\right). \tag{2}$$

The fully differential version of the voltage divider (for what concerns the output voltage) is the well-known Wheatstone bridge, whose schematic circuit is shown in Figure 4, which still operates an *R-V* conversion, better rejecting the common-mode signal. In particular, it can be used for converting low sensor resistance variations into a differential voltage signal V_{OUT}. It is composed by four resistances and, usually, a resistive sensor is placed into one of the four branches of the bridge whose resistive sensing element varies when an external physical or chemical phenomenon occurs.

Referring to Figure 4, the bridge is balanced when the ratio of resistances of a bridge branch is equal to that of the other: $R_1/R_2=R_3/R_{SENS}$. As a particular case, the bridge is balanced when all the four resistances are the same value: $R_1=R_2=R_3=R_{SENS}$. In this case, the generated differential output voltage V_{OUT} is equal to zero.

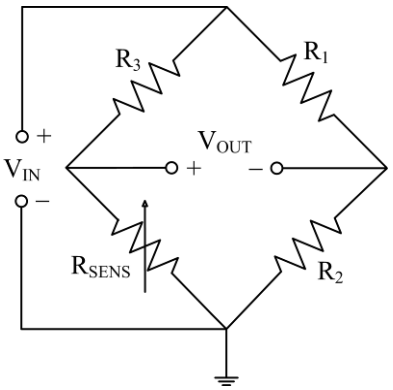

Fig. 4. The Wheatstone bridge as a resistive sensor interface: the *R-V* conversion

On the contrary, starting from equilibrium condition (balanced bridge), when R_{SENS} varies its resistance, a non-zero differential voltage V_{OUT} is provided at the output of the bridge, whose value is proportional to the sensor resistance variation (but only when these variations are small, in particular, referring to Figure 4, if $x<<1$, supposing $R_{SENS}=R_{S0}(1+x)$, being R_0 the baseline sensor value). More in general, the output voltage can be expressed as follows:

$$V_{OUT} = \left[\frac{R_1 R_{SENS} - R_2 R_3}{(R_1 + R_2)(R_3 + R_{SENS})} \right] V_{IN}, \tag{3}$$

from which:

$$R_{SENS} = \frac{R_2 R_3}{R_1} \left[\frac{1 + \frac{V_{OUT}}{V_{IN}} \left(\frac{R_1 + R_2}{R_2} \right)}{1 - \frac{V_{OUT}}{V_{IN}} \left(\frac{R_1 + R_2}{R_1} \right)} \right]. \tag{4}$$

Unfortunately, this kind of resistive sensor interface shows a low and unsettable sensitivity value; in particular, it can be expressed as:

$$S_{R_{SENS}} = \frac{\partial V_{OUT}}{\partial R_{SENS}} = V_{IN} \frac{R_3}{(R_3 + R_{SENS})^2} \tag{5}$$

If $R_1=R_2=R_3=R_{SENS}$, in the basic Wheatstone bridge, the sensitivity is constant and equal to $V_{IN}/4$ considering a small variation of only one bridge resistance (R_{SENS}). This value of the sensitivity is exactly the same of the simple voltage divider (see Figure 3). In fact, in the both cases, if the relative variation of the sensor resistance ($x=R_{SENS}/R_0$) is reasonably small (*e.g.*, lower than 5% with respect to the sensor resistance baseline R_0), a quasi-linear relation between the differential output voltage V_{OUT} and the relative variation x exists, as follows:

$$V_{OUT} = V_{IN} \frac{x}{4 + 2x} \cong V_{IN} \frac{x}{4}. \tag{6}$$

Alternatively, referring to Figure 5, through a suitable null detector (*e.g.*, a simple multimeter or voltmeter), which reveals the balanced condition of the bridge (that is, the output voltage equal to zero), by changing the value of a variable resistor R_{VAR} (one of the resistors in the branch), it is possible to determine the unknown resistance value provided by the resistive sensor R_{SENS}, that changes as a function of an external (physical or chemical) phenomenon to be detected and measured.

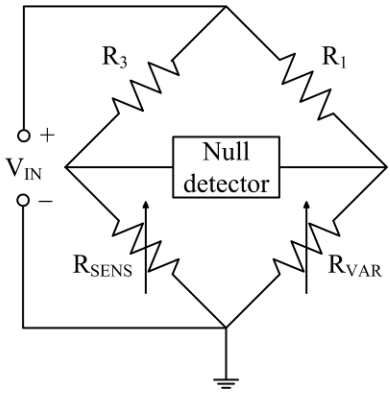

Fig. 5. The null detector in a resistive Wheatstone bridge

The use of a differential input OA-based voltage amplifier, as reported in Figure 6, allows to enhance the front-end circuit sensitivity. This VM circuit, performing also the single-ended conversion, can be placed at the output nodes of the bridge.

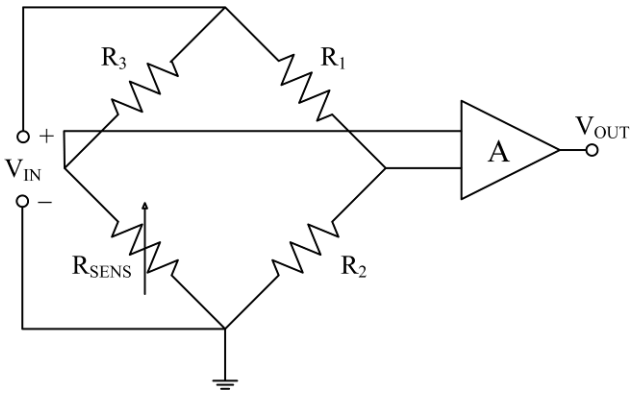

Fig. 6. Differential-to-single ended Wheatstone bridge output by using a voltage differential amplifier

In this case, an instrumentation differential amplifier is the best circuit topology since shows a very high input impedance and, through its internal feedback configuration, gives a well-defined and controlled amplification factor. Another fundamental characteristic of this amplifier must be its low input voltage offset. If A is the OA gain and supposing $R_1=R_2=R_3=R_{SENS}$, we can write, for low-resistive variations (x):

$$V_{OUT} \cong A\left(V_{IN}\frac{x}{4}\right). \tag{7}$$

Current-Biased Solution: A basic interface for resistive sensor, utilizing a current biasing, is shown in Figure 7 [3]. This solution is based on a Resistance-to-Current (*R-I*) conversion, allows to generate an output current I_{OUT} dependent on the sensor resistance value R_{SENS}.

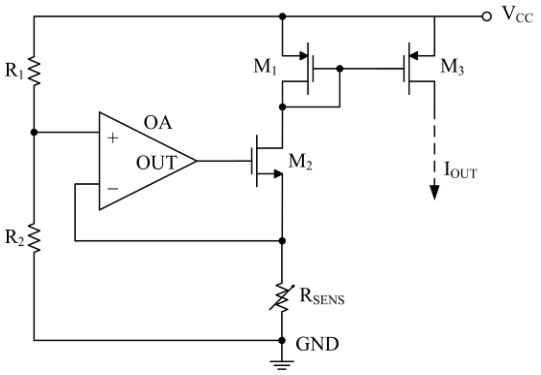

Fig. 7. Resistance-to-Current converter as a resistive sensor interface

Through a simple analysis it is possible to evaluate ideally the generated current, as follows:

$$I_{OUT} \cong V_{CC} \frac{R_2}{R_1 + R_2} \frac{1}{R_{SENS}}, \tag{8}$$

assuming that M_1 and M_3 are matched and equal *p-MOS* transistors. Obviously, the output current I_{OUT}, if required, can be also further converted into a voltage output signal through an additional Current-to-Voltage (*I-V*) conversion.

Current-Mode Resistive Sensor Interface: Figure 8 shows a CCII-based analog interface suitable for DC-excited resistive sensor applications. The advantage of this CM circuit in the sensor interfacing is its capability to perform the offset compensation, in this way the output voltage is linearly proportional to the resistive variation [26]. The only feature to be considered is the design of *CCIIs* having negligible parasitic impedances (see a quasi-ideal configuration reported in Figure 23). In particular, also in this case, it is assumed that the sensor is modelled by the resistance $R_{SENS}=R_0(1+x)$, being R_0 the resistance value referred to the sensor baseline value and x the relative sensor variation.

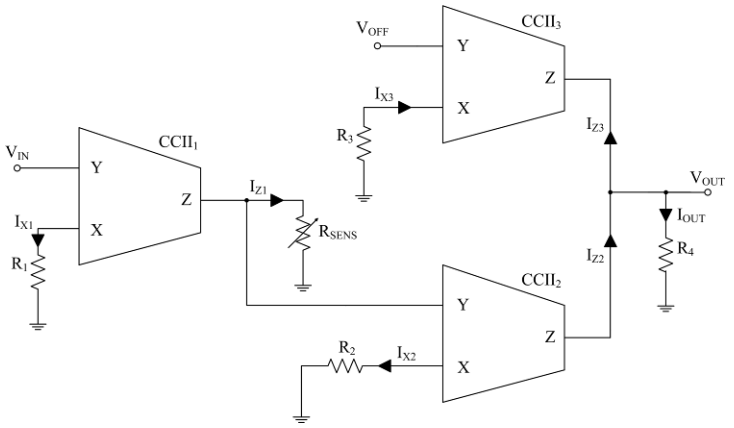

Fig. 8. CCII-based electronic interface for resistive sensors

A straightforward analysis gives the following expression of V_{OUT}:

$$V_{OUT} = \left(\frac{R_4 R_0 V_{IN}}{R_1 R_2} \right) x + \left(\frac{R_4 R_0 V_{IN}}{R_1 R_2} - \frac{R_4 V_{OFF}}{R_3} \right). \tag{9}$$

The first term is linearly proportional to the relative variation x of the sensor resistance, while the second one can be set to zero by a suitable choice of V_{IN}, V_{OFF}, R_1, R_2, R_3 and R_4, so cancelling the voltage offset without reducing the speed of the interface, even if, in this way, time-varying errors, such as drift and *1/f* noise, might not be compensated.

AC Excited Sensor Interface Solutions

Current-Mode Uncalibrated Solution for High-Valued Resistive Sensors: A CM interface for AC-excited high-valued resistive sensors, performing a current differentiation rather than a voltage integration as in typical oscillators, is shown in Figure 9 [27]. In particular, this solution, based on an oscillating circuit (*R-T* conversion), allows to neglect the *Z* and *Y* nodes saturation effects in the square waveform generation. Moreover, it is possible to easily set the interface working range through several passive components which allow also to set the desired sensitivity of the readout circuit. As a consequence, this circuit configuration, which can be employed as a suitable solution for small-range resistive sensor analog front-ends, allows to reveal, with a good accuracy, variations of grounded resistive sensors typically ranging in [MΩ÷GΩ], even if the same circuit is also suitable for wide-range floating capacitive sensors [pF÷μF].

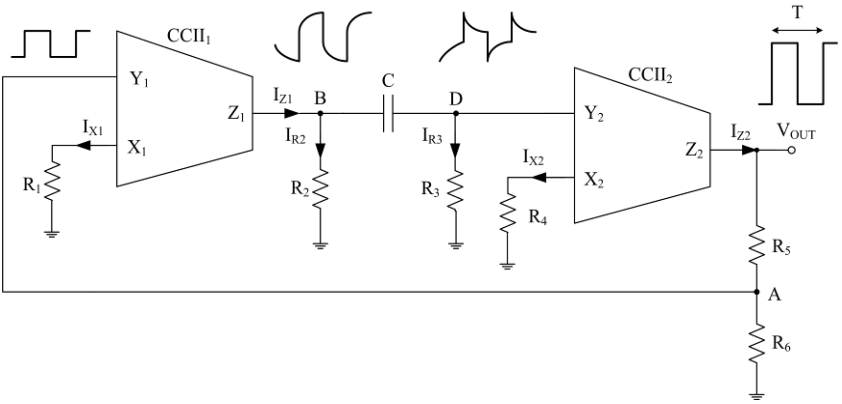

Fig. 9. Block scheme of a CCII-based AC-excited interface

Through a straightforward analysis, considering an ideal CCII behaviour, it is possible to determine the expression for the period T of the generated output square wave signal, revealed at V_{OUT} node, as a function of the sensor resistance (*e.g.*, R_2 or R_3), as follows:

$$T = 2C(R_2 + R_3)\ln\left[\frac{2R_2R_3R_6 - R_1R_4(R_2 + R_3)}{R_1R_4(R_2 + R_3)}\right]. \tag{10}$$

OA–Based Uncalibrated Solution: In Figure 10 we present a square-wave oscillator, based on OA, performing an *R-T* conversion, also in this case based on a voltage differentiation, so ensuring a good immunity to low-frequency disturbs [28].

In the circuit, OA_1 serves as a voltage differentiator, while OA_2 is a hysteresis voltage comparator. Thanks to a suitable closed loop, which avoids any system calibration, resistive sensors can be excited by an AC signal. The block scheme of the circuit shows also the voltage signals at the main circuit nodes, from which the differentiating effect on V_C can be seen.

Through a straightforward circuit analysis, considering ideal OAs, it is possible to achieve the following expression for the period T of the generated square waveform, revealed at V_{OUT} node:

$$T = 2CR_5\ln\left(\frac{\dfrac{R_5}{R_6}\left(\dfrac{R_3}{R_3 + R_4} - \dfrac{R_1}{R_1 + R_2}\right) - 2\dfrac{R_4}{R_3 + R_4}}{\dfrac{R_5}{R_6}\left(\dfrac{R_3}{R_3 + R_4} - \dfrac{R_1}{R_1 + R_2}\right)}\right). \tag{11}$$

From eq.(11) it is evident the direct proportionality between the output period and capacitance *C* (useful for capacitance estimation and/or for the sensitivity setting) but, under particular conditions about the resistance values, it is possible to consider R_5 as a resistive sensor achieving a good linear response for a reduced variation range.

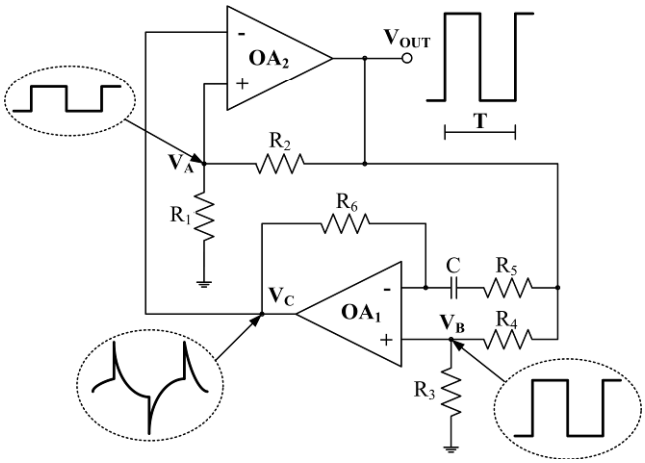

Fig. 10. Block scheme of the proposed capacitive/resistive sensor interface

4 Wide Range Resistive Sensor Interfaces

DC Excited Sensor Interface Solutions

Automatic Uncalibrated Wheatstone Bridges: The Wheatstone bridge configuration can be made "automatic" (so that the circuit does not need initial calibration) through the development of the topology shown in Figure 11 which employs a tuneable resistor implemented through a voltage controlled resistance, based on a novel use of an analog four quadrant multiplier [29], whose variations follow those of the resistive sensor, and a suitable feedback loop.

More in detail, the circuit reported in Figure 11 represents the configuration suitable for a grounded resistive sensor placed in the lower position of the left branch of the bridge. The differential bridge output is connected to an OA-based differential amplifier with a voltage gain *A*; then, the single-ended output is sent to a voltage inverting integrator whose aim is both to create the stable negative feedback loop and to provide the correct control voltage value (V_{CTRL}) for the tuneable resistor R_{VCR}.

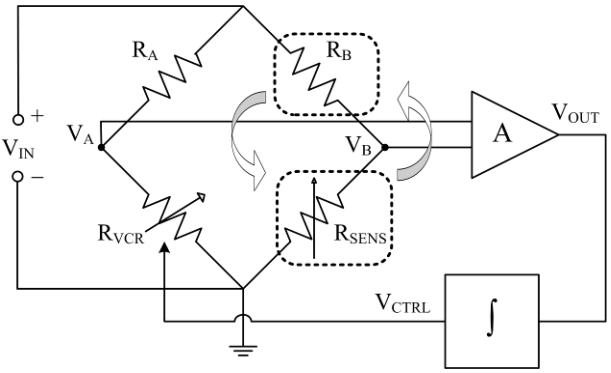

Fig. 11. Block schemes of the proposed bridge-based interfaces (according to the position of the two right branch elements, it is possible to study the "Grounded" and "Floating" sensor configuration)

If a measurand variation occurs into a determined range, the unbalanced output voltage is amplified and the integrator produces a ramp that tunes the active element R_{VCR} until a new equilibrium condition is reached (i.e., the automatic range). The complete expressions for the estimation of the sensor resistance R_{SENS}, as a function of the other three bridge resistances (R_A, R_B and R_{VCR}), the supply voltage V_{CC} and the bridge differential output voltage $\Delta V = V_A - V_B$, is given by:

$$R_{SENS_{GROUNDED}} = \frac{R_{VCR} R_B}{R_A} \cdot \left(\frac{1 - \frac{\Delta V}{V_{CC}} \frac{R_A + R_{VCR}}{R_{VCR}}}{1 + \frac{\Delta V}{V_{CC}} \frac{R_A + R_{VCR}}{R_A}} \right). \tag{12}$$

Similar results can be obtained with another configuration of the automatic bridge, obtained by swapping the two dashed elements in Figure 11, achieving a solution suitable for a floating resistive sensor. In this case, the resistive sensor estimation can be performed through the following equation:

$$R_{SENS_{FLOATING}} = \frac{R_A R_B}{R_{VCR}} \cdot \left(\frac{1 + \frac{\Delta V}{V_{CC}} \frac{R_A + R_{VCR}}{R_A}}{1 - \frac{\Delta V}{V_{CC}} \frac{R_A + R_{VCR}}{R_{VCR}}} \right). \tag{13}$$

This modification maintains the same working principle, but the effect of the variable floating sensor implies an opposite trend, with respect to the first configuration, of the control voltage signal V_{CTRL}, as depicted in Figure 12 where the behaviours of V_{CTRL} and ΔV voltages, for both the configurations, vs. R_{SENS}, have been reported. Due to the electrical limits of the considered analog multiplier inputs, the circuit is not able to

follow any bridge unbalancing out of the automatic range, where the control voltage V_{CTRL} reaches the saturation level. However, since the differential output ΔV is not zero and, through eq.s (12) and (13), it is possible to estimate resistive sensor values for more than 5 decades (in a settable range) in a very fast way by only reading the two voltages V_{CTRL} and ΔV.

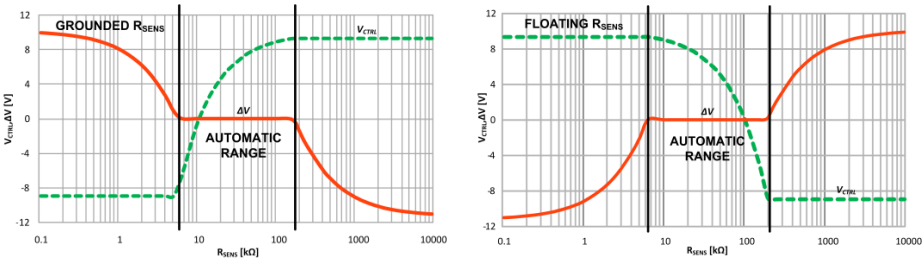

Fig. 12. ΔV and V_{CTRL} vs. sample resistance for "grounded" (left) and "floating" (right) configurations

Voltage-Mode Uncalibrated Solution: In Figure 13 an OA-based interface, performing an *R-T* conversion, is presented. This circuit, based on an oscillator topology and exciting the sensor with a DC voltage V_{EXC}, is able to reveal more than 4 decades of high resistance variations (*e.g.*, 1MΩ÷10GΩ) [30]. It employs three OAs and four switches in order to properly control the voltage signal V_1 generated by the first stage, dependent on the sensor resistance value R_{SENS}, while OA_2 operates both as an inverting integrator and as a non-inverting one, through the suitable use of the four switches.

Considering an ideal behaviour for the OAs, through a straightforward analysis, it is possible to evaluate the relationship between the sensor resistance R_{SENS} and the period T of the output square wave signal, as follows:

$$T = 2R_2C_1\left[\left(\frac{R_4}{R_3+R_4}\frac{V_{SAT+}-V_{SAT-}}{R_1V_{EXC}}\right)R_{SENS}-1\right], \tag{14}$$

being V_{SAT+} and V_{SAT-} the OA saturation voltages.

Since the voltage integrator has a double operating function, the presence of the capacitance C_1 involves a charge effect, which influences instantaneously the ramp signal when there is the operating function commutation (from inverting to non-inverting and vice versa), through a vertical edge on V_A, as also depicted in Figure 13, whose value depends on the V_1 level, thus on R_{SENS} (low values of sensor resistance provide a high voltage gap).

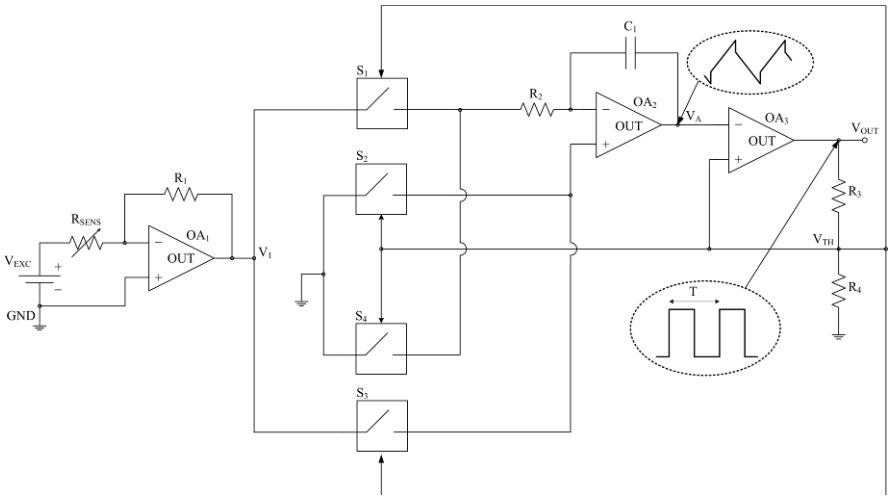

Fig. 13. The proposed OA-based interface with a DC resistive sensor excitation voltage

Current-Mode Uncalibrated Solution: In Figure 14, a similar solution, developed with the CM approach, based on an oscillating circuit, always suitable for resistive sensing elements which do not tolerate an AC excitation voltage, is reported. This interface does not require any preliminary calibration and operates, once again, an *R-T* conversion [31].

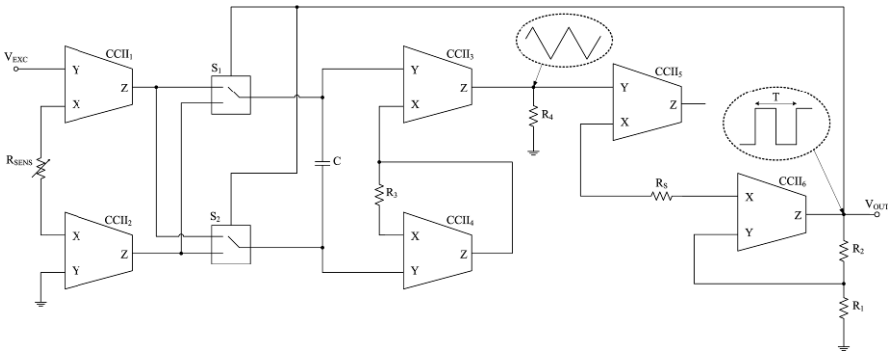

Fig. 14. Scheme of the proposed CCII-based front-end

Through a straightforward analysis, considering ideal *CCIIs* and switch behaviours, it is possible to determine the expression for the period *T* of the generated output square wave signal as a function of the sensor resistance R_{SENS} as follows:

$$T = 2R_{SENS}C\left[\frac{k\left(V_{SAT+} - V_{SAT-}\right)}{A \cdot V_{EXC}}\right], \tag{15}$$

where $k = (R_1 - R_S)/(R_1 + R_2)$, A is the voltage gain of instrumentation amplifier ($A = 2R_4/R_3$), V_{EXC} is the DC sensor excitation voltage, while V_{SAT+} and V_{SAT-} are the positive and negative saturation voltages at output terminal V_{OUT}.

AC Excited Sensor Interface Solutions

OA-Based Astable Multivibrator: Generally, when large variations of sensor resistive values occur, the most used strategy is related to an AC-excitation voltage for a (floating) resistive sensor, operating the *R-T* conversion.

The simpler electronic interface which converts a pure resistive variation into a period (or a frequency) can be implemented by an OA in astable multivibrator configuration, as shown in Figure 15 [3,19]. This circuit solution implements a square wave generator, whose output voltage signal period is linearly dependent on the sensor resistance value. Obviously, the same topology is certainly suitable also as a capacitive sensor interface.

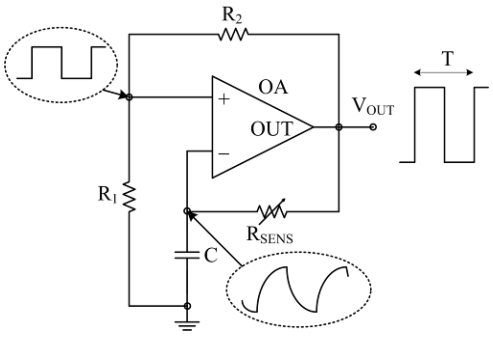

Fig. 15. OA-based astable multivibrator circuit as resistive sensor interface

Through a straightforward circuit analysis, it is possible to evaluate the output period T of the generated square waveform V_{OUT}, dependent on R_{SENS}, according to the following equation:

$$T = 2R_{SENS}C\ln\left(\frac{1+\beta}{1-\beta}\right), \tag{16}$$

being:

$$\beta = \frac{R_1}{R_1 + R_2}. \tag{17}$$

Eq. (16) is valid only for an ideal OA and, more in detail, if we consider $R_1=R_2$, it simply becomes $T \approx 2.2R_{SENS}C$. However, considering ideal conditions, the circuit has no limitations for high period values (except for the fact that a long measurement time occurs), so it is able to operate, for an example, at least for 6 decades of resistance variations, which correspond to a period span of the same number of decades. The sensitivity, for this kind of resistive sensor interface, is relatively low and, consequently, the main problem related to this front-end concerns the detection of small resistance values or variations. In addition, it is also important to employ accurate values of R_1 and R_2 resistances and non-linear effects (among which the temperature) have to be taken into account and verified so to be eventually considered both in the period measurement and, consequently, in the sensor resistance estimation.

CCII-Based Astable Multivibrator: A CM version of the astable multivibrator, implemented with a single CCII, performing a square wave generation, is reported in Figure 16 [32]. This solution can be used in resistive sensor interfacing, showing a linear relation, between sensor and oscillation period, in an operating frequency range up to about 50MHz.

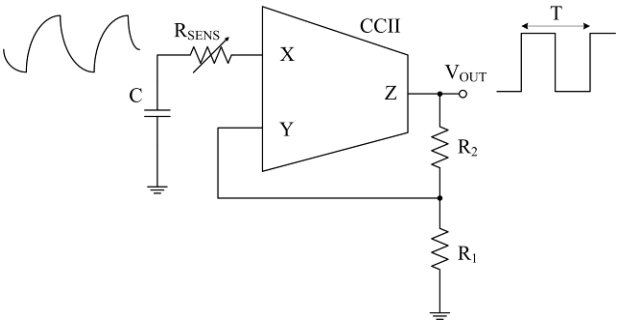

Fig. 16. CCII-based astable multivibrator

The output square-wave signal period is ideally given by:

$$T = R_{SENS}C\ln\left(\frac{V_{TH-}-V_{X+}}{V_{TH+}-V_{X+}}\cdot\frac{V_{TH+}-V_{X-}}{V_{TH-}-V_{X-}}\right) \tag{18}$$

being:

$$V_{TH+} = \frac{R_1 - R_{SENS}}{R_1 + R_2}V_{SAT+};\quad V_{TH-} = \frac{R_1 - R_{SENS}}{R_1 + R_2}V_{SAT-}, \tag{19}$$

$$V_{X+} = \frac{R_1}{R_1 + R_2}V_{SAT+};\quad V_{X-} = \frac{R_1}{R_1 + R_2}V_{SAT-}, \tag{20}$$

where V_{SAT+} and V_{SAT-} are the saturation voltages that the CCII is able to reach at its output. Therefore, the period T can be varied by changing R_{SENS}; in this sense, the CCII internal series parasitic resistance at X node must be carefully considered.

CCII-Based Uncalibrated Solution: A CM interface circuit, for AC-excited sensors showing a wide resistive variation is reported in Figure 17 [33]. It is composed by: a voltage integrator ($CCII_1$), a voltage buffer ($CCII_2$) and a CM hysteresis comparator ($CCII_3$). Through a straightforward analysis, considering ideal CCII behaviour, it is possible to determine the expression for the period T of generated output square wave signal, revealed at V_{OUT} node, as a function of the sensor resistance R_{SENS}, as follows:

$$T = 4R_{SENS}CG, \tag{21}$$

being:

$$G = \frac{R_2 - R_1}{R_2 + R_3}. \tag{22}$$

From eq.s (21) and (22), the circuit sensitivity can be opportunely set by choosing C, R_1, R_2 and R_3 values.

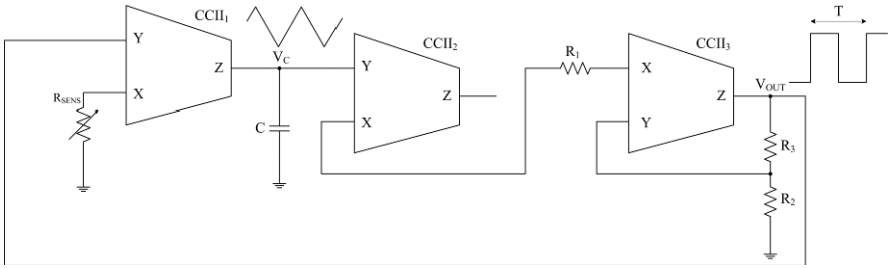

Fig. 17. Block scheme of the proposed uncalibrated CCII-based interface

OA-Based Uncalibrated Solution: Starting from the OA-based astable multivibrator circuit, Figure 18 shows the block scheme and related main node voltage behaviours of an improved VM wide range resistive sensor interface, always based on an oscillator topology, formed by: an inverting amplifier (AMP), a voltage comparator (COMP) and an inverting integrator (INT). This circuit, able to reveal about over 6 decades of sensor resistance variations (*e.g.*, kΩ÷GΩ) without any initial calibration, performs an *R-T* conversion, where the oscillation period T of the generated output square wave signal V_{OUT} is directly proportional to sensor resistance value R_{SENS} [34].

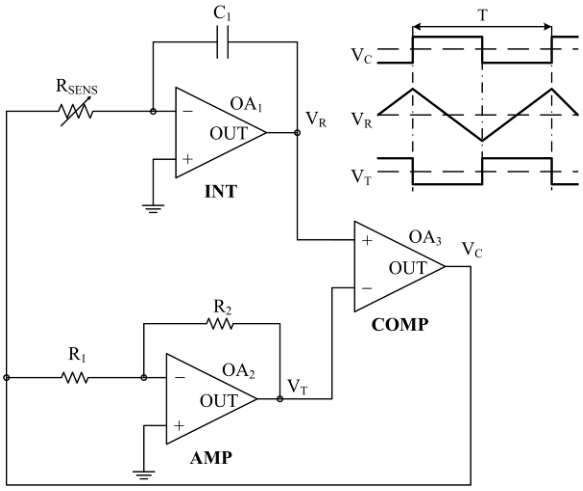

Fig. 18. Block scheme of the resistive sensor interface based on an *R-T* conversion and voltage behaviours at its main nodes

In this case, the ideal relationship between the period T and the sensor resistance R_{SENS} is the following:

$$T = 4GC_1R_{SENS} \tag{23}$$

being G the ratio between R_2 and R_1, typically lower than 1. From eq. (23), it comes that the proposed interface shows two degrees of freedom, in particular C_1 and G (i.e., R_1 and R_2), that helps to choose its sensitivity and so the oscillation frequency range.

OA-Based Time-Controlled Oscillating Uncalibrated Solution: Possible evolutions of previous schemes go towards a main direction: the development of solutions showing a reduced measurement time for high resistive sensor values; some of the latter will be shown in the following.

A suitable interface circuit, capable to overcome the main limit of the solutions based on the *R-T* conversion (i.e., the long measuring time occurring in the evaluation of high-value sensor resistances), is reported in Figure 19. This solution, always performing an *R-T* conversion, is based on a particular oscillating circuit architecture which operates a suitable "compression" of the higher part of the resistive wide range, thus limiting the measuring time, by means of an "ad-hoc" oscillator architecture utilizing suitable feedbacks [35]. This solution provides always an AC excitation voltage for the sensor and results capable to estimate its resistance over a wide range (about 5 decades, *e.g.*, 100kΩ÷10GΩ) with a maximum measuring time lower than hundreds of ms (settable values).

More in detail, referring to Figures 19 and 20, INT_1 is an inverting integrator which generates the sensor ramp V_R, INT_2 is a non-inverting integrator providing the ramp threshold V_Z, COMP is a hysteresis comparator; this last block detects the intersections between the ramp threshold V_Z and the sensor ramp V_R, generating a

square-wave signals V_Y. Moreover, V_Y is the main signal which is also employed both to close the circuit loop and to provide the AC sensor excitation voltage (i.e., $\pm V_{CC}$), so performing the oscillating behaviour. Therefore, the output period T, calculated as T_1+T_2, depends on both V_Z (independent from R_{SENS}) and V_X (related to V_R and therefore to R_{SENS}). On the other hands, the measuring time T of the sensor interface is properly regulated by means of both the ramp threshold slope (i.e., the "fixed" time constant of the non-inverting integrator) and the sensor ramp slope (i.e., the "variable" time constant of the inverting integrator depending on sensor resistance value).

Thus, if R_{SENS} is very high, V_R and V_X are almost constant, but the oscillator output period is limited by the presence of the threshold voltage V_Z that, since it is a ramp signal having an opposite slope with respect to both V_R and V_X, "moves" towards the sensor ramp V_R. As a consequence, for very high R_{SENS} values, the output period maximum value is always limited by the ramp threshold V_Z to a finite value, through the implemented "time-compression". On the contrary, for low R_{SENS} values, V_R and V_X show very fast ramps (i.e., having a high slope) when compared to the threshold voltage V_Z which is, in this case, "approximately" constant, since it is a ramp signal with reduced slope.

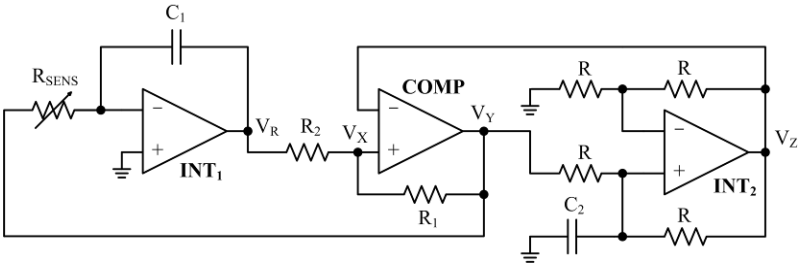

Fig. 19. Electronic implementation of the time-controlled oscillating circuit

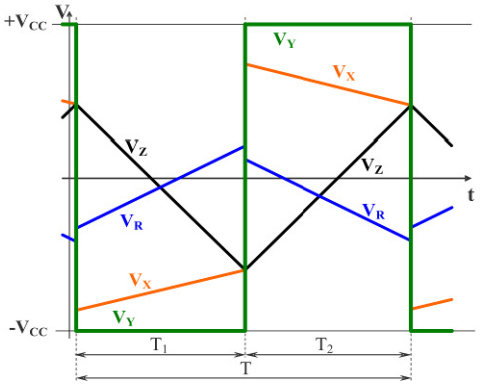

Fig. 20. Typical timing diagram of the voltage signals revealed at the main terminals of the interface solution shown in Figure 19

In this way, the R_{SENS} estimation is performed by measuring the period T of the output V_Y of the comparator COMP, according to the following ideal relationship:

$$T = \frac{4B}{\frac{(1-B)}{R_{SENS}C_1} + \frac{2}{RC_2}}, \tag{24}$$

being $B = R_2/(R_1+R_2)$. Moreover, in this case, the oscillating circuit sensitivity, expressed as $\delta T/\delta R_{SENS}$, shows a quasi-constant value for small resistances, while for high resistor values it decreases for the effect of the "time-compression" of T with respect to R_{SENS}, as shown in Figure 21.

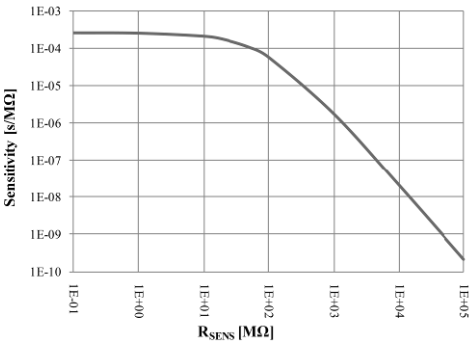

Fig. 21. Example of the time controlled sensitivity response vs. sensor resistance value

5 Integrated Microsystems

Introduction and Basic Main Concepts

The recent evolution in the Very Large Scale Integration (VLSI) industry contributing to the rapid technology changes and leading to an improved interest in analog circuit design (especially for what concerns *ICs*), the tremendous competition among vendors and the demand in the market for *ICs*, represent all together the factors which have led to consider the time-to-market factor with utmost importance. Regarding the electronic/sensor systems, with maximum performance and least turnaround time, an *ASIC* seems to be the best option to meet the ever growing demands for quality chips.

In particular, a huge design effort has been put toward the placement of a larger number of elements and devices on a single chip, together with supply voltage and power dissipation reductions, as much as possible. The suitable analog integrated circuit design, widely utilized in portable single-cell battery operated applications (*e.g.*, biomedicals, cellular phones, etc.), has led to implement new design microelectronic strategies, to be developed in low cost standard CMOS integrated technologies, even if analog blocks, as voltage/current amplifiers, must be carefully designed in

integrated sensors interface applications since these processes show transistors with high input offset voltages and a not negligible low-frequency noise levels.

In this sense, as regard integrated microelectronics, the continuous reduction of the threshold voltage in standard CMOS has definitively directed LV design towards CMOS itself, which is also typically characterized by a very low quiescent power consumption. Reducing the supply voltage, CMOS transistor is often biased to work in weak inversion region. In addition, a suitable interfacing of the sensitive element with a proper *ICs* is fundamental, especially when they are fabricated on the same chip. In this sense, CMOS technology is widely used, because it allows to match the reduction of costs of the silicon with the possibility of designing new LV LP interface circuits to be easily dedicated to the portable sensor applications market [21-23,36].

Moreover, referring particularly to the AMS 0.35μm standard CMOS technology, also the passive components have to be taken into account and properly designed. In this sense, in fact, note that there are several problems, especially related to the required silicon area. Therefore, sometimes, analog electronic designers have to evaluate the limitations related to resistors and capacitors integrations. Detailing, an *R-poly* resistance requires 7Ω/□ (i.e., square resistance) and a *Poly-Sub Plate* capacitance needs 0.12fF/μm^2; on the contrary, typical areas requested by an active block, such as *OTA* and CCII, are lower than 0.1mm^2 (*e.g.*, see next Sections).

However, concerning the analog circuit design, the reduction of the supply voltage does not necessarily correspond to a decrease of related power consumption. Therefore, in order to reduce the power dissipation, analog circuits have to be designed as much simple as possible. Moreover, it is important to consider that a trivial decrease of biasing currents, which can reduce circuit dissipation, degrades the circuit performance, first of all bandwidth and dynamic range. As a consequence, chip area cannot be drastically reduced with the lowered feature dimensions. As a result, LP design is characterised by an efficient use of the supply current (*e.g.*, through the utilisation of class-AB output stages) and an efficient frequency compensation strategy.

Finally, for example, referring to GMR sensor integrated technologies, it is important to consider that high density arrays have been integrated and fabricated on a single chip, in a standard CMOS process and with a very small silicon area (*e.g.*, lower than 1mm^2), for different applications, especially in biomedical fields (*e.g.*, *DNA* hybridization detection) [8,9,15,16]. In fact, integrating GMR resistive sensor arrays and signal conditioning electronics on a single silicon-based chip, fabricated in standard CMOS technologies, yield low-cost complete microsystems (System-on-Chip, *SoC*) that constitutes a promising tool for the future of portable applications. This kind of GMR-based CMOS integrated solutions, compared for example to complex and expensive optical detection approaches or imaging systems, measures electrical signal directly from the sensor and makes a low-cost, highly portable device feasible, especially for applications such as fuel cells monitoring, current sensing in power electronic modules, *ICs* current monitoring and power measurements, etc. [7,10-14,17,37-39].

OTA and CCII CMOS Transistor-Level Solutions

Generally, in microelectronic systems, the active block used as OA is implemented by a suitable *OTA*. A possible *OTA* internal topology, designed at transistor level in a standard CMOS technology, is reported in Figure 22 [3,34].

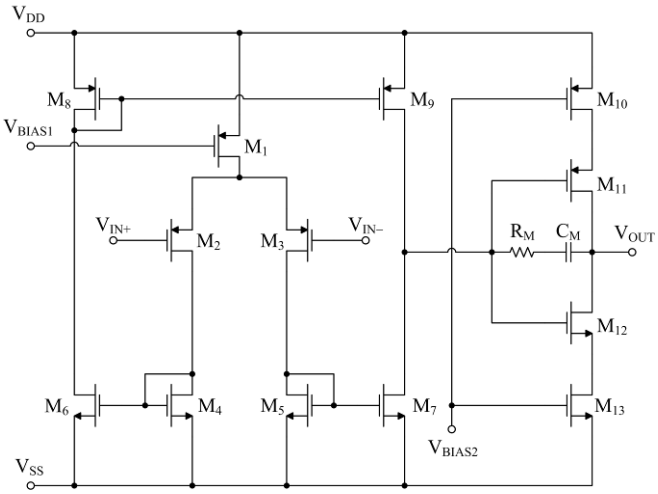

Fig. 22. OTA schematic at transistor level

More in detail, the *OTA* shown in Figure 22 is composed by two stages: the input stage (formed by transistors M_1–M_9), which is a symmetrical *OTA*, and the output stage (formed by transistors M_{10}–M_{13}), that is an AB-class inverter amplifier, based on a push–pull configuration (M_{11},M_{12}), that allows to obtain a full dynamic output range, with a source degeneration (M_{10},M_{13}). In particular, transistors M_{10} and M_{13} allow a better control of the current flowing in the output branch, even if, through the source degeneration, this same current has been done slightly dependent on supply voltage variations. Moreover, this second stage allows to get a high open loop voltage gain, so to make the amplifier more ideal. Frequency stability has been obtained by an *R-C* series Miller compensation (i.e., R_M and C_M components, Figure 22). The choice of a symmetrical configuration as *OTA* input stage and a careful layout implementation have allowed to reduce both the systematic and the random input offset voltages. Furthermore, two *p-MOS* matched transistors, M_2 and M_3, have been utilized as input differential pairs so to have a low input equivalent noise.

This schematic has been developed so to obtain better performances, in terms of very high *SR* and very low input voltage offset, and to operate at reduced supply voltage with low power consumption, as detailed in Table 1. In this sense, it can be employed so to develop suitable integrated versions of previous described VM sensor interface solutions. Moreover, in this way, especially referring to those solutions based on oscillating circuits, the relative error between ideal/theoretical and measured oscillation periods becomes negligible.

Table 1. Main characteristics of the implemented *OTA*, designed in AMS 0.35μm standard CMOS technology

***OTA* parameter**	**Post-layout simulated value**
Voltage supply	3.3 V
Power dissipation	992 μW
GBW	65.8 MHz
Output dynamic range	Full
Open Loop DC Voltage Gain	66 dB
Slew-Rate	40 V/μs
Input voltage offset	100 μV
Input equivalent noise	169 nV/√(Hz) @ 1 kHz
Silicon area	0.05mm^2

At least, in this paragraph, we will show also a possible transistor level integrated solution of a CCII [26], developed in AMS 0.35μm standard CMOS technology. It can be employed so to develop suitable integrated versions of previous described CM sensor interface solutions [3]. This CCII internal topology, reported in Figure 23, shows negligible parasitic impedances and unitary voltage and current gains for a very large bandwidth (quasi-ideal characteristics), as detailed in Table 2.

More in detail, the circuit shown in Figure 23 is formed by a differential input stage (M_1–M_7; R_3), an AB-class output stage (M_8–M_{11}; R_1,R_2; M_{16}–M_{17}) and a LV cascode Wilson current mirror (M_{12}–M_{15}; M_{18}–M_{21}). The AB-class output stage allows to decrease the *X* parasitic impedance, whereas the cascode current mirror increases the *Z* impedance.

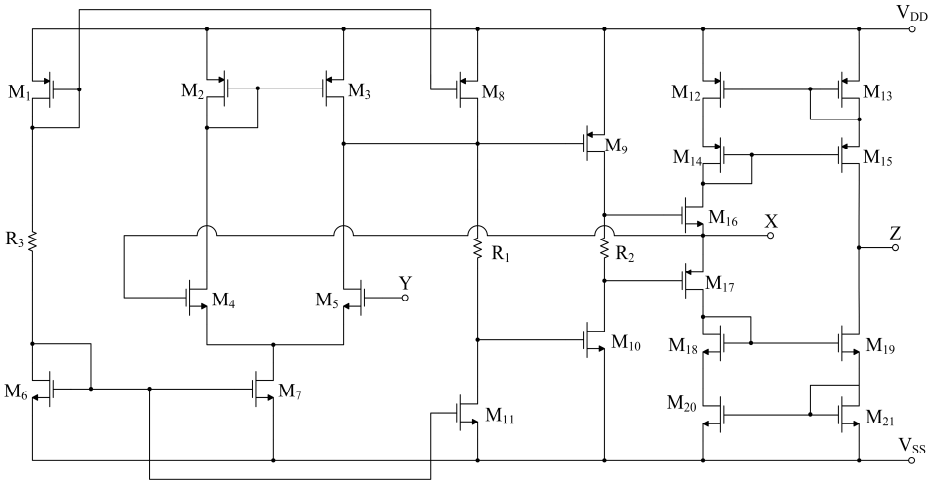

Fig. 23. Quasi-ideal CCII schematic at transistor level

Table 2. Main characteristics of the implemented quasi-ideal CCII

CCII parameter	Post-layout simulated value
Supply voltage	± 0.75V
Power consumption	118μW
3dB Bandwidth	10.5MHz
Biasing Currents	6μA
Voltage Gain (α)	1.00
Current Gain (β)	1.00 (R_{load_X}=R_{load_Z}=10kΩ)
X Parasitic Resistance R_X	13Ω
X Parasitic Inductance L_X	0.4μH
X Parasitic Capacitance C_X	0.1pF
Z Parasitic Resistance R_Z	2.6MΩ
Z Parasitic Capacitance C_Z	0.03pF
Y Parasitic Capacitance C_Y	0.1pF
Silicon area	0.09mm^2

Sensor Arrays Management

As stated before, the modern advances in CMOS and VLSI technologies have enlarged the ever-increasing demand of high resolution sensors by integrating a large number of identical microsensors (i.e., arrays) on a single chip [8,18,40-44]. The multiple resistive sensing elements, typically having identical behaviours, when combined, usually in two-dimensional, *N*×*M*, array configurations, generate patterns. Obviously, the quality or the resolution of this information is enhanced by increasing the array size. Unfortunately, accessing all the elements for information collection and signal processing puts limitations on the array size [45].

Moreover, these sensors are interfaced using a suitable integrated readout circuit. In this way, the ultimate performance of the sensor arrays, employing the proper front-end electronics, depends not only on the sensor chip, but also on the same interface and its matching with the sensors. Typically, the development of a matched readout circuit itself requires a careful evaluation of sensors before its design, resulting in the iterative improvement process and making the implementation of the high resolution multi-sensor arrays complicated, costly and time consuming. Therefore, in general, the sensor array technology development needs the initial fabrication of small/moderate sized arrays as test structures that do not require the use of a particular electronic interface.

Starting from these considerations, one of the main keynodes in integrated system is the interconnection complexity of sensor arrays. In general, the access of all individual sensors requires two physical connections from each sensor resulting in a total of 2[*N*×*M*] connections. This number becomes large for even a small sized array, considering the required on-chip interconnecting metal lines and the number of bonding/probing pads.

In order to solve this problem, different scheme solutions, having reduced interconnections for the readout of all the sensors in a $N \times M$ resistive sensor array, have been proposed in the literature. One of them is reported in Figure 24 where, by means of a suitable control switching circuit, the internal connections related to the matrix rows and columns have been reduced and simplified. Moreover, Figure 24 shows also the basic signal conditioning circuit, considered to the readout of the array elements, based on the simple inverting voltage amplifier [46,47].

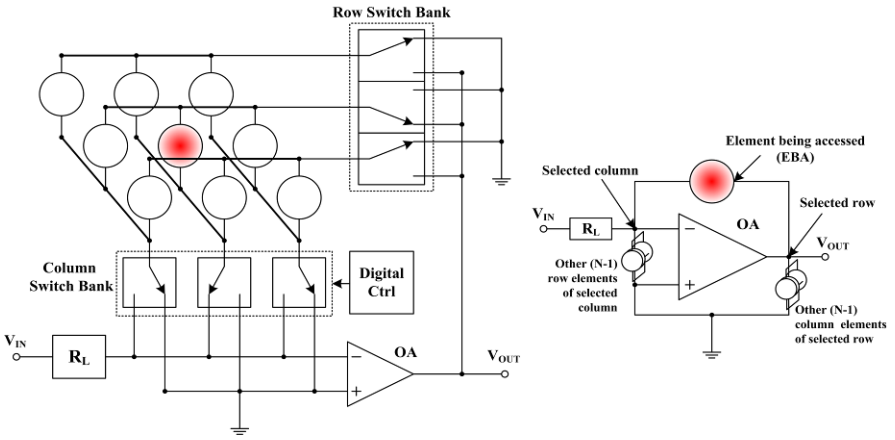

Fig. 24. A solution with reduced interconnections for a sensor array (left) and its simplified equivalent connection scheme at the conditioning circuit (right)

However, in some solutions, it is important to consider also a further significant matter resulting in the undesired information, spreading in the array, due to the interconnect overloading and the crosstalk among the sensor elements. This effect has to be necessarily avoided or reduced in integrated microsystems [44-47].

Finally, it is important to mention that in array-based sensor microsystems, composed by several sensors sensing various measurands with different sensitivities and selectivities, feature extraction techniques can be used to pull out information also from the transient sensor response [48].

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