Chapter 9
Lanthanide-Based High-k Gate Dielectric Materials

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Abstract This chapter covers selected issues related to lanthanides (or lanthanoids) used in oxide gate dielectrics. In general, lanthanides offer key material property advantages for gate dielectric applications. These include high dielectric constants, stable amorphous silicate (or ternary) phases, thermodynamic stability with Si, interface properties allowing threshold voltage tuning, and crystalline properties making possible epitaxial growth on Si and other semiconductors. Although not as heavily researched as Hf-based materials, lanthanide materials continue to hold promise for device scaling on Si, and as dielectrics on other high-mobility semiconductors.

9.1 Introduction to Lanthanide Dielectrics

Lanthanides (or lanthanoids, or rare-earths) have atomic properties making them key components for materials designed for a wide range of material properties. For example, lanthanides are key components for enhancing magnetic, optical, catalytic, and electrical properties of many materials. The dielectric properties of their respective oxides make them of interest as candidates for high dielectric constant (high-k) gate dielectrics. For example, initial interest was generated by binary compounds such as lanthanum oxide or lanthana (La_2O_3) and ternary compounds such as lanthanum aluminate ($LaAlO_3$) and lanthanum scandate ($LaScO_3$) found to have dielectric constants (k) in the range of 25–30, and sufficiently large band gaps for use as dielectrics on silicon, in the 5.0–6.0 eV range [1–3]. Additionally, from

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a thermodynamic viewpoint, it appears that lanthanide oxides are chemically stable in contact with Si [2]. Additional reasons fueling interest in these materials as metal–oxide–semiconductor field-effect transistor (MOSFET) gate dielectrics include the following: (1) many of these lanthanide oxide materials have not been comprehensively studied in bulk form, certainly not the many potential ternary alloy options; (2) the properties of metastable amorphous thin films of these binary or ternary alloys were in many cases unknown; and (3) the fact that some properties are 'tunable' as one moves across the series due to f-orbital filling levels opens possibilities for desirable properties to be obtained.

This interest in lanthanides in the arena of high-κ gate dielectrics has continued to strengthen as it has been shown that lanthanide materials: can provide MOSFET threshold voltage (V_T) control to achieve band-edge values for n-channel devices [4]; and are promising as dielectrics on alternate channel materials such as GaAs or other III–V compounds [5], as lanthanides are chemically similar to group III elements in some respects.

As is the case for all materials and applications, a host of factors must be considered when selecting particular materials for a given application. Although the lanthanides are similar in many respects (all have electronegativity values of $\sim$1.1, most have +3 valence), and have some properties which vary smoothly across the series (such as ionic radius), they differ in various ways. For example, for stable dielectric properties which are insensitive to electric field or temperature or oxidation environment, it is typically essential to have cation elements having a single stable oxidation state. This would favor the use of La, Nd, Gd, Dy, Ho, Er, and Lu which have stable +3 oxidation states (disregarding the radioactive Pm) over the other lanthanide elements which have some tendency towards mixed +3 and +2 oxidation states. Furthermore, La, Gd, and Lu might be grouped due to their similarity in electron configuration, with $5d^16s^2$ available bonding electrons and their f-orbital being empty, full, or half-filled; however, other properties differ along this group such as ionic radius (decreasing), and melting point (increasing). Thus, we will discuss only some key lanthanide elements primarily from those listed above with a single oxidation state, with the hope of covering key materials having properties of interest as gate dielectrics.

9.2 Lanthanide Materials Properties

Most of the known properties of lanthanide dielectrics derive from studies on bulk crystalline materials, to be briefly summarized here, with some information related to thin films included as appropriate. Discussed here are some prerequisite dielectric properties for use as a gate dielectric; detailed issues specific to particular thin film gate stacks will be discussed later.

9.2.1 Physical/Structural Properties

As covered in reviews by Adachi and Imanaka [6] and others [7, 8], all the lanthaniods oxidize readily, typically forming +3 valence sesqiuoxide (Ln_2O_3) lanthanide compounds, with melting points ranging from 2,200 to 2,500 °C. The f-orbital electrons do not participate directly in chemical bonding, but do facilitate valence changes to +2 or +4 that occur in some elements such as Ce, Pr, or Tb. F-orbital electrons also affect other properties, such as magnetic or optical properties, not discussed here.

In the presence of water vapor, many of these oxides will form lanthanide hydroxides, with the hydroxide tendency decreasing with increased lanthanide atomic number, in general [6]. For example, La_2O_3 readily forms hydroxides [9], while for Dy_2O_3 or Ho_2O_3, hydroxide formation is minimal [7]. Carbonates will also form, but these are more limited to the outer surfaces. Hydroxide and carbonate formation will generally result in a lower density material, with lower dielectric constant (k), and higher loss and leakage. Thus in situ capping of these binary dielectrics is critical, and partly explains the desire to move towards ternary compounds such as silicates and aluminates, which are very stable with respect to atmospheric exposure [9, 10].

The binary lanthanide sesquioxides can exist in 5 crystal structure variations, as shown in the Fig. 9.1 phase-relationship diagram adapted from Adachi and Imanaka [6]. For temperatures of interest here (up to ~1,000 °C) typically either a hexagonal (termed 'A' form) or a cubic (termed 'C' form) phase are observed. Table 9.1 summarizes key materials and dielectric properties of select lanthanides. Below ~400 °C the cubic phase has been generally believed to be the stable phase for all lanthanides [6], but the hexagonal 'A' phase persists in practice for La through Nd (for example, Zhao et al. [11] and Schroeder et al. [12]). Marsela and Fiorentini [13]. have shown by structure calculations that the hexagonal phase of La_2O_3 has 0.2 eV lower energy per formula unit than the cubic bixbyite phase, and thus expected to be the equilibrium phase. It appears that the cubic bixbyite phase is only observed for La_2O_3 if impurities or appropriate nucleation sites are present

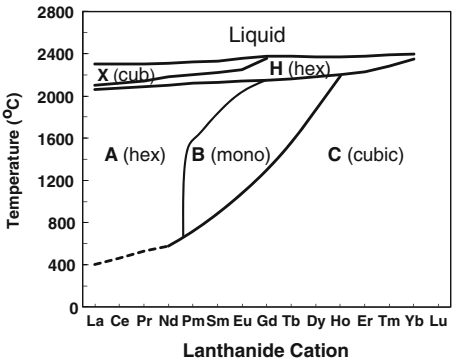

Fig. 9.1 Phase relationship diagram of binary lanthanide sesquioxides (adapted from Adachi [6])

to stabilize this structure, as occurs for some thin films formed by decomposition of molecular precursors [14]. In the hexagonal 'A' phase (La_2O_3 through Nd_2O_3), the cations have a coordination number of 7. The cubic 'C' phase is the bixbyite structure, in which cations are 6-fold coordinated in a matrix which can be described as having ordered vacant sites on the oxygen sub-lattice.

Ternary compounds are typically found in perovskite-like orthorhombic (pseudo-cubic) crystal structures (such as $LaAlO_3$) or pyrochlore phases ($La_2Hf_2O_7$). Lanthanide silicates may exist in a variety of crystalline phases, but typically in either Ln_2SiO_5 or $Ln_2Si_2O_7$ compositions [15, 16].

For use as a gate dielectric, the tendency has been to focus on amorphous dielectrics (following on the success of SiO_2 and SiO_xN_y), and to attempt to frustrate dielectric crystallization, as defects within grains or at the grain-boundaries have been linked with reliability degradation [17]. For standard (gate first) silicon-based transistor application, specific materials-related properties of interest are: (1) the amorphous phase stability temperature; and (2) the interface properties of lanthanides in contact with silicon or silicon dioxide.

From a thermodynamic viewpoint, the lanthanide oxides appear to be very stable oxides, with very large (negative) enthalpy of formation [6]. From available data, these oxides appear to be stable in contact with Si [2]. However, in the presence of excess oxygen, the interface will oxidize to SiO_2, and the mixing of silica and lanthanide oxides to form silicates is energetically favorable, as Liang et al. [16], Marsela and Fiorentini [13] discuss. The mixing of silica and lanthanide oxides to form a silicate lowers the overall free energy compared to having separate oxide layers, although reaction temperatures will depend on diffusion coefficients and other kinetic considerations. A comparison of amorphous La and Hf silicate crystallization temperatures and dielectric constants [1] are shown in Fig. 9.2. The higher temperature amorphous phase stability favors amorphous lanthanum silicate over Hf silicates. Additionally, the crystallization of HfSiOx dielectric corresponds with a decomposition reaction (phase separation) [18] resulting in low-k SiO_2 formation, while the lanthanide-silicates maintain a silicate phase without phase-separation [18]. Lanthanide silicates are also more stable with respect to atmospheric exposure [9] than the binary oxides, and the silicate reaction can be used to minimize the low-k silica interface layer thickness in the stack [19]. Thus the silicate is in many respects advantageous compared to the binary lanthanide. For a gate-last approach, with limited process temperatures and less restriction on the amorphous phase stability or interface reactivity, dielectrics with higher k than the silicates may be utilized.

9.2.2 Electrical/Dielectric Properties

In their crystalline forms, binary lanthanides have band gaps and dielectric constants making them attractive choices as gate dielectrics; select values are listed in Table 9.1 (some data is that of amorphous films, when crystalline reference data is

Table 9.1 Materials and dielectric properties of selected lanthanides. Structure and lattice parameters from JCPDS (1998), unless indicated

Material	Equil. structure	Lattice parameter (Å)	Dielectric constant (k)	Band gap (eV)	CB offset (eV)	ΔH_f° kJ/mol O_2
Ln_2O_3						
La_2O_3	Hex. 'A' type	a 3.94 c 6.13	23 [49] 27 [36]	5.5 [6]	2.3 [3]	−1,196 [6]
Nd_2O_3	Hex. 'A' type	a 3.83 c 5.99	12–14 [20]	4.7 [6]		−1,205 [6]
Gd_2O_3	Cubic 'C' type, bixbyite	10.81	12–14 [20], 24 [21]	5.4 [6]		−1,211 [6]
Dy_2O_3	Cubic 'C' type, bixbyite	10.67	12–16 [20]	4.9 [6]		−1,242 [6]
Ho_2O_3	Cubic 'C' type, bixbyite	10.61	12–13 [20]	5.3 [6]		−1,254 [6]
Er_2O_3	Cubic 'C' type, bixbyite	10.55	12–14 [20]	5.3 [6]		−1,265 [6]
Lu_2O_3	Cubic 'C' type, bixbyite	10.39	11–13 [20]	5.5 [6]		−1,247 [6]
Sc_2O_3	Cubic 'C' type, bixbyite	9.85	14 [25]	6.3 [25]		−1,271 [6]
Y_2O_3	Cubic 'C' type, bixbyite	10.60	11.4	5.7 [26]	1.6 [3]	−1,270 [6]
$LnMO_3$						
$LaAlO_3$	Rhomb., Perovskite-like	3.79 pseudo-cubic	24 [29]	5.5 [30]	1.8 [3]	
$LaScO_3$	Orthorhombic Perov-like	a,b ~ 5.84, c ~ 8.06 [52]	24–27 [52]	5.5–5.8 [52]	2.0 [54]	
$GdScO_3$	Orthorhombic Perov-like	5.49, 5.75, c 7.93	20 [27, 52]	5.5–5.8 [52]	2.0 [54]	
$LnLnO_3$						
$LaLuO_3$	Orthorhombic Perov-like	5.8, 6.0, c 8.35 [33]	32 (amor) [32]	5.2 [32]	2.1 [32]	
$Ln_2M_2O_7$						
$La_2Hf_2O_7$	Cubic, ~Pyrochlore	10.77	20 (amor) [28]	5.9 [54]	2.0 [54]	
$Ln_xSi_yO_z$						
~La_2SiO_5	monoclininc	9.33, 7.51, c 7.03	20 (amor) [49]	6.5 [76]		−1,106
~$La_2Si_2O_7$	monoclininc	13.19, 8.79, c 5.41	12 (amor) [49]	7.0 [76]		
SiO_2	~amor		3.9	9.0	3.1 [3]	−910.7

not readily available). La_2O_3 has possibly the largest dielectric constant ($\sim$23–28), with the expected dielectric constants in the $\sim$12–15 range for most of the binary oxides [20]. However, some reports for Gd_2O_3 [21], CeO_2 [22] and Pr_2O_3 [23] describe dielectric constants in the 20–30 range or higher, presumably due to effects of crystal structure and orientation, requiring further validation. Scarel et al. [24] reports that hexagonal La_2O_3 has a k of 27, whereas the cubic phase gives a value of 17. This may be the key explaining why many different values of k are reported, especially for the lanthanides composed of La, Ce, Pr, and Nd, which can exist in either hexagonal or cubic structures, in various orientations. Indeed, the higher atomic number lanthanides of the cubic bixbyite phase (and bixbyite Sc_2O_3 and Y_2O_3) almost universally have k from 10 to 15, indicating that crystal structure may be more influential than lanthanide atomic number for k determination.

As one moves across the lanthanide binary oxide series, the band-gap has a maximum value of about 5.5–6.0 eV for La_2O_3, Gd_2O_3, and Lu_2O_3, corresponding to empty, half-filled, or a full f-orbital. Thus, due to dielectric constant and band-gap, La-based materials have been most heavily researched, although due to its hygroscopic nature some researchers have focused on other lanthanides such as Gd or Lu which are more moisture resistant, or related Sc and Y compounds having similar band gaps [25, 26] although lower k values.

Although somewhat more complex when considering film growth and composition control, ternary compounds typically offer higher temperature amorphous phase stability [1], as shown in Fig. 9.2 for silica alloying of La_2O_3 and HfO_2. This has been believed to be the key for maintaining smooth interfaces and low leakage after source/drain activation anneals. Silicates also offer dielectrics with wider band gap, but lower dielectric constant, shown in Fig. 9.2 comparing La and Hf silicate dielectric constants as the SiO_2 content is increased. As shown in Fig. 9.2, these amorphous dielectrics (processed below the crystallization temperature), show dielectric constant scaling nearly following a simple component mixing rule considering density effects, between the silica and lanthanide end points [1]. Mixing binary lanthanides with other lanthanides or group III or IV binary oxides, besides Si, typically also increases the amorphous phase stability, while producing

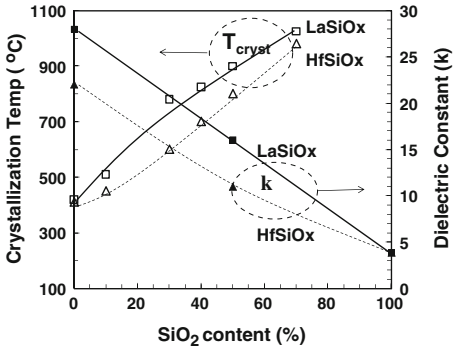

Fig. 9.2 Comparison of La and Hf silicate crystallization T and dielectric constant with silica content (adapted from Kingon et al. [1])

slightly higher dielectric constants, with little change in the band gap. Examples include lanthanide scandates [27], hafnates [28], aluminates [29–31], and mixed lanthanides such as $LaLuO_3$ [32, 33]. Additionally, for epitaxial dielectric growth, alloying can often reduce lattice mismatch with the substrate. For all these reasons, ternary compounds offer more ultimate promise than binary lanthanide oxides. The dielectric properties of La_2O_3 based ternary compounds—LaYO and LaAlO—have been briefly analyzed in Sect. 10.4.

9.3 Thin-Film Deposition and Processing

Commonly used growth techniques for lanthanide films include sputtering, thermal or e-beam evaporation (physical vapor deposition (PVD) techniques), and more recently chemical vapor deposition (CVD) techniques such as atomic layer deposition (ALD). A comprehensive listing of the growth techniques used by various researchers for lanthanide materials can be found elsewhere [34]. The gate dielectric, on silicon substrates, is deposited on either hydrogen terminated (hydrofluoric acid treated, or HF-last) oxide-free Si (001), or an 'engineered' SiO_2 or SiO_xN_y surface layer for interface defect minimization and channel mobility optimization. Thin film growth techniques typically must not damage either of these surfaces, so sputtering techniques are less preferable to other options. A key issue in general for lanthanides is the hygroscopic nature of the materials, especially La through Nd. This means that special precaution against atmospheric (water vapor and carbon dioxide) exposure is a critical issue for all deposition techniques. Additionally, magnetic properties of many of the lanthanide metals can affect the deposition process if using metallic sources. Some features specific to each deposition approach are discussed below. The basics of the deposition techniques for gate dielectrics have been described also in Chap. 4: atomic layer deposition (Sect. 4.2.2); precursors (Sect. 4.2.3); and physical vapor deposition (Sect. 4.2.4).

9.3.1 Physical Vapor Deposition

Utilizing physical vapor deposition (PVD) techniques, lanthanide-based gate dielectrics films have been reported using sputtering [11], pulsed-laser ablation deposition (PLD) [35], e-beam evaporation [36, 37], or thermal evaporation from effusion cells in molecular beam epitaxy (MBE) systems [10, 31]. Details are rarely given in the research reports, but materials must be carefully handled. Source materials should be purchased sealed in an inert gas ambient. As the lanthanide metals are very reactive with oxygen and water vapor, metal powders will quickly form oxides and hydroxides, and thus larger pieces of elemental materials should be used for e-beam or effusion cell evaporation source charges.

For e-beam evaporation of La, Al_2O_3 crucibles appear to be satisfactory [38], while we have found W crucibles effective for effusion cells. Although La melts at ~920 °C, a vapor pressure of 10^{-4} torr is not reached until 1,368 °C; practically we find that an effusion cell temperature of ~1,700 °C is necessary for La evaporation. The other lanthanides tend to evaporate more easily (typically 200–400 °C lower [38]), while oxides of any of the lanthanides typically require evaporation temperatures of 1,400–1,600 °C, with O loss occurring during heating. For effusion cell evaporation or sputtering of elemental lanthanides, reactive evaporation in oxygen ambient is sufficient to deposit oxide films. Growing the elemental lanthanide and subsequently oxidizing is an option, but rapid interface reactions can produce silicides and roughened interfaces [39]. During e-beam evaporation, it may be problematic to operate in high enough oxygen pressures, since the electron emission decreases with oxygen increases. For PLD or sputtering, elemental or oxide target materials may be used (although oxide targets require RF sputtering due to the insulating target). Again, even oxide targets convert to hydroxide very easily, and care must be taken to minimize atmospheric exposure.

9.3.2 Chemical Vapor Deposition and Atomic Layer Deposition

The advent of atomic layer deposition (ALD) has brought the general technique of chemical vapor deposition to the realm of monolayer growth control, and thus is of key importance for the growth of nm-scale gate dielectrics. This is an emerging field in relation to lanthanide oxide growth, and new or recently formulated precursor chemicals have made possible successful implementation of ALD for these compounds. Ultimately ALD is expected to be the technique of choice for virtually all high-κ dielectrics, although lack of suitable precursors has resulted in more exotic dielectric materials being studied initially by PVD techniques, with appropriate ALD precursor materials closely following.

A variety of precursors for lanthanides have been utilized by various groups [34]. Aspinall et al. [40] report that complexes of the early (lower atomic number) lanthanides with the donor-functionalized alkoxide ligand mmp (Ln (mmp)3 complexes; mmp referring to methoxy-methylpropanol) are excellent precursors for metal–organic CVD or ALD; while Paivasaari et al. [14]. utilize volatile β-diketonate type chelates Ln $(thd)_3$. Others report the use of various Ln-cyclopentadienyl complexes (Ln $(Cp)_3$) [41, 42], which result in uniform deposition at low rates, and may be advantageous due to their low melting temperatures [41].

Ozone is often used as an oxidant (instead of H_2O or O_2) to reduce C content and hydroxide formation [14, 41–43]. Complex chemistries are at play, and understanding the chemistries of the ALD process remains an area of extensive research, beyond the extent of this chapter. However, using an O_3 oxidant, these

Ln-based ALD precursors can be utilized to give high-quality low EOT (0.68 nm) device properties for La-capped HfO_2 dielectrics [41].

9.4 Lanthanide-Based Dielectric Gate Stacks

9.4.1 Lanthanum Oxides and Silicates

Extensive research has been performed on La-based oxides and silicates, as it was recognized [1] that these had the most promising values of dielectric constant, band gap, and amorphous phase stability. Key to the successful application of high-κ materials is the ability to fabricate the transistor gate with capacitance values equivalent to sub-nm SiO_2 oxide thickness. When utilizing high-κ dielectrics, gate capacitance properties are compared by referencing to the dielectric properties of ideal SiO_2 dielectric, thus determining a capacitor's 'equivalent silica oxide thickness' (EOT). Making use of the silicate reaction provides a route towards aggressive sub-nm EOT scaling [19] by thinning the SiO_2 interface layer (IL). La-based dielectrics have resulted in some of the lowest EOT gate stacks reported (0.5–0.75 nm) when processed under moderate temperatures [19, 36, 39, 41]. Discussed below are properties of La_2O_3 and lanthanum silicate ($LaSiO_x$) gate stacks deposited by reactive evaporation of La in an O_2 ambient, typically on a thin SiO_2 oxide on Si.

9.4.1.1 Gate Stack Electrical Properties

One approach to obtain low EOT devices is to deposit a thin lanthanide oxide on a silica chemical oxide, and anneal to allow interface SiO_2 consumption by the silicate phase formation. Capacitance versus gate voltage, and gate leakage data are shown in Fig. 9.3a, b for metal insulator semiconductor (MIS) capacitors with

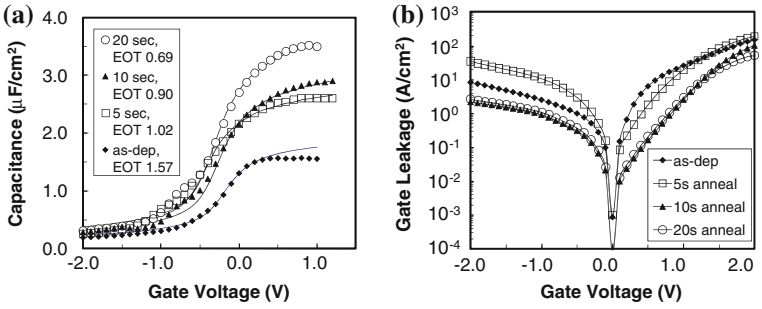

Fig. 9.3 **a** Gate capacitance and **b** leakage curves of a La_2O_3/SiO_2 bilayer stack as a function of 400 °C RTA time, in N_2

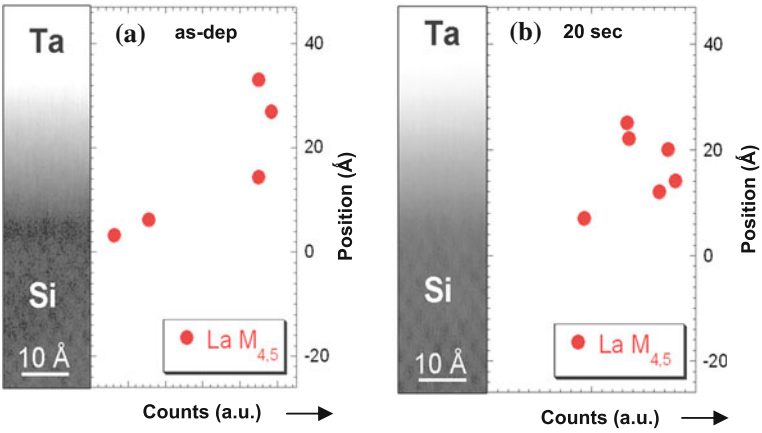

Fig. 9.4 HAADF images and corresponding EELS La $M_{4,5}$-edge intensity (increasing to the right), with position indicated as distance from the Si interface (taken as zero). The figures show La_2O_3/SiO_2 bilayer gate stacks (**a**) as-deposited, and (**b**) after 20 s RTA in N_2. SiO_{-2} interlayer is consumed by gate stack anneal

e-beam evaporated 60 nm Ta electrodes, capped with 60 nm W and reactive-ion etched (RIE) [19]. The data are shown for a bilayer dielectric of 1.6 nm La_2O_3 deposited on a ~0.8 nm SiO_2 chemical oxide on Si, measured at 1 MHz, with a 50 mV signal. As the gate stack undergoes a post-metallization anneal (PMA), the stack EOT decreases from an initial value of 1.57–0.69 nm after 20 s at 400 °C in N_2 [19]. Also, the gate leakage correspondingly decreases, as in Fig. 9.3b. As corroborated by the cross-sectional transmission electron microscope (TEM) image, the EOT lowering corresponds to dielectric thinning, caused by a combination of silicate formation, densification, and some oxygen gettering of the SiO_2 layer. Note the flatband voltage decrease as the silicate reaction proceeds, which may explain the flatband voltage shifts observed by Kuriyama et al. [44] for post-deposition anneal (PDA) of La_2O_3 on HF-last Si.

Figure 9.4a, b shows high-angle annular dark-field (HAADF) images and La electron energy loss spectra (EELS) peak intensity of the gate stack before (a) and after (b) the 400 °C 20 s PMA. The initial SiO_2 interface layer (dark in Fig. 9.4a HAADF) is seen to disappear after the anneal (Fig. 9.4b), corroborated by the La EELs signal uniformity after annealing. The lanthanum silicate bonding is determined by X-ray photoelectron spectroscopy (XPS) analysis [10] of La 3d and O1 s peaks in films with no metal capping; O gettering by the gate metal is a possible secondary EOT reduction mechanism, in conjunction with the silicate formation. The key aspect is that this silicate reaction can be a route to achieve low (sub nm) EOT, by minimizing SiO_2 IL thickness, ideal for the gate-last fabrication processes.

Under only low temperature processing [without forming gas (H_2 in N_2) anneal (FGA)], although low EOT can be obtained, high fixed charge level and high interface trap density (D_{it}) are observed as shown in Fig. 9.5. In Fig. 9.5a

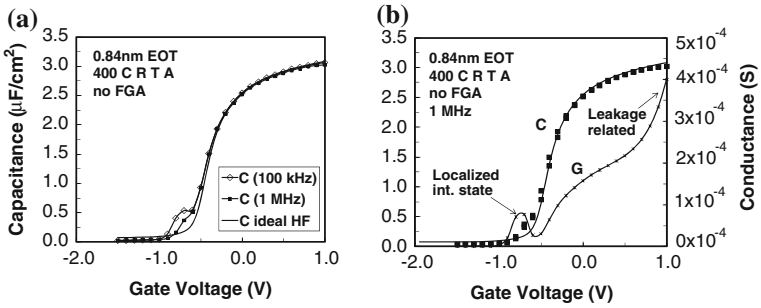

Fig. 9.5 **a** Frequency dispersion in low temperature processed $LaSiO_x$ on n-type Si. **b** C–V and G–V curves at 1 MHz showing effects of a localized interface state

frequency dispersion comparing 100 kHz, 1 MHz, and an 'ideal' HF curve are shown, revealing a sharp capacitance (C) 'hump' indicative of a localized trap state. Figure 9.5b shows the 1 MHz, 50 mV C–V and conductance versus voltage (G–V) signals, showing that the C 'hump' correlates with the conductance peak as expected. Comparing the frequency dispersion of low temperature processed La-SiO_x (1.4 nm EOT) on p- and n-type Si, we note a much greater frequency dispersion on n-type Si than on p-type Si, and determine that electron trapping is much more prevalent than hole trapping [45]. The lanthanum silicate reaction process is believed to result in this high interface defect density, under low temperature processing. This is expected to be due in part to the low temperature (forming an imperfectly bonded silicate), and partly due to the silicate reaction virtually eliminating the SiO_2 at the Si interface, and new La–O–Si interface bonding taking its place at (or very near to) the Si interface. In general, interface bonding constraints due to differing valence and O coordination number will tend to increase trap densities when introducing lanthanide oxides (or silicates) on Si or SiO_2/Si [46].

Typical gate-first processing requires that the complete gate stack undergo a high temperature anneal. Results for PMA of gate stacks which have received a prior 400 °C in situ silicate reaction anneal (to form silicate before gate metal deposition) are shown in Fig. 9.6. For capacitors with W-capped TaN electrodes, PMA anneals up to 1,000 °C for 5 s (simulating the source/drain anneal) result in a gradual increase in EOT, from 0.6 to 1.0 nm, as shown in the Fig. 9.6a C–V curves (1 MHz, 50 mV signal). In this case, starting with a silicate, further anneals grow an additional SiO_2-rich interface region [19] if excess O is available, often coming from the gate metals such as W [47]. This lowers the interface state density and the total stack charge, as revealed by the C 'hump' and V_{FB} shifting. Modeling these C–V curves and their frequency dependence [45] allows D_{it} distributions and total fixed charge densities to be extracted. After the 1,000 °C RTA, the net effective charge is reduced by 5×10^{12} cm^{-2} (V_{FB} shift), and the peak interface trap density (as shown in Fig. 9.6b) decreases from 3×10^{13} to 6×10^{11} cm^{-2} eV^{-1} without FGA. C–V data fits indicate device effective work function ($\phi_{m,eff}$) values

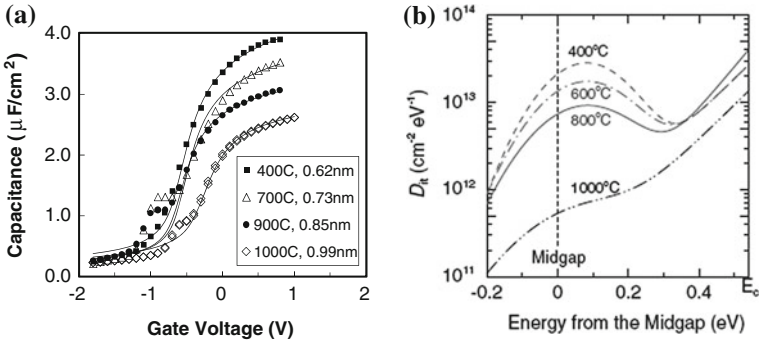

Fig. 9.6 TaN/LaSiO$_x$/Si gate stack after RTA in N_2. **a** Annealing results in some SiO_2 interface re-growth (excess O present), increasing EOT from 0.6 to 1.0 nm, but reducing interface states. **b** D_{it} extracted from C–V for each temperature

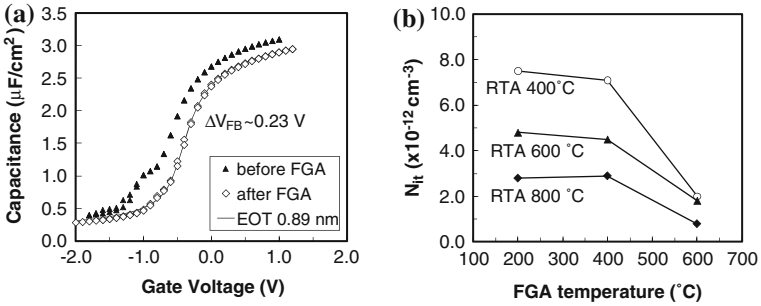

Fig. 9.7 **a** C–V before and after FGA for W/TaN/LaSiO$_x$/Si stack. **b** total N_{it} as a function of PMA RTA temperature, and subsequent FGA temperature

in the range of 3.6–4.0 eV. This makes these stacks of interest for n-channel (nMOSFET) devices; as will be discussed in Sect. 9.5.

After a high-temperature PMA of 1,000 °C for 10 s in N_2, a subsequent 450 °C 30 min FGA reduces both the total charge states reflected in a V_{FB} shift, and the interface states reflected in the lower C 'hump', as shown in Fig. 9.7a. However, typically FGA temperatures above 450 °C are required to significantly lower total interface state density (N_{it}) levels, as shown in Fig. 9.7b [45]. Because aggressive gate stack annealing typically results in some interface SiO_2 growth, D_{it} characteristics with increasing anneal temperature should approach that of SiO_2/Si [48]. So although high temperature processing can clearly result in low interface trap levels, obtaining low trap densities while maintaining sub-nm EOT remains a key process challenge, as excess O is hard to eliminate.

High temperature processing also significantly improves reliability under gate voltage stress (negative (or positive) bias temperature instability, NBTI (PBTI))

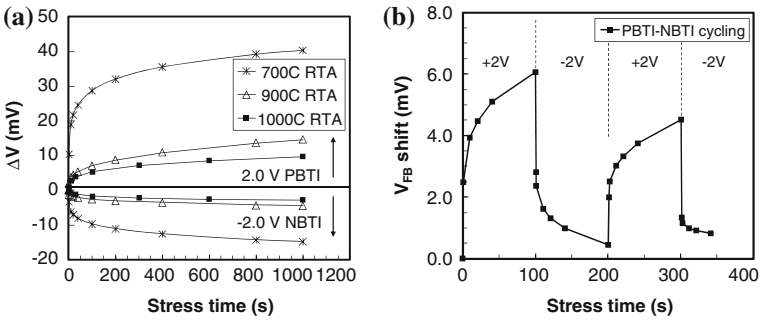

Fig. 9.8 V_{FB} shift under 2 V (PBTI) or −2 V (NBTI) gate bias, for TaN/$LaSiO_x$ MOS capacitors on n-Si with EOT ≤ 1.0 nm. **a** V shift as a function of PMA temperature, and **b** V_{FB} shift reversibility for sample with 1,000 °C PMA

stresses. Figure 9.8a, b shows the room temperature flat-band voltage (V_{FB}) shift of sub-nm EOT TaN/$LaSiO_x$/n-Si MOS devices as a function of stack RTA temperature, comparing −2 V and +2 V gate bias [49]. It is clear from Fig. 9.8a that lower T processing results in increasing amounts of V_{FB} shift, consistent with the increased defect densities as shown in Figs. 9.6, and 9.7. Also, the V_{FB} shifts are clearly recoverable as shown in Fig. 9.8b, although some net $+V_{FB}$ shift occurs revealing faster e- trapping (PBTI) than detrapping (NBTI). This reveals that PBTI stress is a more urgent problem than NBTI especially for electron-channel devices, due to large amounts of pre-existing electron traps [50].

Table 9.2 summarizes La_2O_3 and $LaSiO_x$ dielectric properties, comparing MIM to MIS devices, and various processing temperatures. While TaN MIM capacitors are useful to demonstrate potential dielectric constants, MIS devices typically will contain more Si than expected (due to additional O and subsequent silicate reaction), and thus lower k values for $LaSiO_x$. This reveals the difficult processing balance in which low temperature processing promotes aggressive EOT scaling (0.5–0.7 nm) while moderately high temperature processing is required to minimize D_{it} levels. Aggressively pursuing means to eliminate excess O in the gate electrode is critical for the gate first processes.

9.4.1.2 Gate Stack Materials Characterization

To better understand the obtained electrical properties, it is of importance to study the materials properties of these gate stacks. Critical for aggressive EOT scaling of typical gate-first processing of gate stacks are: (1) amorphous phase stability of the dielectric to source/drain activation anneal temperatures; (2) no cation diffusion into the Si channel; and (3) minimizing the low-k SiO_2 growth at the dielectric-Si interface. These have been investigated for $LaSiO_x$ gate stacks using cross-sectional TEM, back side secondary ion mass spectrometry (SIMS), and medium-energy ion-scattering (MEIS).

Table 9.2 Lanthanum-based dielectric film property summary

Film	Process temp (°C)	Thickness (nm)	EOT (nm)	k	Peak D_{it} (cm^{-2} eV^{-1})	Leakage V_{FB} +1 V (A/cm^2)
La_2O_3	400	5.6		23		**MIM** capacitor
La_2SiO_5	400	5.6		20		**MIM** capacitor
La_2SiO_5	400	4.5	1.1	16		1×10^{-4}
$LaSiO_x$	400	1.8	0.63	11	1×10^{13}	1×10^{-1}
$LaSiO_x$	1,000	~2.5	1.0	~10	4×10^{12}	3×10^{-2}
$LaSiO_x$	1,000, 600 FGA	~2.8	1.2	~9	1×10^{11}	1×10^{-2}

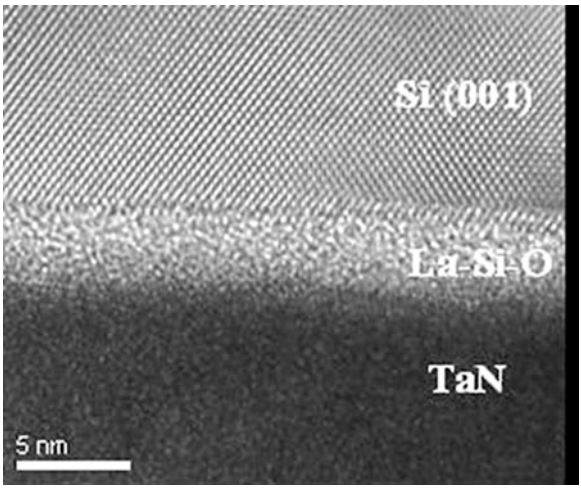

Fig. 9.9 Cross-sectional TEM of TaN/$LaSiO_x$/Si stack after RTA at 1,000 °C for 10 s in N_2

As shown in Fig. 9.9, cross-sectional TEM clearly shows that the $LaSiO_x$ dielectric remains amorphous after a 1,000 °C 10 s RTA in N_2 [51]. This is a key to keeping smoother interfaces and low gate leakage. There is no indication of phase separation with lanthanum silicate as there is with Hf or Zr silicates [18], another key advantage of lanthanide silicates in general. Using back-side SIMS analysis, it is clear that La does not diffuse into the Si [51], and thus the stack shows good thermal stability. Although the stack is chemically stable, an EOT increase is typical with annealing, as Fig. 9.6 shows. MEIS analysis of $LaSiO_x$/Si without metal capping shows clearly that there is dielectric thickening after a 1,000 °C 10 s RTA, as Fig. 9.10 reveals [49]. As these were uncapped, presumably O from the anneal chamber diffuses to the Si interface, silica forms, which subsequently reacts to form silicate. Thus annealing ultimately lowers the La content, thus lowering the dielectric constant as well. Annealing at high temperature also creates a dielectric which is stable against hydroxide formation. Figure 9.11 shows the O1s XPS spectra of uncapped $LaSiO_x$ before and after 1,000 °C 10 s RTA, from stacks corresponding to the MEIS data of Fig. 9.10. Fits to the spectra clearly show that with ~1 day of air exposure, the 400 °C formed

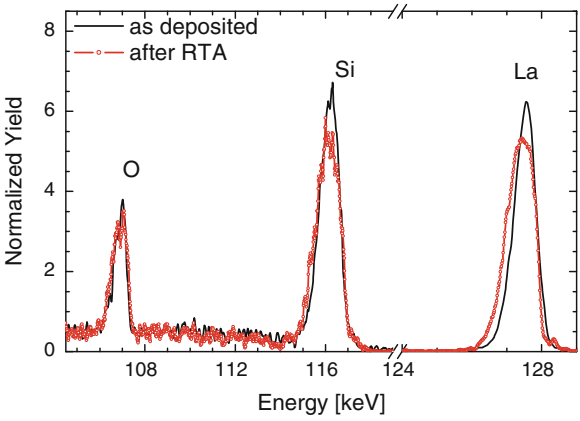

Fig. 9.10 MEIS spectra of $LaSiO_x$/Si comparing silicate without and with a 1,000 °C RTA (wider peaks, thicker $LaSiO_x$ with high-T anneal)

silicate reacts to form some hydroxide (20 % of O as hydroxide), while after the 1,000 °C RTA only about 3 % of O is bonded as hydroxide. Thus a dense silicate is very stable against hydroxide formation [10].

If excess O is properly eliminated from the gate electrode, there appear to be no fundamental reasons why these materials cannot be implemented into scaled MOSFETs, although the obtained V_{FB} (effective work function <4 eV) indicates that nMOSFET devices will be more practical, while pMOSFET devices will require stack modifications.

9.4.2 Aluminates and Scandates

The addition of a second +3 valence cation to a simple binary lanthanide oxide has important implications. Typically this will: (1) result in higher-temperature stability for an amorphous film compared to the binary oxide; (2) render the lanthanide more stable against hydroxide formation; and (3) result in crystalline structures more suitable to epitaxial growth on Si (001). Lanthanide aluminates (e.g. $LaAlO_3$) and scandates (e.g. $LaScO_3$, $GdScO_3$) have perovskite-like orthorhombic structures when crystallized. These materials have received attention especially as epitaxial oxide candidates (to be discussed in Sect. 9.6), since they have cubic lattices allowing some matching with Si, and the crystalline structures lead to large k values (of about 24–27 as reported by Heeg et al. [52], while $LaScO_3$ may have a k as high as 33 even for amorphous films [53]) and large conduction band offsets (of $\sim$2.0 eV [54]) with respect to Si. In comparison to silicates described previously, the dielectric constants of these ternaries without Si will be greater, while the amorphous phase stability limit is typically lower.

Considering $LaAlO_3$, amorphous films have been observed to have a k of only 16 [31], lower than the crystalline value of 24. However, upon PMA at above

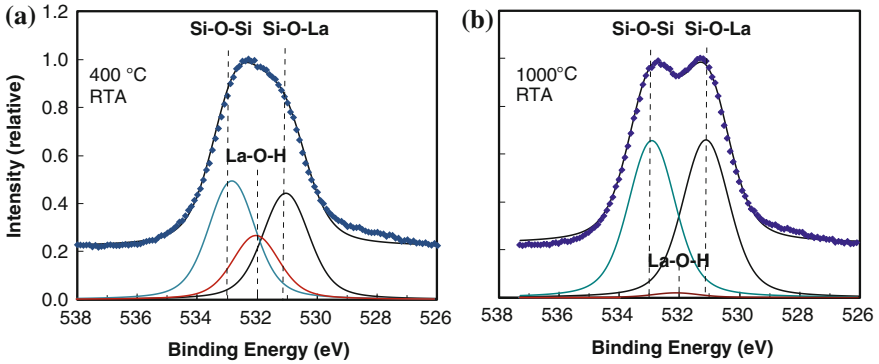

Fig. 9.11 XPS O1s peak shape of uncapped $LaSiO_x$ (**a**) with 400 °C 20 s RTA, or (**b**) after 1,000 °C 10 s RTA. High temperature silicate is impervious to hydroxide formation

900 °C simulating a source/drain activation anneal, films crystallize and partially decompose, allowing both Al and La to diffuse into the Si substrate [55]. Amorphous mixtures of La_2O_3–Al_2O_3 have an increased tendency to separate, rather than crystallize into the perovskite phase, especially in the presence of SiO_2, in which case Al_2O_3 separation occurs, and lanthanide silicate forms [56]. The amorphous phase stability can be increased to at least 1,000 °C by depositing a LaAlON film [57], in which case the phase stability rivals that of $LaSiO_x$, and the k should be higher. Cation diffusion into Si appears to correspond with the crystallization event, such that no La or Al diffusion into Si is observed for amorphous LaAlON. This is reasonable, in that this amorphous-crystalline structural change to the equilibrium phase acts as an indicator of increased diffusivity. Thus amorphous LaAlON maintains promise as an alternative dielectric, while amorphous $LaAlO_3$ would appear restricted to gate-last processing routes.

9.4.3 Hafnates and Zirconates

Key improvements in the properties of dielectrics such as HfO_2 can be achieved by alloying with lanthanides, such as increasing the amorphous phase stability [58], and lowering of defect levels [59]. Due to the maturity of the use of HfO_2 dielectric, Ln-modified Hf-based dielectrics have been implemented in scaled MOSFET devices, thus better characterized than other lanthanide binary or ternary compounds.

When alloying lanthanides with Hf or Zr oxides, the resulting compound retains a high dielectric constant, in contrast to the silicates. The +3 valence Ln cation addition to the +4 Hf or Zr results in a mixed cation coordination alloy, which helps to frustrate crystallization. If formed, the crystalline phase is a very stable pyrochlore-type phase, such as the $La_2Hf_2O_7$ composition. In addition, the Ln

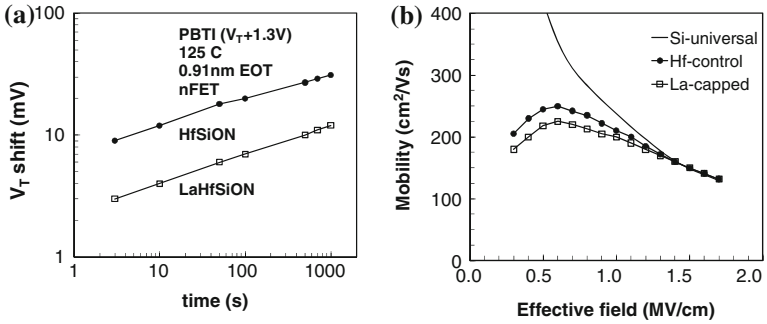

Fig. 9.12 MOSFET properties comparing effects of La addition, on **a** PBTI reliability, and **b** electron mobility (from Kirsch et al. [64], and Kang et al. [65])

present plays the important role of converting (at least some of) the SiO_2 interface layer to a higher-k Ln-silicate, to further lower EOT beyond that possible with HfO_2 alone [60].

Another key improvement obtained by alloying HfO_2 with lanthanides (expected to apply to zirconia as well) is the attainment of nMOSFET band-edge effective work function [4, 61–63]. Effects of Ln addition on V_T, a critical issue with regard to MOSFET device properties, will be discussed in Sect. 9.5.

It has been observed that HfSiON-based MOSFETs (EOT $\sim$0.9 nm) with a lanthanide addition improves the PBTI device reliability [63–65]. Using a La_2O_3 capping layer results in a $\sim 3\times$ reliability improvement under PBTI stress compared to a control $HfSiO_x$ dielectric without lanthanide, shown in Fig. 9.12a, and listed in Table 9.3. Additionally, there is little mobility degradation upon adding La, indicated in Fig. 9.12b and Table 9.3. The PBTI reliability enhancement may be linked with the ability of the Ln addition to enhance the amorphous phase stability, thus limiting defects associated with crystalline dielectrics [17]. Maximizing device mobility is another complex issue relating to the entire gate stack including the metal gate electrode, but it is clear that the Ln addition can result in very little mobility degradation.

Table 9.3 nMOSFET properties with and without La addition to $HfSiO_x$ (Kirsch et al. [64].)

	LaHfSiON	HfSiON
EOT	0.9 nm	0.9 nm
V_T	0.33 V	0.66 V
Mobility (1MV/cm)	200 $cm^2/(V{\cdot}s)$	210 $cm^2/(V{\cdot}s)$
PBTI (V_T + 1.3 V) (125 °C, 1,000 s)	12 mV	31 mV

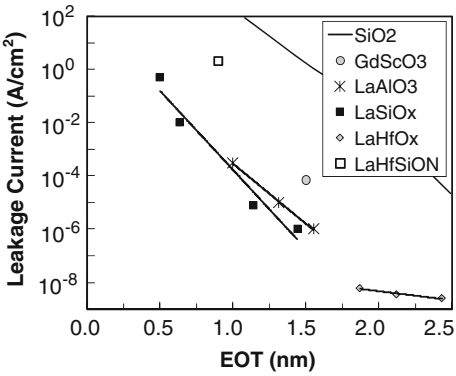

Fig. 9.13 Comparison of leakage and EOT of representative multi-component lanthanides. Data from Wagner ($GdScO_3$ [27]), Edge ($LaAlO_3$ [31]), Lichtenwalner ($LaSiO_x$ [49]), Rittersma ($LaHfO_x$ [59]), and Kirsch (LaHfSiON [64])

9.4.4 Multi-Component Dielectrics Summary

In comparison to binary lanthanides or other binary oxides such as HfO_2, dielectrics with at least one additional cation (ternaries) offer several potential advantages for use as a gate dielectric. These include: (1) a higher-temperature amorphous phase-stability; (2) a potential for limiting IL SiO_2 formation; (3) an ability to control device V_T; and (4) a means of reducing V_T shift during PBTI stress. A comparison of capacitor data of various ternary dielectrics from various groups is shown in Fig. 9.13 (while LaHfSiON represents MOSFET data). These ternary dielectrics all result in much lower-leakage gate stacks in comparison with SiO_2, while maintaining the additional benefits described above. As the search for higher k is expected to move towards epitaxial oxide growth, multi-component systems allow the ability to tune the lattice parameter for enhancing epitaxial lattice match.

The particular choice of which dielectric is the best as a gate dielectric has to consider the many aspects of device properties such as EOT, V_T, mobility, ease of processing, etc.; and the choice may differ for n versus p MOSFET, or for gate-first versus gate-last processing.

9.5 Threshold Voltage Control

Although V_T control will be covered in a separate chapter, key issues related to V_T control using Ln elements in the dielectric layer is mentioned briefly here. (Sects. 2.3 and 2.8.1—covers the theoretical basis for flat-band and threshold voltages and the complications in the case of the high-k gate stacks. The threshold voltage anomaly and the role of the interface dipoles in it have been analyzed in Chap. 6. Work function considerations and threshold voltage tuning by interface dipoles and oxygen vacancies has been outlined in Chap. 5.) Initial attempts to control V_T

were based primarily on finding appropriate electrode alloy work functions. More recently it has been understood that any region of the gate stack may be influential in controlling device V_T, especially the regions near the Si interface. It is worth noting, although not covered here, that Ln elements alloyed in the metal gate can influence the device work function [66], but here we focus on Ln (or similar) elements within the dielectric layer.

9.5.1 nMOSFET V_T Control Strategies

Early work with capacitors showed that lanthanide dielectrics resulted in very low effective work function devices (originally perceived to be problematic, as it was expected to degrade channel mobility), while for Hf-based dielectrics mid-gap work functions were prevalent. This was taken advantage of in a simple way by Alshareef et al. [4]. by applying a thin lanthana cap layer to a Hf-based dielectric to obtain nMOSFET band-edge V_T devices. It was shown that with a 0.5 or 1.0 nm La_2O_3 cap, a V_T reduction of more than 0.4 eV was obtained, with very little mobility loss (achieving 92 % of the SiO_2 universal mobility). Split C–V measurements of nMOSFETs are shown in Fig. 9.14a, revealing the V_T lowering by a La_2O_3 capping of the HfSiO dielectric. Backside SIMS analysis (Fig. 9.14b) reveals that after a spike anneal processing, the final device has the La reaching the bottom of the HfO_2 layer, although initially deposited as a cap layer [4].

The V_T lowering has been correlated to the presence of Ln cations at the SiO_2 top interface (as is corroborated by depositing lanthana directly on SiO_2 [49]), and is adequately described by an interface dipole model [67] which considers electronegativity and ionic radii of the various cation components in the dielectrics, and their influence at the SiO_2/high-κ interface. It has been shown that V_T lowering occurs with various Ln elements as well as other group II or III cations mixed with HfO_2 [62, 67].

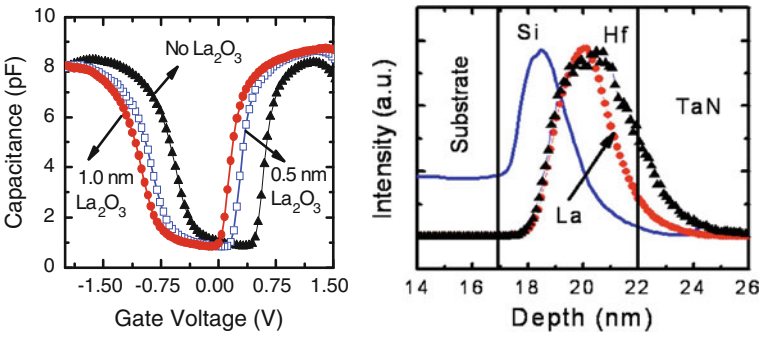

Fig. 9.14 MOSFET split CV (*left*) showing the V_T lowering with La_2O_3 capping. After spike anneal processing, the La reaches the bottom of the HfO_2 layer, shown by backside SIMS (*right*). From Alshareef et al. [4]

Other critical aspects of the V_T control are expected to relate to the silicate-like bonding at the interface, which determines bond density and directionality at the interface, and thus contributes to determining the net dipole moment beyond the issues of ionic radius and electronegativity. Without considering effects of local interface chemistry, a simple addition of a series of interfaces would not be expected to result in the significant net dipole effect as is seen in practice. Kita and Toriumi [68] present a model describing how the O density difference in the dielectrics at the SiO_2 interface may be the root origin of the interface dipole. Although there remains debate concerning specifics, there is wide consensus [62, 67, 69] that the V_T control relates to effects predominantly at the bottom high-k interface with SiO_2, and is not simply a top-electrode work function change.

9.5.2 pMOSFET V_T Control Strategies

As any high-temperature treatment typically results in the Ln element diffusing to the SiO_2 IL, typical gate first processing will produce nMOSFET V_T values. To obtain pMOSFET V_T with a Ln element present, the Ln would need to remain at the top interface, necessitating gate-last processing and additional dielectric layering schemes [70]. However, the use of elements such as Al [68] would be more suitable, and Ln elements are typically not pursued for pMOSFET applications.

9.6 Epitaxial Lanthanide High-*κ* Gate Dielectrics

As device scaling continues to push EOT to the values required for the 22 nm device node and beyond, dielectric constants in the range of 25 and higher will be required. This drives research efforts into epitaxial dielectrics compatible with the semiconductor channel material, as epitaxial dielectrics should have virtually no low-k interface layer, and crystalline oxides have higher k than their amorphous counterparts. This is another area where lanthanide-based dielectrics appear to again be advantageous, based on lattice structure and chemical compatibility. Issues related to epitaxial growth of lanthanide oxides on semiconductors is covered in detail in Chap. 11, in particular that of Gd_2O_3 on Si.

9.7 Lanthanide Dielectrics on High-Mobility Semiconductors

Scaling beyond the limits of Si devices has many researchers looking into the use of high-mobility semiconductors for the device channel, in device structures which allow higher drive current to be realized. Candidates of present interest include Ge,

GaAs and related III–V materials such as InGaAs. Whether the high mobility channel is formed from an epitaxial layer on Si, or an alternative semiconductor bulk substrate, the dielectric must be chemically compatible with the channel. Lanthanides are expected to be suitable dielectrics on GaAs based on the work of Passlack [5], and should result in acceptably high band-offsets [71] to minimize the gate leakage.

In order to realize higher device currents, the key challenge for MOSFETs on alternative semiconductors has been to achieve a low defect-level interface with the gate dielectric. On GaAs, extensive research has been performed on the use of Gd_2O_3 dielectric by Passlack [5]. They have shown the ability to obtain a low leakage dielectric and reduce interface states to acceptable levels, through an optimized process to obtain $GaGdO_x$ ($k \sim 20$) on a $\sim$1 nm Ga_2O_3 interface layer. Eliminating As oxides while precisely controlling Ga interface oxides appear to be key factors for obtaining good MOS behavior. Additionally, many groups are investigating the use of sulphur-passivation treatments [72, 73] or deposited interface layers [74] in attempts to lower D_{it} on III–V semiconductors.

As HfO_2 directly on GaAs appears to result in unacceptably high interface state densities [74], there is an impetus to look at various interface treatments, and other dielectrics, such as $LaSiO_x$ [75, 76]. Shown in Fig. 9.15a–b is an XPS comparison of 3 nm $LaSiO_x$ films on p-type GaAs (001) subjected to three different surface treatments (native oxide, HCl dip, or HCl dip and S-passivation) [75]. It can be seen that, under the restriction of a 400 °C process temperature limit, interface As-oxides are reduced after dielectric deposition, and the presence of Ga-oxide depends on the GaAs surface treatment. The S-treated interface, composed of minimal Ga-O (and/or Ga-S) bonding with no As-O, is conducive to low interface state densities [5, 72, 77]. MOS capacitor C–V characteristics as show in Fig. 9.16 indicate that the S-treatment results in the thinnest dielectric, with small hysteresis and lowest V_{FB} [75]. It has also been shown that $LaSiO_x$ on GaAs results in good values of band gap (6.5 eV) and conduction band offset of 2.7 eV [76], and thus lanthanide dielectrics appear to show promise for practical application to III–V

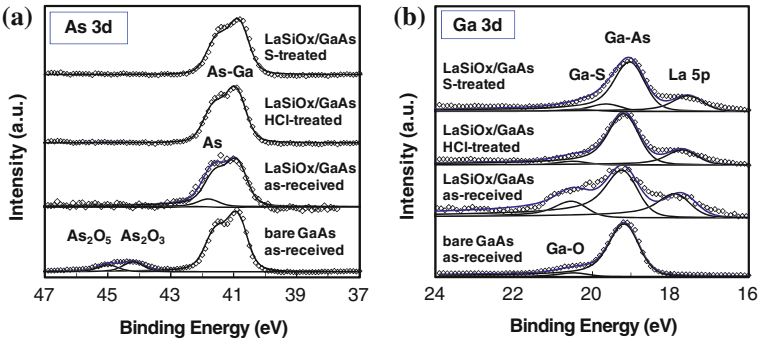

Fig. 9.15 XPS spectra of bare GaAs, and $LaSiO_x$ on GaAs comparing three surface treatments. **a** As 3d, and **b** Ga 3d spectra shown

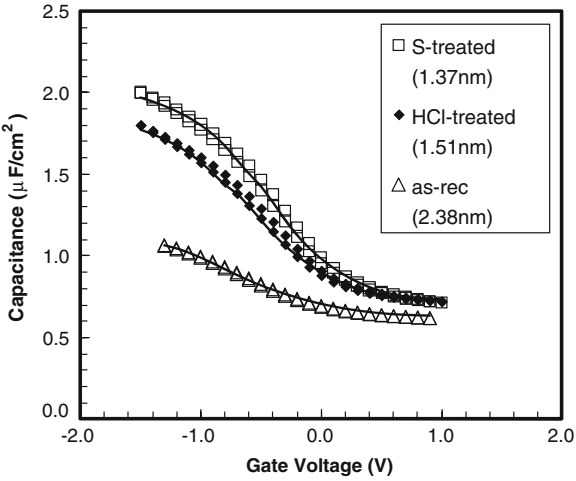

Fig. 9.16 MOS C–V characteristics of $LaSiO_x$/GaAs corresponding to the XPS spectra in Fig. 15

semiconductors. These effects of surface treatments and processing on the interface oxides is similar to that observed during ALD deposition of HfO_2 on GaAs, termed 'self-cleaning' [78].

However, as is the case for all dielectrics on III–V semiconductors, much more work needs to be done to eliminate or control defect levels near band edges, as well as deep levels, which result in channels with low carrier concentration, and low mobility. This can be done to a large extent by utilizing semiconductors such as $In_xGa_{1-x}As$, but the interface with the dielectric must be optimized simultaneously, while maintaining a high dielectric constant stack. Passivation of Ge, GaAs, and InGaAs surfaces has been covered in detail in Chap. 12.

9.8 Processing, Scaling, and Integration Issues

While lanthanide-based oxides are thermodynamically very stable oxides, as mentioned the binary oxides have tendencies towards hydroxide and carbonate formation. Consideration of the oxide integrity must be taken into account when considering wet process methods. However, ternary lanthanides or silicates do not suffer from these limitations; and gate stacks typically have some interface mixing which renders the hydroxide formation issue moot if the dielectric is extremely thin.

Relatively successful small gate length MOSFET processing of lanthanide-containing dielectrics has been demonstrated by both SEMATECH [4] and IMEC [79]. Wet etching of Ln-based oxides in weak HCl solutions gives good selectivity w/r to HfO_2 etching [79]. However, Ln-based oxide caps on HfO_2 for nMOSFET V_T tuning must be etched off in regions requiring pMOSFET V_T. When etched, it is observed that some Ln element remains in HfO_2 due to Ln intermixing [80].

Thus the ability to attain the pMOS WF will be affected. To get around this, some HfO_2 etch and re-deposition may be required, thus complicating the processing. Although processing must be optimized, there appears to be no inherent limitation to the use of Ln-based dielectrics or electrode materials. Indications are that, to obtain the lowest possible EOT gate stacks, and low effective work function for nMOSFETs, Ln materials will indeed be required in the gate stack for future technology nodes.

9.9 Summary of Lanthanide Materials and Properties

Lanthanide materials will continue to gain interest as device features shrink, requiring higher-k dielectrics with thinner interface layers, and possibly alternative channel materials. To date lanthanides have proven key components in dielectrics providing for: (1) sub-nm EOT gate stacks due to high dielectric constant and SiO_2 interface reduction, while maintaining good MOSFET mobility; (2) nMOSFET V_T control and PBTI reduction of Hf-based dielectrics; and (3) obtaining low leakage, low D_{IT} dielectrics on GaAs. Application areas which remain open for further study for lanthanide dielectrics include epitaxial oxide integration on Si or SiGe, and oxides on alternative high-mobility (III–V based) substrates for high speed applications, as well as use as a gate dielectric or passivation layer for high power FETs (for example, on SiC or GaN).

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