

Chapter 4

Hf-Based High-k Gate Dielectric Processing

Masaaki Niwa

Abstract This chapter focuses on the processing of Hf-based high-k gate dielectric film and its device fabrication to improve its electrical properties. First, the formation process of Hf-based high-k dielectric thin film is introduced followed by detail study of these films from the materials science point of view, such as its crystallization and its control, carrier trapping and doping effect on the bulk high-k film. Finally, the device processing of the Field Effect Transistor including the CMOSFET with Hf-based high-k gate dielectric and metal gate electrode is discussed.

4.1 Introductory Remarks

In accordance with the requirement of CMOS (Complimentary Metal Oxide Semiconductor) scaling, replacement of thermally grown SiO₂ gate dielectric with other dielectric materials of high dielectric constant (k) has become imperative. However, replacing of the SiO₂ conduces to a variety of other disadvantages and is not as simple as it may seem. Many challenges caused by different dielectric properties are to be conquered before the high-k dielectrics find practical use in industry. In spite of such difficult situations, thanks to intensive efforts, these insuperable difficulties have been solved gradually and finally CMOS with high-k/metal gate stack for high performance application has been in commercial production in 2007 for the first time [1]. However, still many issues were left unsolved and have been addressed continuously to overcome them. Most of them come from the fact that Hf-based high-k dielectric materials are thermodynamically unstable and the nature of the electrovalent (ionic)-bonded HfO₂ is quite

M. Niwa (✉)

Center for Innovative Integrated Electronic Systems, Tohoku University,
Sendai 980-0077, Japan
e-mail: niwa.masaaki@cies.tohoku.ac.jp

different from that of the covalently-bonded SiO_2 . Although oxygen vacancy is a common problem for the oxides, behavior of each system is completely different. For SiO_2 , the remaining unpaired electrons in Si tend to form Si–Si bond, whereas Hf is produced by releasing two electrons into the valence band of the HfO_2 and the amount of oxygen vacancy is rather large compared to SiO_2 . Key issues to improve the high-k gate stack characteristics are (1) dielectric material has high permittivity, (2) gate electrode is metal to obtain the desired work function without a depletion layer, (3) process control is easy for interfaces between high-k gate dielectric, Si substrate, and gate electrode, and (4) their module/integration process is not complicated and cost effective, and (5) the gate stack has high reliability.

In this chapter, issues of material and processing of Hf-based high-k gate dielectrics are described. First, formation process and material properties of Hf-based high-k gate dielectric are discussed. Then its influence on electrical characteristics including reliability based on the intrinsic solid state properties are taken into consideration. Several intrinsic key issues such as interfacial control, optimization of the Hf-based high-k gate dielectric formation, breakdown issues, work function control, bulk trapping phenomena as well as process integration are discussed from the point of materials science and device process technology. Issues of metal gate electrode and gate stack reliability as well as its process integration including the comparison of gate first and gate last processes are relegated to other chapters and discussed in detail.

4.2 Hf-Based High-k Gate Dielectric Formation Process

Among the current high-k gate dielectrics, the Hf-based material is the most promising, in particular HfO_2 and its silicate (HfSiO_x) have been studied intensively for practical use. As a result HfO_2 has been introduced into industry for high performance application in 2007 [1]. Generally, the requirements for the gate dielectric are: (1) High k value (but $k < 50$ because of short channel effect of FET—Field Effect Transistor); (2) High barrier property with respect to N-, PMOS gate electrodes; (3) Robust against high thermal budget; (4) Good process controllability; and (5) Capability of thin film thickness controllability. In the following sections, typical formation methods are addressed.

4.2.1 Metal Organic Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a chemical process used to produce high quality thin films, in which process the Si substrate is exposed to volatile precursors, which react and/or decompose on the substrate surface to obtain the desired composition. During the reaction, volatile byproducts are often produced, which are removed by gas flow in the reaction chamber. Among the variety of

CVD depositions, metal-organic chemical vapor deposition (MOCVD) based on metal-organic precursors is the principal method of depositing high-k gate dielectric layer. To form Hf-based high-k dielectric films, it is necessary to use metal-halide or metal-organic as a basic ingredient. Different from the Atomic Layer Deposition (ALD) method with a single wafer treatment, MOCVD has the advantage of its high throughput because of its batch processing.

HfSiON deposition is taken up as an example. For the high-k part, Si_2H_6 and HBT ($\text{Hf}(\text{OtBu})_4$) are used to form HfSiO_x . HBT has high vapor pressure among liquid Hf precursors and is generally moderate in price compared with other precursors. NH_3 is often used to form HfSiON, which leads to suppression of large gate leakage by keeping up the amorphous state in the HfSiO_x film during high temperature annealing. The effect of nitrogen doping is considered in detail in Sect. 4.3. In addition, an interfacial oxide layer (SiO_2) which is necessary to obtain high quality interface between high-k and Si substrate is formed by conventional oxidation such as Rapid Thermal Oxidation (RTO), pyrogenic oxidation or chemical oxidation.

The HfSiON thickness is selected depending on the device application. Concentration of Hf, [Hf] and Si, [Si] in HfSiO_x can be controlled by the polymerization reaction by desorption of C_4H_{10} from Si_2H_6 and HBT; and the intermediates such as $\text{Si}_2\text{H}_3[\text{O}-\text{Hf}(\text{OC}_4\text{H}_9)_3]_3$ ([Hf] = 60 %) and $\text{Si}_2\text{H}_2[\text{OHf}(\text{OC}_4\text{H}_9)_3]_4$ ([Hf] = 67 %) are decomposed on the Si substrate. However, it is interesting to note that the Hf concentration in the HfSiO_x remained constant ([Hf] = approx. 62 %) regardless of the deposition condition. It may be considered that the decomposed intermediates contribute to form HfSiO_x film under stable composition, i.e., [Hf] = approx. 60 %.

In order to reduce contaminants such as H and C in the high-k film, which are introduced from the basic ingredients, O_3 is often introduced to cause outward diffusion by forming H_2O and CO or CO_2 . Figure 4.1 shows carbon and hydrogen concentration in the HfSiO_x film observed by SIMS (Secondary Ion Mass Spectroscopy) indicating that these impurities have been effectively reduced by O_3 treatment (250 °C for 3 min.) [2]. In order to improve the film quality, MOCVD is often combined with other techniques such as Remote-Plasma Oxidation.

HfO_2 films were fabricated by MOCVD through an alternating supply process, which consists of deposition using tetrakis-diethylamino-hafnium ($\text{TDEAH}_2\text{Hf}(\text{N}(\text{C}_2\text{H}_5)_2)_4$), followed by oxidation using remote-plasma oxygen (RPO) [3]. Deposition rates are found to depend on temperature (above 350 °C) and the supply duration of TDEAH, which indicates a non-self-limiting growth mode. From X-ray photoelectron spectroscopy (XPS) analysis, it is found that as-deposited films formed only by the TDEAH are unstable due to presence of carbon and nitrogen impurities in the film. These impurities can be removed by the RPO treatment. When the supply duration of RPO is increased, the high-k film tends to be stoichiometric HfO_2 with low gate leakage current; however, excess RPO supply results in an increase of the equivalent oxide thickness (EOT) due to a decrease in the permittivity of the interfacial layer.

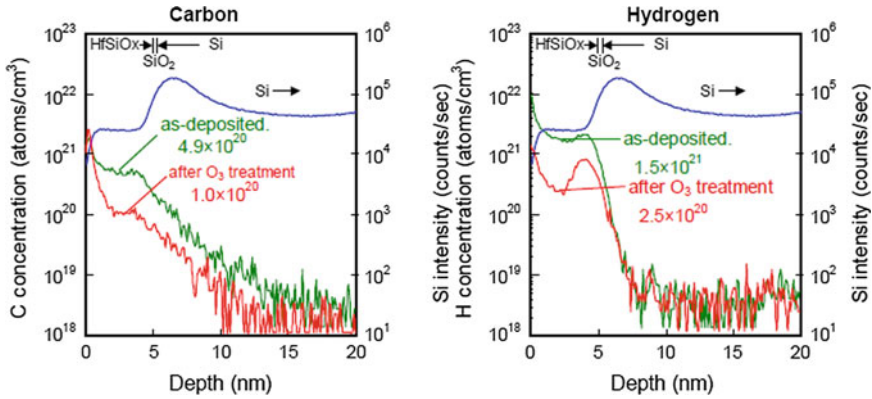


Fig. 4.1 Carbon and hydrogen concentrations in the HfSiO_x film [2]

This implies that optimization of the supply durations of TDEAH and RPO is necessary. By this optimization, a minimal EOT of 1.6 nm and a leakage current of 1×10^{-4} A/cm² at -1 V relative to the flat-band voltage are obtained without any problem.

Effect of the RPO treatment is also confirmed by other metal-organic (MO) precursors. In case HfO₂ film is formed from Hf(OC(CH₃)₂CH₂OCH₃)₄, deposition rate of HfO₂ becomes higher when oxygen gas is supplied together with the precursor, however, the deposited film contains large amount of H₂O due to the oxidation of Hf precursor. Excess oxygen process tends to degrade the HfO₂ film properties. As a countermeasure, in situ RPO is effective in reducing the contaminants in the HfO₂. As a result, leakage current of HfO₂/Si capacitors with TiN gate electrode formed without excess oxygen flow and subsequent in situ RPO can be effectively reduced [4].

In order to obtain higher deposition rate with component flexibility than the conventional ALD, precise atomic growth at high deposition rates of advanced MOCVD is developed by means of accurate injection of small quantities of liquid precursors into a heated vaporizer volume using its short pulses for the delivery of the liquid [5]. This enables a precise control of the nucleation layer growth and in situ grading of composition during film formation.

4.2.2 Atomic Layer Deposition

Atomic layer Deposition (ALD) was, at the beginning, invented as Atomic Layer Epitaxy (ALE) which is a specialized form of epitaxy by depositing alternating monolayers of two elements onto a substrate and makes use of the fact that the occurring chemisorption will continue until all sites are occupied due to self-limiting surface reaction. ALD should be taken up as a special CVD, i.e. Atomic

Layer CVD as it is similar in chemistry to CVD, except that more than one ingredient gas does not exist in the reacting chamber in the ALD reaction. In ALD reaction, two complementary precursors (e.g. $\text{Al}(\text{CH}_3)_3$ and H_2O) are pulsed alternatively and then chemisorbed onto the surface of the substrate to form monolayer. More precisely, one of the precursors adsorbs onto the substrate surface until it saturates the surface sites and extra precursor is carried away by an inert gas such as nitrogen, purging the chamber, and further growth cannot occur until the second precursor is introduced. And this cycle is repeated alternatively until the film thickness reaches its desired value. Although the film thickness is controlled by deposition time for the conventional CVD processes, it is controlled by the number of precursor cycles for the ALD process rather than the deposition time. Thus, the ALD film growth is due to self-limited surface chemical reactions and in theory it allows pin-hole free film with excellent conformity and uniformity even against bumpy surfaces.

For the HfO_2 deposition, at least two types of precursors are used in the ALD process at around 300 °C. The typical precursors are HfCl_4 and H_2O . The key issue is to reduce the Cl contamination in the formed HfO_2 to obtain high quality film. The steady growth-per-cycle, defined as amount of HfO_2 deposited in one reaction cycle, is 1.3×10^{14} Hf/cm²/cycle. As starting surface, a chemical oxide is usually introduced to allow good nucleation of the ingredient of precursors, resulting in continuous HfO_2 film growth. In order to obtain ultra-thin high-k gate stack with EOT (Equivalent Oxide Thickness) < 1 nm with minimum gate leakage as well as high channel mobility, HfAlON film was investigated by precise layer-by-layer deposition and annealing where annealing was carried out for each ALD layer [6].

4.2.3 Precursors

Precursors used for MOCVD and ALD are described in this section. Most precursors used in MOCVD and ALD are in the liquid form (liquid or solid dissolved in a convenient solvent). Liquid precursor is advantageous to limit particle formation during the deposition. Liquid solutions are injected in vaporization chamber towards injectors and vapor of the precursor is transported to the substrate. This technique is commonly used for solid precursors as well as liquid precursors and high growth rates can be achieved using this technique. Hafnium silicate layer, for example, is often deposited using the liquid precursors such as tetrakis-diethylamino-Hafnium (TDEAH) and tetrakis-dimethylamino-Silicon (TDMAS). Typical deposition temperature is around 600 °C. By changing the pressure and the gas flow rate, the produced composition can be controlled from Hafnium-rich (e.g. [Hf] = 65 %) to Silicon-rich (e.g. [Hf] = 23 %) phase. Typical precursors are listed in the Table 4.1. Order of the vapor pressure is TDEAH > HTTPB > TDMAS > TEMAZ > TEMAH for all temperature ranges.

In addition to the above precursors, solid phase precursor in which the solid is easily sublimated has also been investigated. Attempt to introduce $\text{Hf}(\text{NO}_3)_4$ as

Table 4.1 Typical Hf-based precursors

| Hf series chemical formula | Name of the precursor | Acronym name | State at room temperature |
|--|---|--------------|---------------------------|
| Hf[N(CH ₃) ₂] ₄ | Tetrakis-Di-Methyl-Amino-Hafnium | TDMAH | Liquid |
| Hf[N(C ₂ H ₅) ₂] ₄ | Tetrakis-Di-Ethyl-Amino-Hafnium | TDEAH | Liquid |
| Hf[N(C ₂ H ₅)(CH ₃)] ₄ | Tetrakis-Eethyl-Methyl-Amino-Hafnium | TEMAH | Liquid |
| Hf(OtBu) ₄ | Hafnium-Tetra-Tertiary-Butoxy | HTTB HBT | Liquid |
| Hf[OC(CH ₃) ₂ CH ₂ OCH ₃] ₄ | Tetrakis(1Methoxy-2Methyl-2Propoxy) Hafnium | | Liquid |
| HfAlO | Tri-Methyl-Alminum+TDMAH | TMA+TDMAH | Liquid |
| Hf(NO ₃) ₄ | Hafnium-Nitrate | | Solid |
| HfCl ₄ | Hafnium-Tetra-Chloride | | Solid |

oxidizing agent as well as C free metal source was reported [7]. After RCA (Radio Corporation of America) cleaning followed by diluted HF cleaning, ultra-thin Si₃N₄ layer (approx. 0.7 nm) was formed as an interfacial layer by RTN (Rapid Thermal Nitridation). The RTN treatment was performed in 500 Torr -NH₃ at 700 °C. Then HfO₂ film was deposited on the RTN base layer. HfO₂ film formation process was as follows. By introducing Ar carrier gas, HfO₂ film was formed by sublimated Hf molecular gas which was generated from Hf-nitrato, i.e., Hf(NO₃)₄ solid phase precursor under the appropriate temperature (25–70 °C). Then the Hf gas was mixed with oxygen gas in the chamber to generate HfO₂ followed by the PDA (Post Deposition Anneal) at 800 °C for 30 s in N₂. This CVD-HfO₂ is called as “nitrato”. During this process, substrate temperature was kept in the temperature range from 170 to 350 °C. The reason of using the Hf(NO₃)₄, rather than separate oxidizing agent such as H₂O, is to minimize the oxidation of the interfacial layer between high-k dielectric and Si substrate. Also, in contrast to other widely used precursors, Hf(NO₃)₄ has high reactivity with other materials, which initiates uniform deposition on H-terminated Si. However, because of its high reactivity, the interfacial layer tends to be relatively thick. Thick interfacial layer can avoid mobility degradation by remote coulomb scattering; in contrast, it leads to an increase of EOT. Furthermore, vaporization from solid phase precursor is generally unstable and thus the resulting deposition rate is unstable. Comparison with respect to different precursors is discussed in Sect. 4.3.2.

4.2.4 Physical Vapor Deposition

Different from MOCVD and ALD, physical vapor deposition (PVD) provides different advantages for thin film deposition. This deposition is purely physical deposition process rather than chemical reaction at surface. In the PVD, a wide

variety of vacuum deposition exists such as vacuum evaporation, ion plating, molecular beam epitaxy, sputtering, and laser ablation. Among them, sputtering is the most promising method from the point of commercial viability for high-k dielectric and metal gate deposition, where ions are generated by discharge and directed toward a target material and then these ions sputter atoms from the target material. The generated sputtered atoms are neutral and transported to substrate surface in vacuum and finally condense on the substrate, forming a thin film.

Sputtering is usually a simple system; therefore it provides low cost, contamination free deposition and capability of deposition of high-melting point metal as well as high adhesion to the substrate. Usually, the deposition rate is low; however, this is advantageous for ultra-thin film formation such as capping layer deposition (see Sect. 4.4) for the metal gate/high-k dielectric system. On the other hand, in contrast to ALD, it is difficult to achieve conformal coating on the bumpy structure because of the translatory movement of the sputtered atoms in the vacuum and also care should be taken for the damage generated by collision on the substrate surface. Nowadays, the PVD tool is capable of damage-free deposition and precisely controlled film composition through ultrahigh vacuum co-sputtering with excellent uniformity across the 300 mm wafer ($1\sigma < 1\%$).

Comparison of the film formation method is important because often material density and its microstructure influence more seriously than the expected chemical composition. An interfacial layer growth by unintentional oxidation during high-k deposition is a matter of concern. CVD and ALD methods suffer from contaminants such as carbon, hydrogen and chlorine that need to be removed by high temperature deposition or post deposition annealing (PDA), which brings excess oxygen into high-k dielectric as well as increase of interfacial layer. In addition, the PDA has a role to densify the high-k film. This additional thermal treatment often leads to undesirable phenomena such as composition change from as deposited composition, EOT increase as well as work function degradation as described in Sect. 4.4.6. Crystallization of high-k dielectric material due to thermal treatment is also an issue as described in Sect. 4.3.2. For this, nitrogen is often introduced to avoid crystallization of Hf-based film. Nitridation after high-k deposition is conventionally used for all types of deposition method. However, by means of PVD, the nitridation can easily be performed during the deposition. The deposited PVD-HfSiON gate dielectric with metal gate, for example, shows lower gate leakage because of its amorphous phase even after higher temperature ($>1,000\text{ }^\circ\text{C}$) annealing [8].

Similar to the discussion of precursor in CVD and ALD, purity of the target material is important in PVD as well. Impurity level in gate dielectric required for Front End of Line (FEOL) is less than 1×10^{10} atoms/cm². This indicates that the desired impurity level for the target material of PVD depends on film thickness. For high-k gate dielectric formation, there seems to be no appreciable problem from contamination point of view for Hf target because HfO₂ thickness is thin enough (approx. 1.3 nm) compared to that of metal gate electrode and purity of Hf (6N) is higher than that of the target used for metal gate (5N).

For conventional gate first process, purity of the ultra-thin capping layer on high-k dielectric for work function tuning to be discussed in Sect. 4.4.6 is also important. Generally, Al_2O_3 and La_2O_3 are intensively investigated as capping material for P- and NMOS respectively. Al or AlO target is used for Al_2O_3 capping for PMOS since its thickness is thin enough and its purity is sufficient. In contrast, La or LaO target is used for La_2O_3 capping for NMOS; however, it has low purity (e.g. 2N5 i.e. 99.5 %) in origin and has problematic deliquescence nature. The purity of La target material has been improved recently to 4N level. By improving the purity, its deliquescence could also be suppressed recently.

Regarding the metal gate electrode, the purity of the metal target is normally 5N. In case of Ti target, when Fe content is 9 wt ppm (Fe in the target material should be suppressed to less than 9 wt ppm), Fe concentration in the target turns out to be 4.4×10^{10} atoms/cm² for 1 nm-thick Ti. When 20 nm-thick TiN (Ti/N = 1/1) is deposited as gate electrode, contamination concentration comes to 4.4×10^{11} atoms/cm² which is not acceptable in the clean room. In this respect, by means of PVD, low purity (4–5N) target such as Ti is difficult to be introduced for fabrication. In contrast, Mo and/or Ta target whose purity is better than Ti, can be applicable.

In addition to pure metal and metal oxide target, alloy target has been intensively developed. In case of TiSiN, it can stay amorphous after annealing and in contrast, TiN tends to conduce to crystalline phase. Owing to its amorphous state, the obtained work function can be uniform across the wafer, however, in case of crystalline materials, distribution of work function has some variation depending on each individual grain orientation.

From purity point of view, however, it is very difficult to obtain high purity alloy target, such as TiSi and/or TaC used for metal gate electrodes because high purity alloying of Si and/or C is difficult to achieve. Similarly, from alloy target, it is difficult to obtain high purity alloy insulators such as HfLaO, AlLaO and HfTiO for future gate dielectrics. Especially, it is extremely difficult to apply them as thick insulator for flash application. For this reason, co-sputtering method is considered to be useful and practical method.

For commercial production with wafer of large diameter, PVD for gate dielectric deposition has challenge to reduce plasma damage and improve the uniformity and reducing of particles across the wafer. On the other hand, MOCVD or ALD are easily used for mass-production, however, they suffer from hydrocarbon or halogen contaminants. In order to avoid such disadvantages, post deposition annealing is necessary to suppress plasma damage or impurity incorporation.

4.2.5 Interfacial Oxide Layer

In the research of high-k gate stack, control of the interfacial reaction with the silicon substrate is one of the key issues to maintain the property of the high-k gate dielectric with suppressed interfacial defects, in particular, how we build-in an interfacial oxide. In this respect, an interfacial layer (IL) between Si substrate and high-k gate

dielectric plays an important role and usually silicon oxide layer is introduced to obtain a high quality SiO₂/Si interface. Generally, conventional high quality ultra-thin oxidation techniques are used such as RCA-type SC-1 and/or SC-2 clean, thermally grown dry oxide by RTO (Rapid Thermal Oxidation), thermally grown oxide by ISSG (In-Situ Steam Generation), ozonated wafer dispense, ozone chemical oxidation followed by HF treatment. In regard to ultra-thin RTO and ISSG oxides, the ISSG film is confirmed to have lower defect concentration at interface than in the RTO film [9]. By means of leakage-free charge pumping, trap behavior with respect to high-k and interfacial layer has been possible to be observed [10].

Effective k value is obtained from the observed EOTs by changing the physical thickness (T_{phys}) of the high-k layer as shown in Fig. 4.2. Corresponding EOT is obtained by changing the T_{phys} of high-k on the interfacial oxide layer which has constant thickness (see Fig. 4.2a). The EOT changes linearly with the high-k thickness as shown in Fig. 4.2b and thus the corresponding quantitative equation is obtained as indicated in (4.1). The first term in this equation is known value and the k value of the high-k film is obtained from the slope in the EOT-T_{phys} relation. From the EOT at T_{phys} = 0 nm (intercept of y axis), k value of the interfacial layer is obtained experimentally. In this case, k value of the high-k layer and the interfacial oxide layer underneath turned out to be approx. 12 and 8, respectively.

$$EOT = \underbrace{\frac{k(\text{SiO}_2)}{k(\text{IL})} \cdot T_{\text{phys}}(\text{IL})}_{\text{Constant}} + \frac{k(\text{SiO}_2)}{k(\text{high-k})} \cdot T_{\text{phys}}(\text{high-k}) \quad (4.1)$$

Fig. 4.2 Relation between EOT of the gate stack and the physical thickness of the high-k film. **a** Cross-sectional TEM (XTEM) of the high-k/IL. **b** Linear relation of EOT-physical thickness of the high-k film

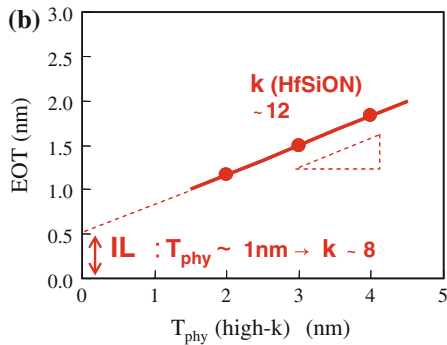
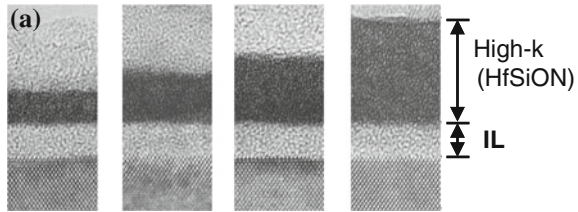


Table 4.2 Typical high-k dielectric material properties

| Material | k_d | Heat of formation (Kcal/mol) | Melting point (°C) | Structure |
|--------------------------------|---------|------------------------------|--------------------|--|
| SiO ₂ | 3.9 | 217 | 1,730 | Amorphous |
| Si ₃ N ₄ | 7.8 | | ~1,900 | Amorphous |
| Al ₂ O ₃ | 8–10 | 267 | 2,050 | Amorphous, α phase |
| ZrO ₂ | 12–25 | 262 | 2,677 | Monoclinic \rightarrow Tetragonal(1,127 °C) Tetragonal \rightarrow Cubic(2,377 °C) Amorphous up to 800 °C |
| Ta ₂ O ₅ | 25–65 | 90 | 1,870 | β phase \rightarrow α phase (1,320 °C) |
| HfO ₂ | ~30 | 266 | 2,900 | Monoclinic \rightarrow Tetragonal(1,700 °C) Tetragonal \rightarrow Cubic (2,700 °C) Amorphous up to 700 °C |
| TiO ₂ | 30–90 | 226 | 1,855 | β phase \rightarrow α phase (1,320 °C) |
| BaSrTiO ₃ | 100–300 | | | Monoclinic \rightarrow Tetragonal (1,700 °C) Tetragonal \rightarrow Cubic (2,700 °C) |

4.3 Hf-Based Gate Dielectric Material and Its Intrinsic Phenomena

In addition to the deposition methods, many attempts to improve Hf-based high-k dielectric properties have been studied involving related process such as robustness against high thermal budget, permittivity, structure and chemistry with metal gate electrode etc. In this section, Hf-based gate dielectric material and its intrinsic phenomena are considered.

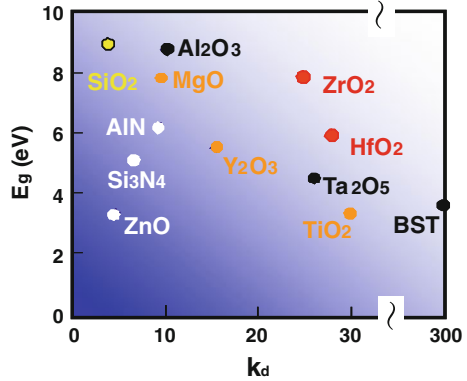
4.3.1 Hf-Based Dielectric Material

In Table 4.2, physical properties of typical high-k materials are listed. BaSrTiO₃ has large permittivity; however, it has huge hysteresis due to its ferroelectricity. This table indicates HfO₂ as well as Al₂O₃ and ZrO₂ are easier to be formed under exothermic reaction with relatively higher melting point compared to other high-k materials. And HfO₂ and ZrO₂ have relatively higher dielectric constant (k_d) among them and higher melting point than Al₂O₃. It should be noted that the lattice constant values of these materials are similar to Si lattice constant.

Also, as is shown in Fig. 4.3, band gap (E_g) varies inversely proportional to dielectric constant (k_d) and these three materials reveal higher k_d with larger E_g , especially HfO₂ and ZrO₂. In this respect, Hf-based high-k materials including Hf-Aluminate and Hf-Zirconate as well as Hf-silicate have been intensively investigated. Incorporation of doped oxide into HfO₂ is discussed in Sect. 4.3.5.

The EOT dependence of the gate leakage current density is indicated in Fig. 4.4. As is shown in this figure, HfO₂ and ZrO₂ dielectrics reveal lower leakage

Fig. 4.3 Relation between band gap (E_g) varies inversely proportional to dielectric constant (k_d)



by six orders of magnitude compared with SiO₂ [11]. Generally, a conventional high-k gate stack has a bi-layer system with high-k dielectric and interfacial SiO₂ to obtain the high quality of interfacial properties. In this case, interpretation of the electrical characteristic is rather complicated, which is discussed in Sect. 4.4.1.

4.3.2 Crystallization and Related Issues

4.3.2.1 Crystallization

An important issue to note is the crystallization of HfO₂ which induces large gate leakage current due to the leakage path along with grain boundary when it is crystallized after the thermal anneal. The ZrO₂-SiO₂ phase diagram [12] shown in Fig. 4.5 is well known and characterized in detail compared to the case for HfO₂.

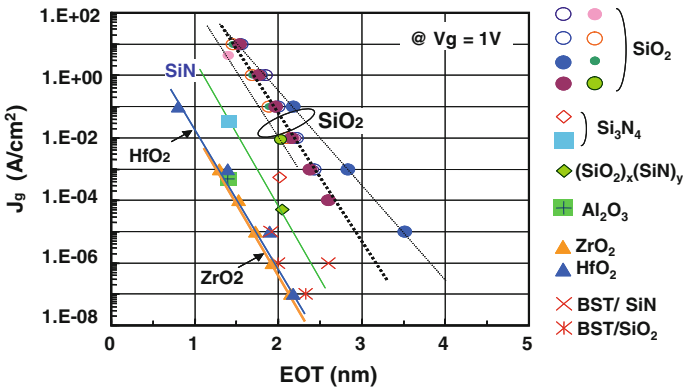
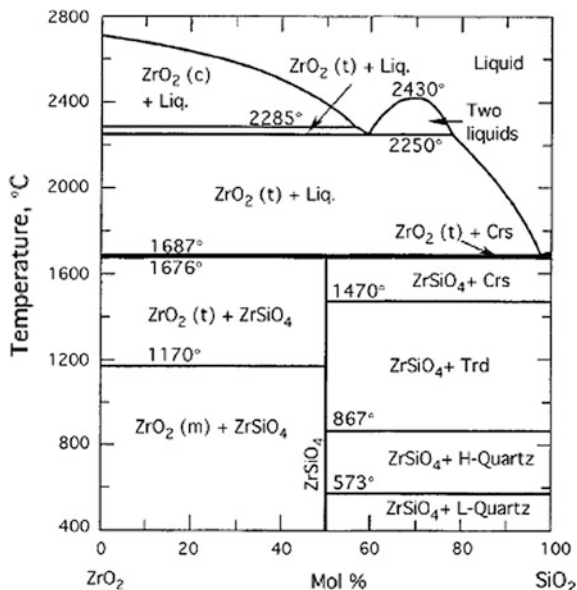


Fig. 4.4 EOT dependence of the gate leakage for various gate dielectrics

Fig. 4.5 Phase diagram of $\text{SiO}_2\text{-ZrO}_2$ system [12]

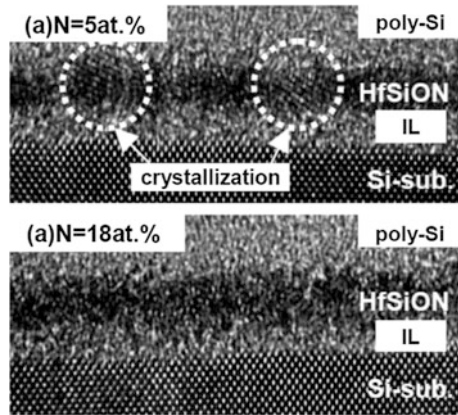


This is because very few reports are available on the phase diagram of $\text{HfO}_2\text{-SiO}_2$ at high temperature region. However, the $\text{ZrO}_2\text{-SiO}_2$ phase diagram can be used as a reliable phase diagram for $\text{HfO}_2\text{-SiO}_2$ system since Zr and Hf have very similar chemical behavior. It should be noted that the behavior indicated in the phase diagram is correct only in the closed chemical system and additional reaction have to be taken into consideration for the practical case which is an open chemical system, such as oxide transformation as well as competitive reaction between oxidation and silicidation. Using the metastable phase diagrams, the microstructure evolution during annealing of amorphous $\text{HfO}_2\text{-SiO}_2$ thin films for gate dielectric applications is studied and this evolution during annealing of amorphous $\text{ZrO}_2\text{-SiO}_2$ and/or $\text{HfO}_2\text{-SiO}_2$ thin films can be characterized by a low solid solubility, a liquid miscibility gap, and a kinetic barrier to the formation of the complex, crystalline silicate [13].

Nitrogen is often introduced to keep the amorphous state by preventing the crystallization. To avoid large gate leakage, nitridation is important to keep up the amorphous state in the HfSiO_x film against high temperature annealing. In case of poly Si electrode, this treatment is also effective for preventing boron in the electrode from diffusing into the Si substrate. Introduction of nitrogen is often accomplished by forming Hf-silicate. By optimizing the nitrogen content ([N]) in Hf-silicate, crystallization can be suppressed effectively.

Figure 4.6 indicates the cross-sectional TEM (XTEM) image of poly Si/ HfSiON /interfacial SiO_2/Si after activation annealing at 1,000 °C with respect to different [N]. At [N] = 5 at %, crystalline region is easily observed in the HfSiON which cannot be seen when [N] is increased to 18 at % due to an increase of Si-N

Fig. 4.6 XTEM image of the poly Si/HfSiON/interfacial-SiO₂/Si after activation annealing at 1,000 °C with respect to different nitrogen concentrations [14]



bond in the film. By increasing the [N], Weibull slope was confirmed to increase as well as the improvement of fluctuation of post-breakdown conductance [14].

Surface morphology by observing the crystalline domain is useful to understand crystallographic signature of HfO₂. “Nitrato” mentioned in Sect. 4.2.3, as an example, is CVD-HfO₂ and is deposited using the Hf(NO₃)₄ solid phase precursor on Si₃N₄ interfacial layer which is formed by a Rapid Thermal Nitridation (RTN). From X-Ray Diffraction (XRD) spectroscopy, the as-deposited 4-nm-thick HfO₂ film reveals amorphous phase and no crystal grains are observed by plan view TEM.

The grains begin to appear from elevated temperature at around 600 °C. Figure 4.7 indicates the in situ plan view TEM of “nitrato” observed after PDA (800 °C for 30 s in N₂) of the sample at 500 and 900 °C in Ultra High Vacuum (UHV), revealing approximate grain sizes of 8 nm for the sample annealed at 900 °C. The film thickness observed by ellipsometry before and after the PDA, indicates clear densification of the film as shown in Fig. 4.8.

Fig. 4.7 In-situ plan view TEM of the CVD-HfO₂ (“nitrato”), deposited on Si₃N₄ interfacial layer by Hf(NO₃)₄ solid phase precursor, observed after PDA (800 °C for 30 s in N₂) at 500 and 900 °C in UHV

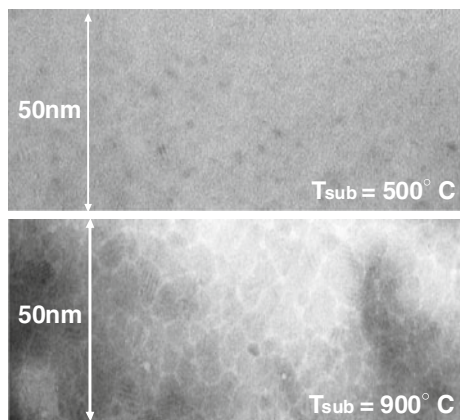
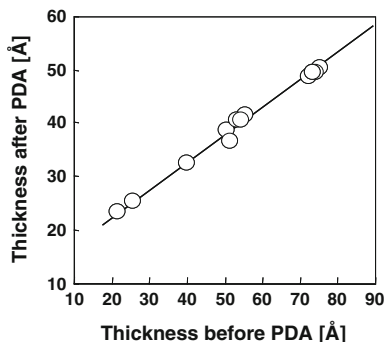


Fig. 4.8 Thickness change of the CVD-HfO₂ (“nitrate”) before and after the PDA at an annealing temperature of 900 °C



4.3.2.2 Role of Nitrogen

Nitrogen incorporation is absolutely imperative from the points of not only preventing the crystallization of the bulk HfO₂ but also preventing various reactions at Hf-based high-k gate dielectric film as well as phase separation of the Hf-based bulk material. The amorphous state in HfSiO_x film against high temperature annealing can be kept up by plasma nitridation and annealing under the NH₃ ambient, i.e., HfSiO_x with PDA (NH₃ treatment under 600 °C).

A nitride layer between the poly silicon gate and HfSiON is well known to be capable of preventing Hf from reacting with Si and Boron in the p+ poly Si from diffusing into Si substrate. This is going to be discussed in detail in Sect. 4.4.4. For this purpose, plasma nitridation and/or annealing under the NH₃ ambient are common techniques.

In case that the nitrogen is incorporated into the bulk HfSiO_x, the dielectric constant is effectively increased and even after high temperature annealing at 1,100 °C, the high permittivity value is maintained as shown in Fig. 4.9. Also boron penetration from poly Si is effectively suppressed in the HfSiON. As illustrated in Fig. 4.10, these properties are ascribed to the homogeneity of the bond structure in the film [15]. As described in the previous section, in contrast to the HfO₂, the HfSiON can avoid silicidation with Si substrate and retain a higher k value than HfSiO_x. The interface property of the HfSiON can be improved by plasma oxidation, which leads to higher drivability [16].

Incorporation of nitrogen also induces a benefit for metal gate processing. It is confirmed, by a comparison with La capped HfSiON and HfSiO, that nitrogen has a role to prevent La from diffusion into the high-k whereby an interaction of La with HfSiON/SiO₂ is less than that with HfSiO/SiO₂ [17]. Thus, nitrogen incorporation is believed to improve the thermodynamic stability [18].

However, care should be taken for the nitrogen incorporation from a device characteristics viewpoint. Nitrogen incorporation influences the channel mobility, which is remarkable for PMOS due to remote coulomb scattering. Therefore, nitrogen should be located away from the channel and the content should be optimized in order not to degrade hole mobility as well as NBTI (Negative Bias

Fig. 4.9 Dielectric constant after annealing at 1,000 °C

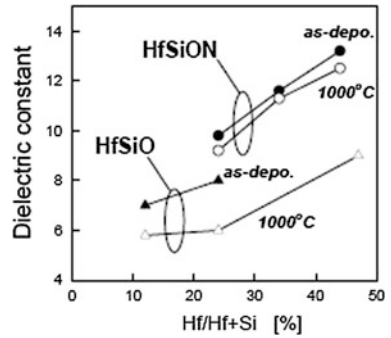
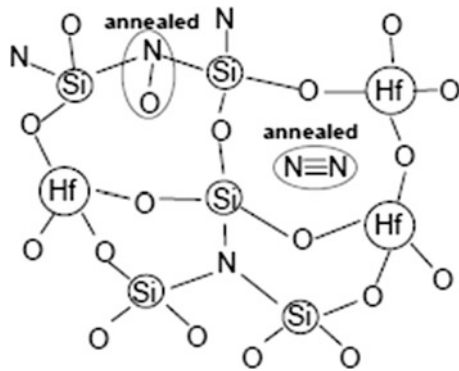


Fig. 4.10 Schematic of bond configuration before thermal annealing

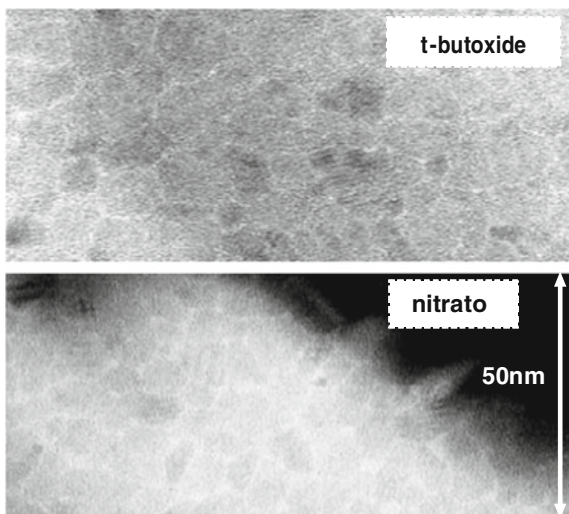


Temperature Instability). Also, the gate leakage tends to increase due to the smaller band-gap when nitrogen is incorporated in large quantity. Nitrogen with an optimum content (3–6 at %) in the MOCVD-HfSiON was found to be a key parameter to obtain thin EOT of 0.8 nm for CMOS with Ni-FUSI (Fully Silicided) gate [19]. How to incorporate nitrogen into the Hf-based high-k gate dielectric is a key issue and a variety of approach has been reported in addition to plasma nitridation and NH₃ annealing. These include direct formation of HfON, deposition of a nitride layer such as SiON and/or SiN onto HfO₂, and adding other element such as Al, Si, Zr to form HfAlON, HfSiON, and HfZrON or HfZrO [20]. The Zr doping technique is taken up in Sect. 4.3.5.

4.3.3 Thermal Treatment and Interfacial Reaction

In relation to crystallization of the bulk of Hf-based high-k material, it is important to control the high-k gate stack interfaces. Not only prevention of crystallization but also its phase separation and inter-diffusion during thermal processing are critical issues. Reaction at the bottom interface, i.e., interface between high-k and interfacial layer on Si substrate (IL), is discussed as well as the control of the top

Fig. 4.11 In-situ plan view TEM image of the CVD-HfO₂ prepared from different precursors (Hf-t-butoxide and Hf-nitrato) after annealing at 900 °C



interface reaction. Difference in the solid state properties due to different precursors (Hf-t-butoxide vs. Hf-nitrato) is discussed here [21].

Hf-nitrato, a CVD-HfO₂ produced from the Hf(NO₃)₄ solid phase precursor as described in Sect. 4.2.3 is denoted as “nitrato”. In contrast, a CVD-HfO₂ film denoted as “t-butoxide” is formed as follows. After RCA cleaning and diluted HF dipping, a HfO₂ film is deposited using the Hf(OC(CH₃)₃)₄ [Hf “t-butoxide”] precursor at 500 °C with O₂. This film was treated under PDA at 800 °C for 30 s in N₂, followed by poly-Si deposition with phosphorus implantation and activation annealing at 900 °C in N₂. All CVD-HfO₂ films are deposited on the Si₃N₄ interfacial layer prepared by RTN on Si substrate. As is seen in the Fig. 4.11, similar grains are observed in these samples after the 900 °C anneal and no specific difference is observed. However, the solid state properties of these films seem to have different features. The HfO₂ is prepared by “t-butoxide” (4.1 nm) and “nitrato” (3.2 nm). Figure 4.12 illustrates the Medium Energy Ion Scattering (MEIS) spectra of these HfO₂ after PDA (800 °C in N₂). From these figures, thickness of the HfO₂ from “t-butoxide” is found to be thicker than that from the “nitrato”. And near the top surface, a gentle slope is observed in the Hf spectra for the “t-butoxide” indicating out-diffusion of Hf and, from the small surface peak in the Si spectra, out-diffusion of Si is observed for the “nitrato”.

In-situ cross-sectional TEM (XTEM) images of these HfO₂ films are investigated as a function of the annealing temperature from room temperature to 860 °C in UHV. The diffusion of Hf into the interfacial layer is clearly observed by the in situ XTEM for the “t-butoxide” as shown in Fig. 4.13, where a new inter-diffusion layer is generated as a result of inter-diffusion of Hf and Si. The hydrogen is supplied from the CVD source of Hf(OC(CH₃)₃)₄ and the desorption of hydrogen from the film occurs at ~700 °C resulting in the inter-diffusion of Hf and Si. And inter-mixing of these elements is enhanced by the vacancy evolution

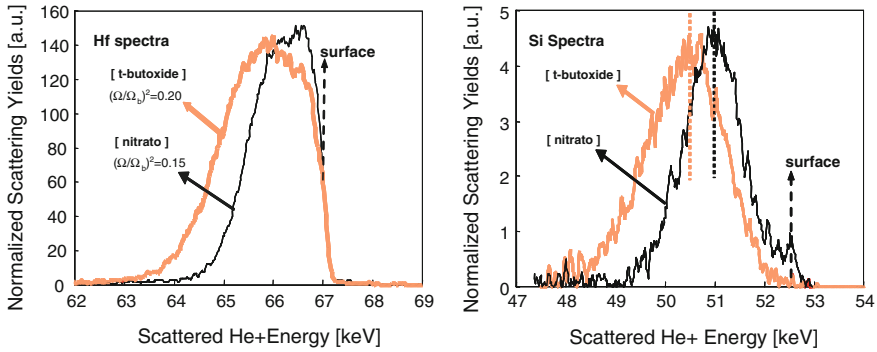


Fig. 4.12 MEIS spectra of the HfO₂ after PDA (800 °C in N₂)

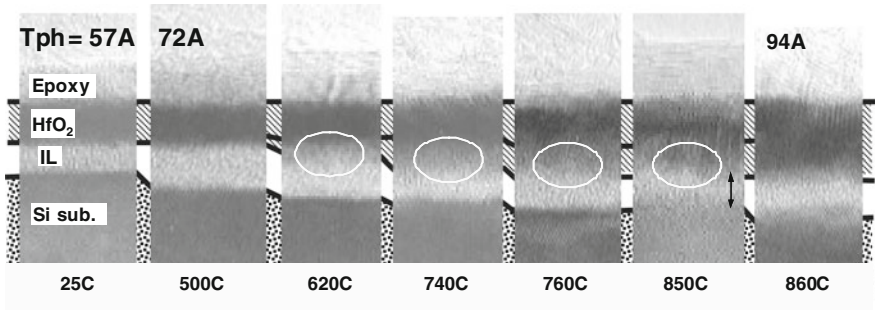


Fig. 4.13 In-situ XTEM images of CVD-HfO₂ by Hf-t-butoxide on 0.8 nm-Si₃N₄/Si substrate as a function of annealing temperature from room temperature to 860 °C in UHV

during the PDA. The oxidation of the Si substrate is observed at even low temperature regime (<500 °C). Gray layer indicated by circles appears in between the HfO₂ and the interfacial layer (IL) above 620 °C. This layer results from Hf diffusion toward the substrate. With elevating temperature, the thickness of the upper dark layer is increased with decreasing interfacial layer (IL) thickness. These diffusion reactions lead to a thinner EOT of the high-k stack. In case of “nitrate”, as is shown in Fig. 4.14, the inter-diffusion of Hf and Si at temperature range above 620 °C is small and the thickness of the IL at higher temperature increases apparently compared to the “t-butoxide”. This thicker IL of the “nitrate” due to less inter-diffusion leads to a large EOT.

Due to the inter-diffusion, in general, it is difficult to decrease the EOT. The inter-diffusion observed for the sample in Fig. 4.13 is caused by oxygen diffusion and additional oxidation during the conventional thermal process. The minimum EOT can be evaluated by the theoretical equations including densification of the film and the oxidation of the Si substrate as well as Hf diffusion into the interfacial layer [22]. Along with experimental results with poly-Si, the calculated results indicate that the minimum EOT of 1.1–1.2 nm exists at 3.0 nm of physical

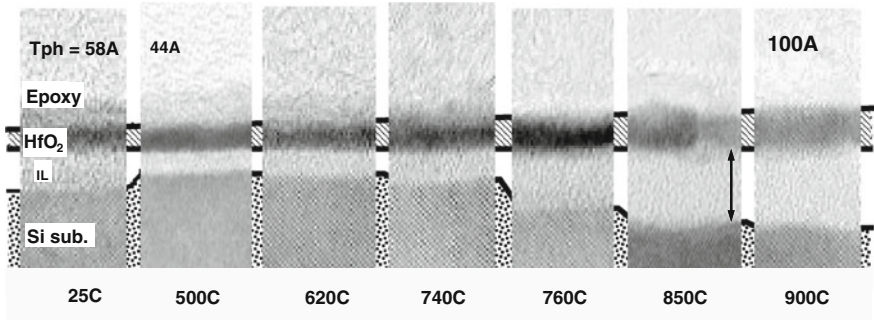


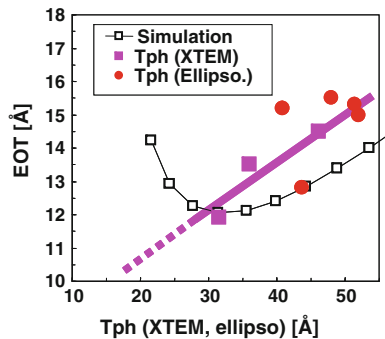
Fig. 4.14 In-situ XTEM images of CVD-HfO₂ by Hf-nitrato on 0.8 nm-Si₃N₄/Si substrate as a function of annealing temperature from room temperature to 900 °C in UHV

thickness of CVD-HfO₂ (“t-butoxide”) as shown in Fig. 4.15. This implies that even though the physical thickness is reduced, it is difficult to reduce EOT due to the oxygen diffusion and the additional oxidation during the conventional oxidation process unless effective countermeasure to prevent such oxygen behavior is implemented. The partial pressure of the residual oxygen should be controlled rigidly to obtain smaller minimum EOT during fabrication.

An Important issue to note is the influence of interfacial degradation on the electrical characteristics. To understand this, “t-butoxide” and “nitrato” were considered. Figure 4.16 indicates the leakage current characteristics as a function of EOT with respect to three types of capacitor structure; A: TiN/HfO₂/Si₃N₄/Si, B: Poly Si, TiN/HfO₂/SiO₂, Si₃N₄/Si, C: Poly Si/HfO₂/SiO₂/Si. It is noteworthy that the leakage current increases with decreasing EOT. And they have minimum EOT depending on the structure.

This phenomenon is roughly interpreted as an interfacial degradation. For the type A sample, no minimum EOT is observed indicating no interfacial reaction. Meanwhile for the type B, an interfacial reaction at least one side of the interfaces seems to occur, which induces large gate leakage. This interfacial reaction happens for both top and bottom interfaces of the HfO₂ [23]. Each sample configuration is illustrated in the right hand side where wavy lines stand for interface reaction. The

Fig. 4.15 Relationship of EOT and physical thickness for CVD-HfO₂ (“t-butoxide”). According to simulation, minimum EOT was found to exist as ~ 1.2 nm at around 3.0 nm of physical thickness



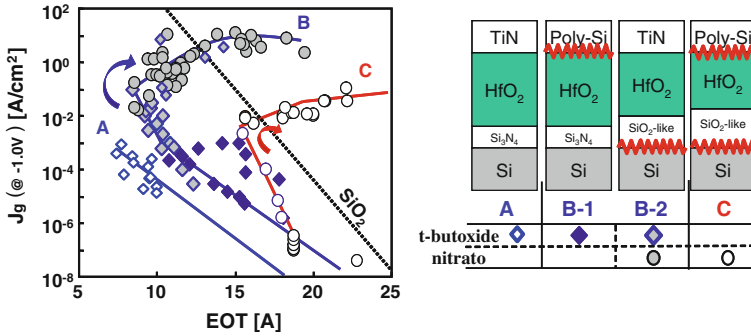


Fig. 4.16 *Left* Leakage current density (J_g) characteristics as a function of equivalent oxide thickness (EOT). *Right* Corresponding sample configurations

corresponding sample with respect to each CVD-HfO₂ film (“t-butoxide” and “nitrate”) is denoted at the bottom of the right hand side. In type B, two types of reactions (B-1, 2) are possible.

Verification of the interfacial reaction is performed by cross-sectional TEM (XTEM). Figure 4.17 indicates cross-sectional view of poly-Si/CVD-HfO₂ (“t-butoxide”)/IL/Si after annealing in N₂ at 900 and 1,150 °C respectively. The interface annealed at 900 °C apparently revealed smooth interfaces compared to the case at 1,150 °C annealing. The HfO₂ film became discontinuous by diffusion of Si atoms from poly-Si, possibly caused by the grain boundaries in the HfO₂. This Si diffusion from poly-Si through the grain boundaries results in an epitaxial growth of Si. This discontinuity of the HfO₂ causes the electrical breakdown. According to detailed analysis, at least two types of different extrinsic defects in the HfO₂ are found to exist. The first one is due to the defects which cannot be seen in the image generated by the impurity in the bulk HfO₂ and roughness at both the interfaces or indirectly related to the grain boundary. The defect density is roughly estimated as $1.5 \times 10^3 \text{ cm}^{-2}$ which may induce gate leakage. The second one shown is directly related to the grain boundary. The defect density for the latter case is around $2\text{--}8 \times 10^3 \text{ cm}^{-2}$, which is the direct evidence of the electrical breakdown [24].

Also, specific structural factor which influences reliability of the CVD-HfO₂ (“t-butoxide”) is considered as an example [24]. By means of theoretical calculation on the diffusion phenomena in the film, behavior of the out-diffused Si concentration into the HfO₂ is studied based on the reactions of oxidation and diffusion of Si. The oxidation happens at the Si substrate surface and Si within the oxidized layer can out-diffuse by a fundamental diffusion process even though the physical thickness is thin enough. In Fig. 4.18, the Si concentration of the calculated results and the experimental results observed by XPS are plotted. Small deviation near the interface implies the presence of SiO_x and a gentle slope for the HfO₂ film with Si nitride underneath indicates suppressed diffusion of Si compared to the case without the SiN layer.

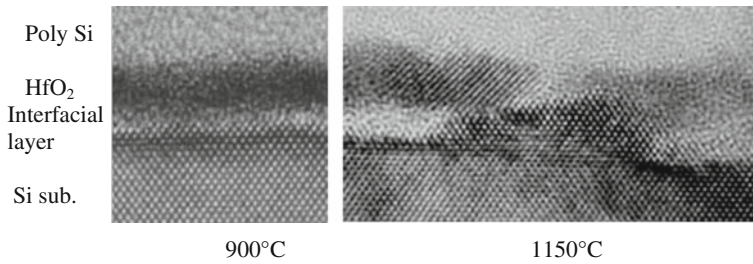
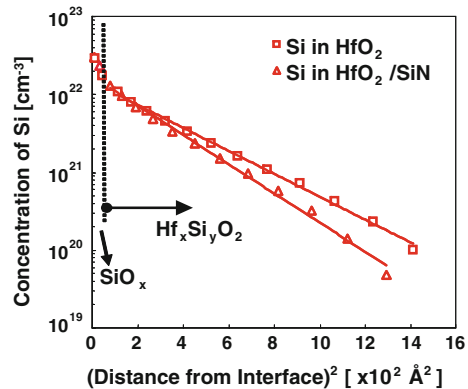


Fig. 4.17 Cross-sectional view of poly Si/CVD-HfO₂ (“t-butoxide”)/IL/Si after annealing in N₂ at 900 and 1,150 °C respectively

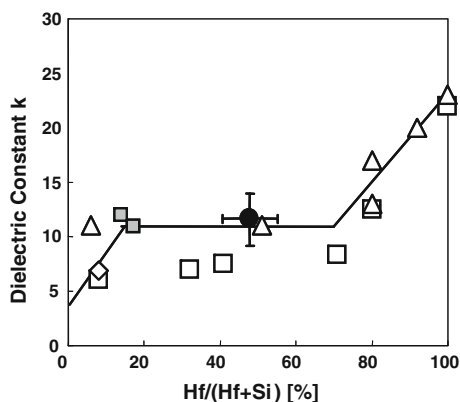
Fig. 4.18 Experimental results on Si concentration in the CVD-HfO₂ (“t-butoxide”) with and without SiN layer underneath. *Solid lines* indicate calculated results from diffusion equation [24]



The dielectric constant k of Hf silicate as a function of the Hf ratio $[\text{Hf}/(\text{Si}+\text{Hf})]$ is a key issue for the electrical property of high- k gate stack. Relationship between the dielectric constant k and the Hf ratio $[\text{Hf}/(\text{Si}+\text{Hf})]$ as obtained by XPS and observed for Hf silicate is shown in Fig. 4.19. The dielectric constant k is obtained by EOT divided by the total physical Thickness (T_{ph}), EOT/T_{ph} . The k value increases rapidly at lower Hf concentration and stays constant afterwards, and then it increases again for higher Hf concentration.

According to the results in Figs. 4.18 and 4.19, depth profiles for Hf ratio and dielectric constant are estimated as shown in Fig. 4.20a. From the fact that good agreement is found between the experimental data and estimated result by adding “0.4 nm” to the EOT thickness estimated from the k values, interfacial layer with EOT of 0.4 nm is considered to exist in between the high- k dielectric and Si substrate. From Fig. 4.20a, it is clarified that the stoichiometrical composition, $\text{Hf}/(\text{Hf}+\text{Si})$ is found to be approximately 63 % and the center value of the dielectric constant denoted as “ k -transition” indicates approximately as $k = 17$. Although it is difficult to determine the location of the interface from the contrast in the XTEM images in Fig. 4.20b, the stoichiometric interface exists at approximately 1.2 nm and the k -transition locates at approximately 2.0 nm from Si substrate surface [24].

Fig. 4.19 Dielectric constant k for Hf silicate as a function of the Hf ratio $[Hf/(Si+Hf)]$ as obtained by XPS. The k value is obtained by T_{ph}/EOT [24]



The interfacial layer between high- k and Si substrate where the electric field is high enough is an important region because, in the high- k /SiO₂ bi-layer system, it determines the breakdown and reliability factors such as time to breakdown (T_{bd}), Weibull slope (β). This lower k layer is defined at the k -transition interface as shown in Fig. 4.20a. Different from the homogeneous mono-layer gate dielectric like SiO₂ where the breakdown is explained by the percolation model [25], the high- k bi-layer structure reveals complicated behavior. As an example, a physical thickness dependence of the Weibull slope (β) with the same EOT of the high- k dielectric stacked structure is considered. The high- k dielectric is assumed to consist of three layers, i.e., SiO₂ (IL), Hf silicate, and HfO₂ on the Hf silicate. And

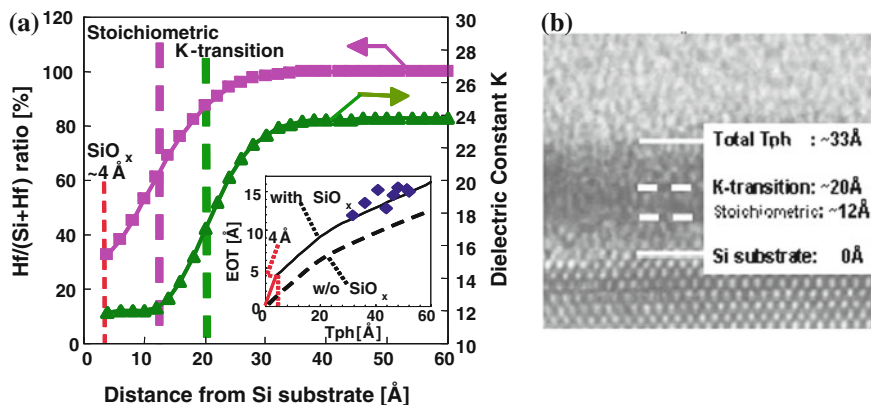
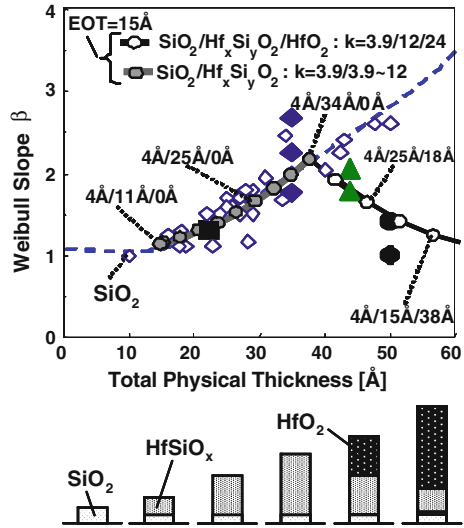


Fig. 4.20 Structural transition region at the *bottom* interface. **a** Hf ratio and k as a function of distance from Si substrate estimated from Figs. 4.18 and 4.19. By shifting the estimated EOT (*solid curve*) to fit to the experimental EOT (*diamonds*), a 0.4 nm thick-interfacial layer seems to exist at the interface. **b** XTEM image of CVD-HfO₂ (~ 3.3 nm). The interfaces of k -transition and stoichiometric SiO_x are located at ~ 2 nm and ~ 1.2 nm away from the Si substrate, respectively. The k -transition interface influences the reliability and is difficult to detect from the XTEM image

Fig. 4.21 Calculated relation between Weibull slope β and total physical thickness under the same EOT (1.5 nm) for a variety of gate stack combination of 0.4 nm-SiO₂, Hf silicate, and HfO₂, based on the data in Figs. 4.19 and 4.20. The Weibull slope has its peak for a structure consisting of 0.4/3.4/0 nm thick SiO₂/HfSiO_x/HfO₂ stack

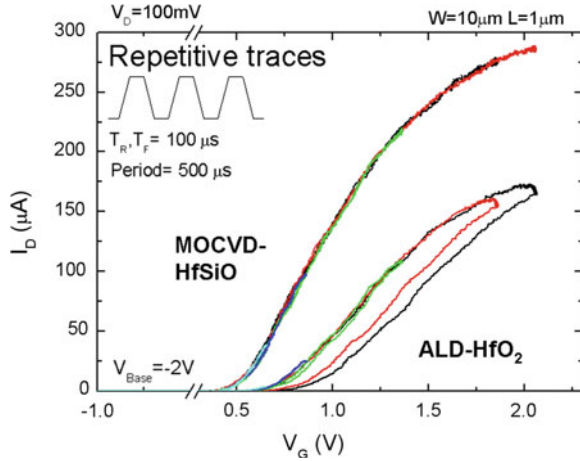


dielectric constant in each layer is assumed to be 3.9, 12 and 24, respectively. As indicated in Fig. 4.21, calculated physical thickness dependence of β under the same EOT (1.5 nm) for each structure is plotted together with other reported results. Here, it is assumed that β is dominantly determined by the distance between the k-transition interface and the Si substrate due to higher electrical field in the interfacial layer. Starting from SiO₂, the β increases with increasing physical thickness. Thickness configuration of each structure is changing from 0.4 nm (IL)/1.1 nm (Hf-silicate)/0 nm with $\beta \sim 1.1$ –0.4 nm/3.4 nm/0 nm where the β has the maximum value $\beta \sim 2.2$ at around total physical thickness (T_{ph}) of ~ 3.8 nm. The film at this point consists of a single layer silicate on SiO₂ as shown below. Then, it decreases with decreasing physical thickness of Hf-silicate due to crystallization of the HfO₂ layer. This phenomenon implies that the β can be improved by increasing the Hf silicate thickness without the HfO₂ layer and for thicker physical thickness regime, crystallization tends to occur with increasing HfO₂ thickness. From this analysis, it is clarified that the β can be improved by increasing the Hf silicate thickness without any HfO₂ layer, indicating that a single layer silicate is the best structure from the reliability standpoint.

4.3.4 Trapping Property

Although reliability is taken up in detail in Chap. 8, difference in trapping with respect to high-k formation process as well as its material (HfO₂ or Hf-silicate) is considered in this section since carrier trap is an intrinsic phenomenon for Hf-based high-k bulk material.

Fig. 4.22 Pulsed $I_d - V_g$ characteristics for NMOS (poly Si/HfSiO and HfO₂)



To understand the trapping behavior, a pulse $I-V$ measurement as well as charge pumping (ICP) are useful techniques [26]. For the FET with the SiO₂/Si system, NBTI (Negative Bias Temperature Instability) for PMOS is more relevant than PBTI (Positive Bias Temperature Instability) for NMOS. This is because PBTI is considered as electron trapping in high- k gate dielectric and thus insensitive to the SiO₂/Si system [27]. In comparison to HfSiON, HfO₂ reveals larger hysteresis at positive gate bias regime, indicating presence of larger number of electron traps in HfO₂ than HfSiON. This becomes serious with less N content as well as increasing of Hf content.

Figure 4.22 presents pulsed $I_d - V_g$ (drain current—gate voltage) characteristics for NMOS with poly Si and HfSiO or HfO₂, respectively, indicating significant large hysteresis for the HfO₂ and strongly reduced electron trapping in the HfSiO layer compared to the ALD HfO₂ in the $V_g > 0$ region.

Precisely, since HfO₂ is formed by ALD and HfSiON is by MOCVD, it is uncertain whether the electron trap is caused by the defects generated in HfO₂ material or by the ALD process. Figure 4.23 illustrates the $I_d - V_g$ characteristics for NMOS with HfO₂ formed by PVD (NH₃ pre-anneal/2 nm Hf(PVD)/Oxidation anneal/SiN cap/poly Si gate), indicating behavior similar to the ALD-HfO₂ baseline and no significant instability is measured for the p-FET ($V_g < 0$ region). From this result, it is conceivable that the origin of the huge hysteresis, i.e., electron trap, is caused by the Hf induced defect in the HfO₂ and not in the Hf-silicate and hole trapping is insignificant in the Hf-based high- k dielectric material. In addition, this trapping becomes remarkable with poly Si gate rather than metal gates.

It is interesting to see the chemistry between the gate electrode and the high- k dielectric material. Conventional technique to measure the charge trapping for high- k material is to measure the hysteresis by stressing and sensing the sample. However, in the presence of the transient charging effect (cf. Chap. 8), pulsed $I - V$ measurement which provides alternative fast measurement is necessary.

Fig. 4.23 Pulsed $I_d - V_g$ characteristics for NMOS with HfO_2 formed by PVD (NH_3 pre anneal/2 nm Hf (PVD)/Oxidation anneal/SiN cap/poly Si gate)

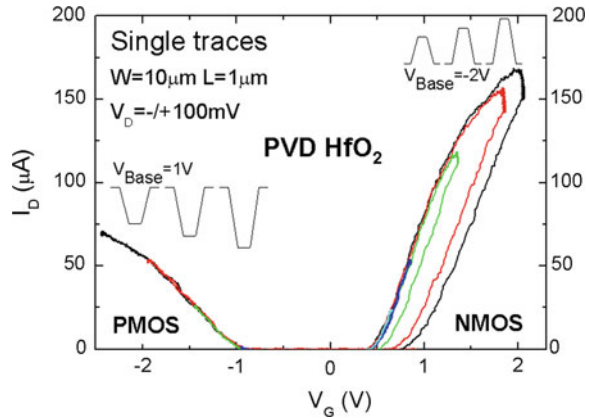


Figure 4.24 shows the pulsed $I_d - V_g$ characteristics for N- and PMOS with ALD- HfO_2 with TiN gate instead of poly Si. Electron trapping is negligible at small V_g and tends to be evident for $V_g > 1.5$ V. Compared to the result of ALD- HfO_2 with poly Si gate in Fig. 4.22, the drain current as well as the hysteresis are improved. This is due to the elimination of the depletion layer caused by the poly Si and less negative charge trapping in the bulk HfO_2 . On the other hand, when compared to the PMOS results in Fig. 4.23, strong positive charge trapping is observed for negative V_g . This behavior depends on the HfO_2 thickness indicating hole trapping in the bulk HfO_2 when TiN is formed on the HfO_2 gate dielectric.

Nitrogen effect is confirmed by the pulsed $I_d - V_g$ characteristics in Fig. 4.25. The capping SiN layer is formed under the condition of 600 °C, 15 s. Compared with ALD- HfO_2 result in Fig. 4.22, this indicates a certain level of reduction of the traps for NMOS. Considering the sweeping direction, the PMOS behavior is more complicated than NMOS, where trapping and detrapping co-exist indicating that positive and negative charge trapings are occurring.

4.3.5 Doping Effect

Attempt to dope some elements into HfO_2 to improve the device performance is a promising approach. Al doped into HfO_2 and ZrO_2 [28] was reported to improve its thermal stability as well as the Zr-Al mixed dielectric [29]. In addition, Si doping into HfO_2 , i.e., hafnium silicate (HfSi_xO_y) gate dielectric films, has indicated better electrical characteristics such as lower leakage, relatively thin EOT with no significant hysteresis, low mid-gap interface state density and high breakdown voltage. Cross-sectional TEM showed no signs of reaction or crystallization in the films being annealed at 800 °C for 30 min [30]. Beside this, fluorine is found to be effective to obtain higher work function (lower V_{th}) by inducing negative charge in the film for PMOS [31].

Fig. 4.24 Pulsed $I_d - V_g$ characteristics for N- and PMOS with ALD-HfO₂ and TiN gate

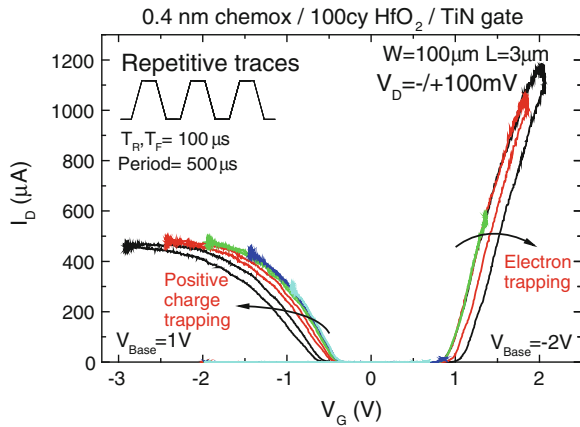
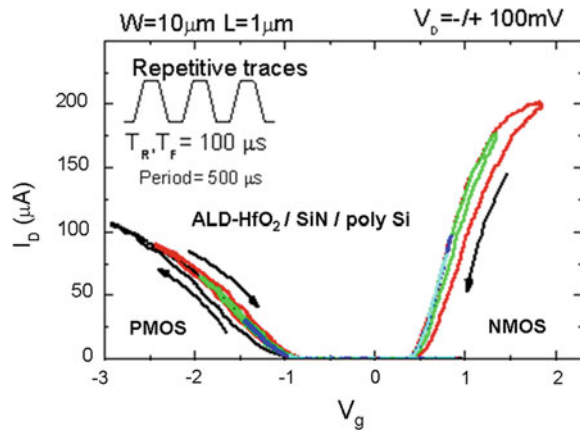


Fig. 4.25 Pulsed $I_d - V_g$ characteristics for FETs with 0.7 nm chemox/40 cy HfO₂/SiN (600 °C, 15 s)/poly Si structure



As an example, Zr doping is discussed here, in the quest to improve the reliability as well as its performance. A hafnium zirconate (HfZrO₄) alloy gate dielectric formed by ALD with tantalum carbide (Ta_xC_y) metal gate has been reported for advanced gate stack applications focusing on its dielectric properties, device performance, and reliability (Fig. 4.26) [32]. The HfZrO₄ dielectric film exhibits narrower band gap, smaller and more uniform grains, less charge traps than HfO₂ as well as good thermal stability with silicon. The HfZrO₄ gate dielectric is found to have smaller capacitance equivalent thickness (CET) owing to its thinner IL and higher k value as shown in Fig. 4.27, lower threshold voltage (V_{th}) and better reliability (with respect to charge trapping, C-V hysteresis, interface state density, and positive bias temperature instability) compared to HfO₂.

In this manner, the incorporation of zirconium dioxide (ZrO₂) into HfO₂ brings in a variety of advantages by enhancing the dielectric constant (k) of the resulting HfZrO₄ which is associated with structural phase transformation from mainly monoclinic to tetragonal (Fig. 4.28). The tetragonal phase has a higher k value as

Fig. 4.26 XTEM of hafnium zirconate (HfZrO_4) alloy and HfO_2 with Ta_xC_y gate dielectrics

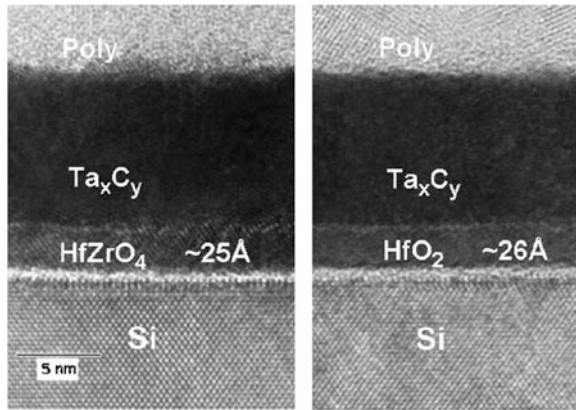
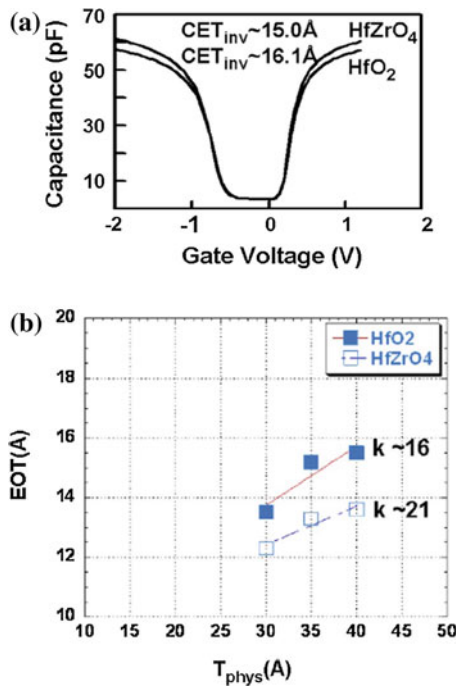


Fig. 4.27 CV curves and physical thickness dependence of EOT for HfZrO_4 alloy and HfO_2 gate stacks



predicted. The improved device characteristics are attributed to less oxygen vacancy in the fine-grained microstructure of the HfZrO_4 films. On the other hand, an issue of concern is the possibility of the presence of micro-crystals in the HfZrO_4 film, which will induce TDDB (Time Dependent Dielectric Breakdown) degradation. Also the electrical property of the HfZrO film as well as its microstructure depends on the thermal treatment method. The surface of the RTP (Rapid Thermal Processing) treated sample (1,000 °C, 5 s) has rough morphology, whereas, laser annealed

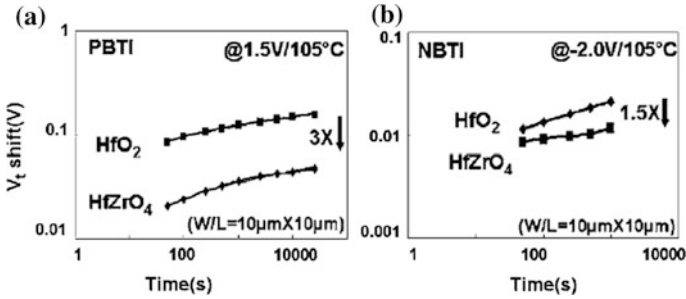


Fig. 4.28 BTI characteristics with respect to HfZrO₄ alloy and HfO₂ gate stack

(1,325 °C, spike) sample has smoother surface and improved electrical characteristics [33]. Further analysis will be necessary for this issue.

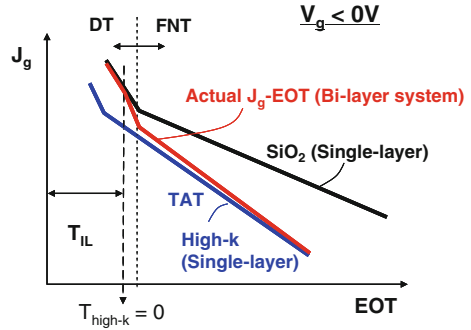
4.4 Device Processing of Hf-Based High-k FET/CMOS

In this section, based on the previous discussions, characteristic features caused by the bulk material property and the interface control, which are closely related to the reliability, are discussed. Reliability assessment in terms of device degradation including measurement techniques, lifetime prediction and other trap related issues is important. Pre-existing traps which are the seeds of generating traps in the HfSiON is found to affect strongly the negative bias temperature instability (NBTI) [34].

4.4.1 Bi-Layer System

It is important to understand the bi-layer system conventionally used for the high-k/metal gate stack. Gate leakage characteristics of the high-k dielectrics were introduced in Sect. 4.3.1. Generally, the actual high-k gate stack has the interfacial layer (IL) to realize the high quality interface. Figure 4.29 illustrates the relation between the gate leakage current density and EOT for single layer systems with respect to SiO₂, high-k dielectric, bi-layer structure of high-k and interfacial SiO₂. In case of the single dielectric system, when the physical thickness of the dielectric is rather thin, the gate leakage indicates a direct tunneling (DT) behavior across its thickness and for larger physical thickness, the tunneling current behaves as Fowler-Nordheim tunneling (FNT) which has a rather gentler slope than DT in the J_g -EOT relation. Since the band gap is narrower for high-k dielectric than SiO₂, the tunneling current shows trap assisted tunneling (TAT) by means of hopping conduction through the shallow traps in the high-k dielectric. In this way, the gate leakage behavior has a

Fig. 4.29 Gate leakage characteristics with respect to single layer and bi-layer structure with high-k and interfacial SiO₂ under V_g < 0 V



kink at a turning point of EOT between FNT and DT in the J_g–EOT relation and this feature is remarkable for the gate injection mode (V_g < 0 V). Black line indicates the case for SiO₂ and blue line indicates for high-k dielectric under single layer structure. In case for the bi-layer stack system with high-k and SiO₂, the leakage characteristic is rather complicated and may be interpreted as follows. The FNT is dominant at thicker EOT regime and in contrast, DT becomes dominant at around the turning point and tends to approach to the DT value of SiO₂ asymptotically at ultra-thin regime and finally it reaches to the DT leakage value of SiO₂ when the high-k gate dielectric thickness becomes zero (T_{high-k} = 0). This, as is discussed in Sect. 4.2.5, is due to the presence of an interfacial oxide layer.

In case of thin interfacial SiO₂ layer, the electrons are injected into the bulk HfO₂ creating defects [35]. Concerning the overall degradation mechanism for high-k/metal gate stack, it has been reported that SiO₂ interfacial layer is considered to control the degradation and breakdown under the inversion mode [36].

In addition to the leakage characteristics, combination of the HfO₂ and the interfacial oxide can also modulate threshold voltage of the transistor. The conventional hysteresis measurement presents a fast screening method to study high-k gate dielectrics. Figure 4.30 shows stress induced V_{th} shifts versus maximum Si field for various HfO₂ gate stacks with different interfacial SiO₂ thickness

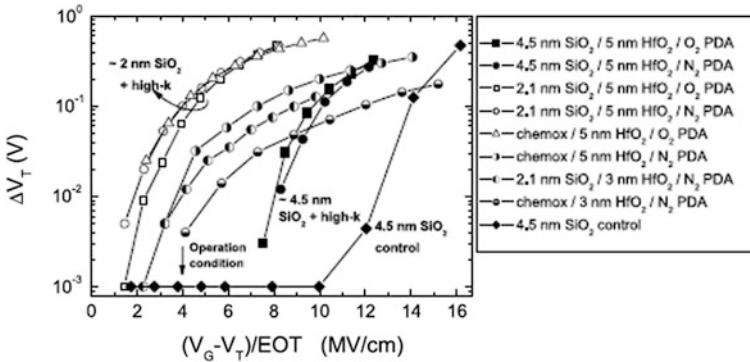


Fig. 4.30 Stress induced V_{th} shifts versus maximum Si field for various HfO₂ gate stacks with different interfacial SiO₂ thickness

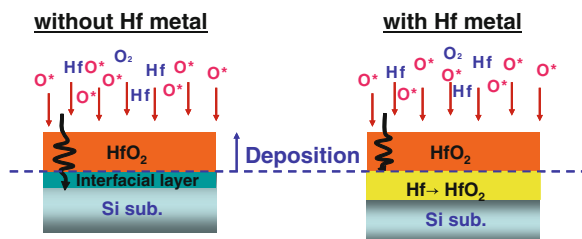
field for various HfO_2 gate stacks with different interfacial SiO_2 thickness. The results show the shift in the V_{th} strongly depends on the thickness of the interfacial SiO_2 as well as the HfO_2 layer. The V_{th} shift increases with increasing HfO_2 and decreasing interfacial SiO_2 thickness. The former is due to the increase of Hf content in the high-k. Regarding the interfacial SiO_2 thickness effect, it is explained by the injection of carriers by tunneling through the interfacial SiO_2 layer. For such a bi-layer system, both TDDB and mobility increase with increasing high-k thickness and interfacial oxide thickness. TDDB improves with increasing the high-k thickness under the same interfacial oxide.

4.4.2 Oxidation of Metallic-Hf

High-k deposition technique by oxidizing the metallic-Hf (mHf) is considered here. Combination of a metal sputtering and successive oxidation is a reasonable approach for fabricating the high-k gate stack with controlled interface and thickness uniformity across the wafer. The important advantages of the PVD method are its higher degree of purity and less water content in the film compared to the other methods.

In this section HfO_2/Si interface stability is studied for various oxidation processes [37]. HfO_2 films are prepared on p-type Si(100) substrates by two different methods, i.e., (1) 3.2 nm-thick Hf metal layer is deposited by DC sputtering using Hf target in Ar (0.5 Torr), followed by Rapid Thermal Annealing (RTA) for 60 s in O_2 (760 Torr) and (2) Hf metal layer of 0–2.6 nm is pre-deposited and 1.3 nm-thick HfO_2 is successively deposited by reactive sputtering in Ar/ O_2 (=50/50) as illustrated in Fig. 4.31. The pre-deposited Hf was oxidized by the exposure to the Ar/ O_2 plasma. The HfO_2/Si capacitors are fabricated using TiN or TaN gate electrodes [38]. Generally, thermal oxidation is achieved by oxygen diffusion at high temperature and facilitates crystallization. In contrast, plasma oxidation is performed by implantation of oxygen ion at low temperature, keeping an amorphous state. The Hf metal pre-deposition technique was studied to optimize the plasma oxidation conditions and to minimize CET [39]. The impact of Hf metal pre-deposition in CVD- and PVD- HfO_2 dielectrics was investigated [40]. As is illustrated in the figure, a deposition by reactive sputtering without the Hf metal layer on the Si substrate, oxygen species in plasma oxidize Si directly or through

Fig. 4.31 Comparison of the deposition method by PVD with and without pre-deposited Hf metal layer



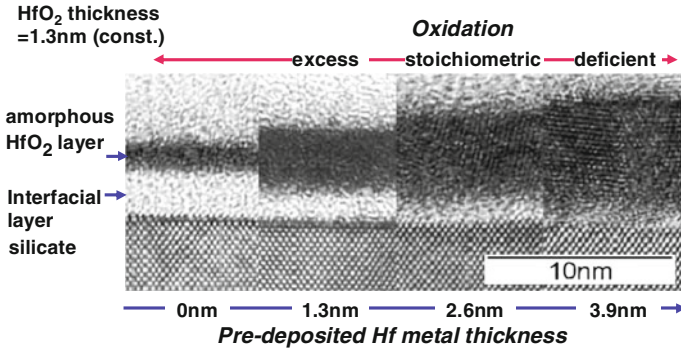


Fig. 4.32 XTEM images of the interface prepared by Hf/HfO₂ deposition

the HfO₂ layer during deposition, leading to a thick interfacial growth. In contrast, if Si substrate surface is coated with Hf metal, the oxygen species are consumed first to react with the pre-deposited Hf metal, therefore oxidation of Si is effectively suppressed. This indicates that Hf metal pre-deposition is an effective method to suppress the interfacial layer growth.

Figure 4.32 shows XTEM images of the interface prepared by the Hf/HfO₂ deposition. Target thickness of the HfO₂ is constantly 1.3 nm and pre-deposited Hf thickness is changed. At 0 nm when HfO₂ is directly deposited, a thick interfacial layer is formed. This thick layer is caused by an excess oxidation of the Si substrate. In case the Hf metal is pre-deposited, it is also oxidized in the amorphous phase and consequently the interfacial oxide layer growth is suppressed with increasing the Hf metal thickness. Thus, Hf metal pre-deposition is capable of minimizing the interfacial layer formation by limiting the amount of oxygen species available to interact with Si. In case of 3.9 nm Hf pre-deposited, the oxidation of Hf is deficient and metallic Hf remains. These observations are also confirmed by XPS analysis. From the image contrast and compositional data, the HfO₂ layer is considered to be amorphous and the interfacial layer is silicate.

Hf metal thickness dependence of electrical properties and thickness of each layer is shown in Fig. 4.33. The CET is found to have the largest value without the Hf metal pre-deposition, due to the thick interfacial layer. With increasing Hf metal thickness, the CET decreases dramatically, corresponding to the thickness reduction of the interfacial layer. For a further increase of the Hf metal thickness over 1.5 nm, the CET increases again, due to an increase of the total thickness of HfO₂. Thus, minimum CET is obtained at an optimum Hf metal thickness using plasma oxidation of Hf metal at low temperatures with amorphous HfO₂. Concurrently, the leakage current J_g is reduced for thin and thick Hf metal where the CET obtained is thick. It is plausible that the interfacial layer is a silicate ($k = 8$), which is conducted by the non-equilibrium nature and/or the mixing effect during plasma oxidation.

It is interesting to compare the electrical properties of the PVD and with the CVD HfO₂. Figure 4.34 indicates the relation between leakage current density J_g

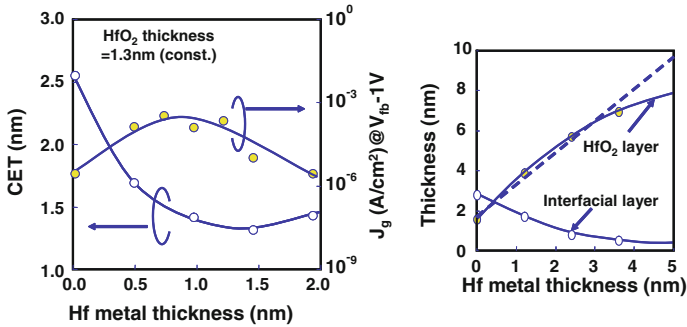
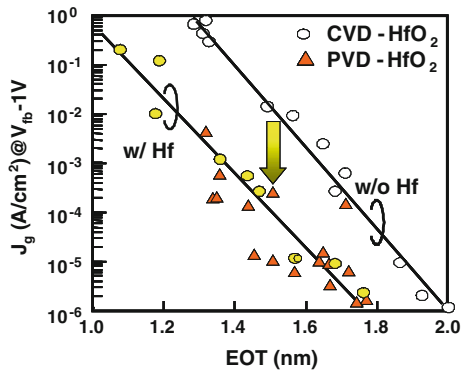


Fig. 4.33 Hf metal thickness dependences of CET, J_g , and thickness of each layer

Fig. 4.34 Relation between leakage current and EOT value with respect to each type of HfO₂



and EOT value with respect to each type of HfO₂. Effective reduction of J_g or EOT is achieved by the Hf metal pre-deposition method.

Figure 4.35 indicates the flat band voltage, V_{fb} , (left hand side) observed from the high frequency CV (capacitance–voltage) curve (right hand side). Compared to the CVD HfO₂ without the Hf metal layer, the PVD-HfO₂ has a larger flat band voltage and a larger shift. Also V_{fb} of the CVD-HfO₂ on Hf metal (denoted as filled circle) has values in between them. Large humps observed for the PVD-HfO₂ with Hf metal in the CV curve imply that this flat band voltage shift originated from the sputtering damage. Longer sputtering time for thicker HfO₂ films is likely to be more damaging. However, as shown in the V_{fb} characteristics (left hand side), this damage can be recovered by post metallization annealing (PMA; 650 °C for 30 min in N₂) to the similar level as that of CVD-HfO₂/Hf.

Although the above discussion relates to the case of HfO₂ deposition on Hf metal layer, a simpler approach is the direct oxidation of a pre-deposited metal Hf layer. Figure 4.36 illustrates a specific PVD formation method which consists of two steps [40]. First, by sputtering, pure Hf-metal is deposited onto Si substrate prepared by HF last treatment. As described above, the pure Hf-metal is deposited uniformly onto any surfaces with high density, and less water content. By using a

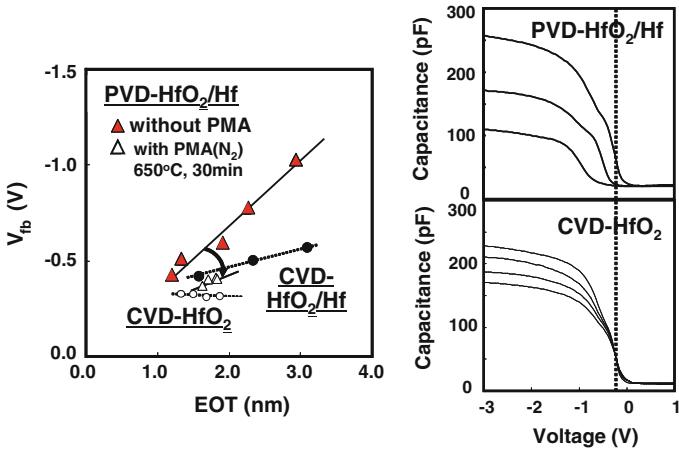


Fig. 4.35 V_{fb} and CV characteristics with respect to PVD- and CVD HfO₂ with and without Hf metal

pure Hf or HfSi target (5N grade), Hf or HfSi is deposited by co-sputtering. i.e., DC (Direct Current) sputtering in Ar under 400 Pa at room temperature. The second step is its oxidation to form HfO₂ by rapid thermal oxidation (RTO) or remote-plasma oxidation (RPO). For thick HfO₂, RPO is often used because of its higher deposition rate by a radical active oxygen [41].

Hf-metal can be oxidized uniformly by the oxygen radicals where Hf acts as a blocking layer to suppress the Si oxidation at low temperature. The HfO₂ thickness is determined by the pre-deposited Hf metal thickness and the interfacial layer can be adjusted by the RPO treatment time. This enables the gate stack structure to be optimized to achieve the best performance. As indicated in Fig. 4.37, the advantage of this method is that Hf can be easily and selectively oxidized when the oxidation temperature is chosen properly ($T = T_2$) where the oxidation rate is stable for both Hf and Si. In addition, the interfacial oxide layer thickness between Si substrate and HfO₂ layer can also be easily controlled by changing the RPO treatment time. Then, PDA is carried out at 650 °C for 15 min. As a gate

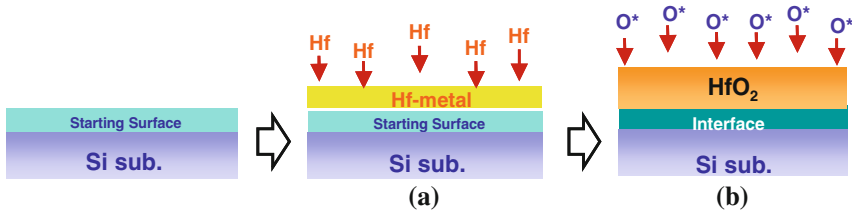


Fig. 4.36 PVD HfO₂ formation which consist of Hf-metal sputter (a) and remote plasma oxidation (b)

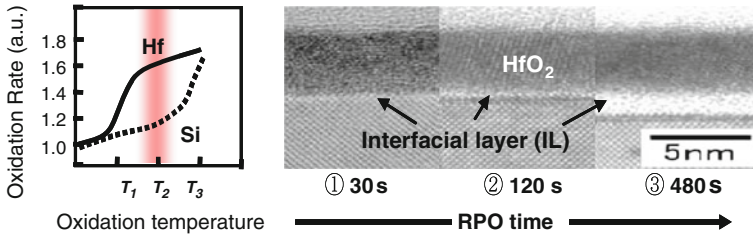


Fig. 4.37 Oxidation of pre-deposited Hf metal and precise control of the interfacial layer thickness by RPO

electrode, CVD-TiN is introduced. Similar electrical characteristics are obtained by this method. This systematic approach leads to a wider process window.

4.4.3 EOT Scaling

The gate stack scalability by the “Hf-metal sputter+RPO” technique is studied. As is explained previously, the interface thickness is controlled by the extended RPO time (Fig. 4.38). The RPO time dependence of EOT and leakage current density J_g for 3 nm-thick Hf metal are plotted in this figure. The pre-deposited Hf metal is selectively oxidized and then starts to grow during the extended RPO treatment time after complete oxidation of the Hf metal. Transistors using this technique are fabricated with a conventional self-aligned process flow up to Ni silicidation. Hf metal ranging from 0.5 to 3 nm is deposited on several kinds of starting surfaces pre-cleaned by HF-last followed by rapid thermal nitridation (RTN) and oxidation (RTO).

The deposited Hf metal was successively oxidized to form the HfO₂ layer increasing its thickness by a factor of 1.6 by RPO where oxygen radicals selectively oxidized the Hf at low temperature (400 °C). Poly-Si and source/drain activation treatment were performed under 1,000 °C for 3 s. The interface is controlled by the extended RPO time. Figure 4.39 presents plots of EOT versus the

Fig. 4.38 RPO time dependence of EOT and corresponding J_g for 3 nm-Hf metal

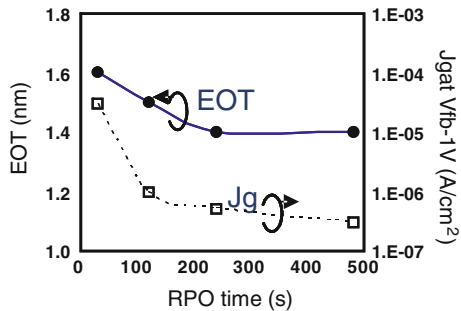
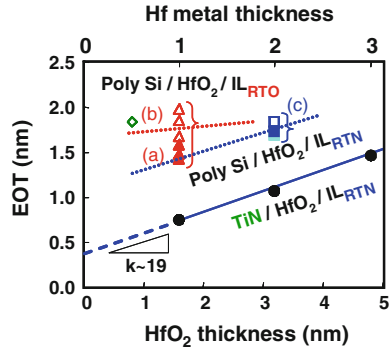


Fig. 4.39 Gate stack scaling by Hf-metal thickness change with respect to various combination of the interfacial layer (RTO and RTN) and the gate electrode (Poly Si and TiN)



physical thickness of HfO_2 with TiN gate, quoted from previous work [42]. From these results the k -value of HfO_2 is found to be $k \sim 19$ and the contribution of the interface turned out to be approx. 0.4 nm in EOT and from (4.1) in Sect. 4.2.5, the ratio of physical thickness of nitride interface and the interfacial k value ($T_{\text{phys}}(\text{IL})/k(\text{IL})$) turn out to be approximately 0.1.

However, under the poly-Si gate process, overall increase in EOT by ~ 0.5 nm occurred for the RTN interface, compared to the TiN gate, mainly due to an additional interface growth during the Poly-Si deposition or/and other possible reasons as discussed in Sect. 4.4.5. On the other hand, for the RTO interface, less EOT dependence on the HfO_2 thickness and a relatively thick EOT was observed in the thin Hf metal thickness region. This implies that an additional bottom interface growth and/or transformation into the silicate phase is enhanced in the thinner Hf metal regime for the RTO interface, compared to that of the RTN. Relations of EOT versus J_g (leakage current density) based on these scaling methods are plotted in Fig. 4.40. Apart from reducing of the bulk HfO_2 thickness, the EOT scaling has also been achieved by reducing the RPO time and/or introducing different types of the interface.

Fig. 4.40 EOT dependence of J_g for the scaled gate stacks with SiON reference and SiO_2 trend. The EOT scaling is performed by changing the RPO treatment time and/or different types of interfacial layer apart from thinning the bulk HfO_2

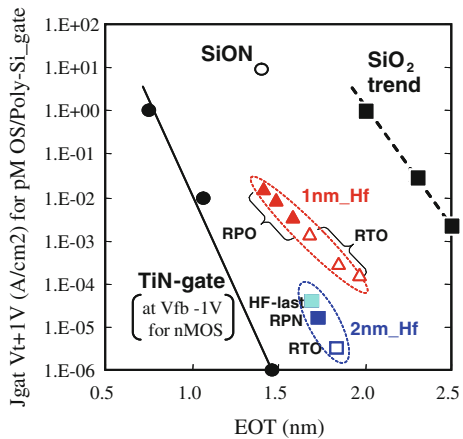
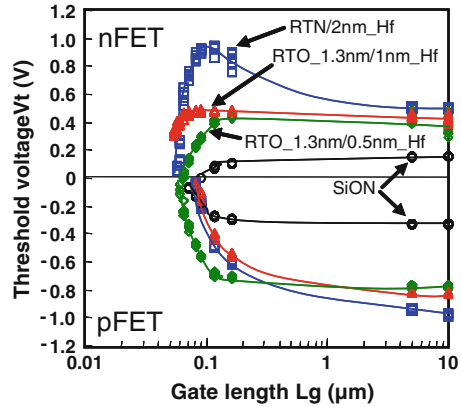


Fig. 4.41 Gate length dependence of the threshold voltage with respect to N- and P-MOS for various combinations of Hf-metal thickness and interfacial layer



In Fig. 4.41, V_{th} for the poly-Si gated FETs with a variety of gate dielectrics is plotted as a function of the physical gate length (L_g). As is seen in this figure, an anomalous V_{th} shift appears at around $L_g \sim 0.1 \mu\text{m}$ in addition to the normal short channel effect (SCE). Also, an anomalous V_{th} lowering appears for p-FET. These V_{th} roll-off for pFET and inverse roll-off for nFET tend to be pronounced with increasing the HfO_2 thickness. Assuming that negative fixed charges remain in the HfO_2 , these undesirable phenomena can be explained without contradiction and this is considered to be a main reason. Mechanical stress and/or Si-recess introduced during the gate fabrication may also influence these phenomena. The thick RTO interface is found to improve the V_{th} hysteresis to less than 10 mV and the $I_{on} - I_{off}$ characteristics can be optimized by tuning the RTO and the Hf-metal thickness to 1.3 and 1 nm, respectively [43].

4.4.4 Process Control

4.4.4.1 Bulk Process [44]

Suppression of the top interface degradation caused by the interfacial reaction between gate electrode and high-k gate dielectric is also a key issue, especially for the case when the metal gate is introduced. Improvement of the electrical properties, degraded by the interfacial reaction between HfO_2 and Ni-rich silicide for the metal gate/SiN/PVD- HfO_2 gate stack, is discussed in this section by introducing the ultra-thin nitrogen layer followed by optimization of the PDA condition. The high-k film is formed by sputtering of 1 nm-Hf metal on the 1.3 nm-RTO. The Hf metal is successively oxidized to form HfO_2 by RPO at 400 °C. A SiN cap is deposited after the PDA to suppress the interfacial reaction between the HfO_2 and the gate electrode. In this case, Ni-rich fully silicided (FUSI) gate is introduced as a metal gate electrode.

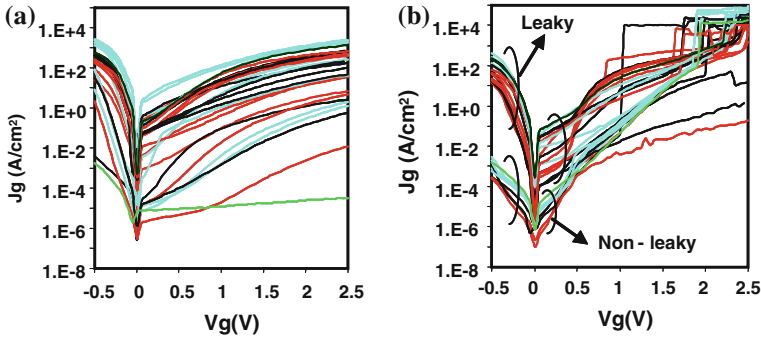


Fig. 4.42 $J_g - V_g$ of n-MOS capacitors for Ni-FUSI/(SiN)/HfO₂ gate stacks without SiN cap between FUSI and HfO₂ (a) and with SiN capping (b), after 700 °C PDA

Figure 4.42 shows the $J_g - V_g$ characteristics for the Ni-FUSI/(SiN)/HfO₂ gate stack after 700 °C PDA treatment. In the case without SiN capping, J_g is scattered over a wide range [(a) in this figure]; in contrast, two types of leakage modes are observed with the SiN cap: leaky part and non-leaky part as indicated in (b) of this figure. Similar dispersion is observed for the poly-Si/HfO₂ gate stacks without the SiN cap. On the other hand, the $J_g - V_g$ curves for poly-Si/SiN/HfO₂ gate stacks did not disperse so much (not shown here). From these results, SiN is found to have a role in suppressing the top interfacial reaction to some extent.

The PDA treatment strongly influences the WF by modulating the oxygen vacancy [45]. Comparison of $I_{on} - I_{off}$ behavior with respect to poly-Si or Ni-FUSI/SiN/HfO₂ gate stacks and with PDA at 700 °C is shown in Fig. 4.43. The poly-Si/SiN/HfO₂ results do not show data scatter; the $J_g - V_g$ curves had similar trend as well; in contrast, the data for the NiSi-FUSI gated transistors with the SiN cap revealed wide spread and in addition, some FETs do not work at all.

Possible explanation for this extraordinary spread in the $I_{on} - I_{off}$ characteristics, could be some micro holes in the flimsy SiN capping layer and/or roughness between the SiN and the HfO₂ layers formed during the processing. Some areas, which contain such holes or irregular thickness distribution due to roughness result in high leakage current whereas the other area without any holes nor roughness exhibit less leaky behavior (Fig. 4.44). Such undesirable issues can be suppressed by modifying the PDA condition which may change the surface roughness as well as the film quality. This can be performed by elevating the PDA condition and increasing the nitrogen pressure during the PDA. In order to confirm this hypothesis, structure of the interface is investigated with respect to conventional and new PDA treated samples. Since the SiN capping film is extremely thin (<0.5 nm), the film property is supposed to depend on the surface condition/roughness of the HfO₂.

The film quality was examined by elevating the PDA temperature from 700 to 1,000 °C. Figure 4.45 shows the XTEM images with respect to the conventional PDA condition at 700 °C and the new condition of 1,000 °C under rather high

Fig. 4.43 $I_{off} - I_{on}$ characteristics for n-FET with poly and or FUSI gate, and with SiN cap after PDA treatment at 700 °C

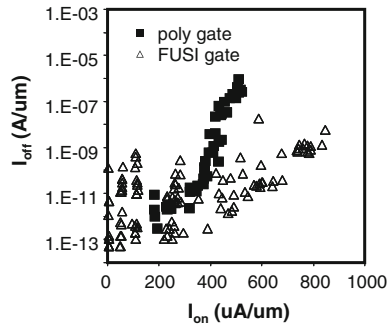
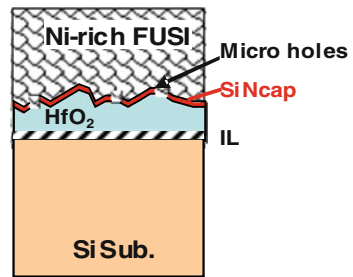


Fig. 4.44 A schematic representation of the flimsy SiN capping layer or roughness between the SiN layer and the HfO₂ to explain the spread behavior in the $I_{on} - I_{off}$ characteristics



nitrogen pressure. Although it is difficult to observe the direct evidence of such holes from the XTEM, some differences can be observed. As for the sample treated at higher PDA temperature (1,000 °C), an ultra thin layer indicated by the bright contrast is observed at upper interface, while this layer is not observable in the conventional PDA treated sample. The ultra-thin layer is considered to be a nitrided layer and the above dispersion in the $I_{on} - I_{off}$ can be explained. From these results, it is confirmed that the SiN capping at elevated temperature (1,000 °C) PDA condition is an important issue (Fig. 4.46). It should be noted that this argument is valid only when the FUSI gate is used. In the case of a pure metal such as TiN, since the interaction between gate and high-k layer does not happen, the SiN capping barrier is not necessary (see Fig. 4.16 in Sect. 4.3.3)..

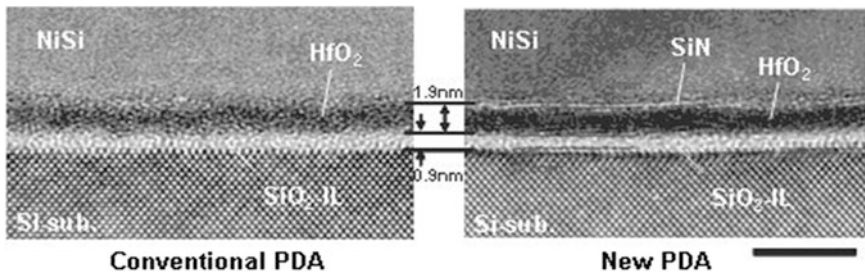


Fig. 4.45 XTEM image with respect to conventional PDA condition (700 °C in N₂) and new condition (1,000 °C in N₂)

Fig. 4.46 The $J_g - V_g$ characteristics of n-MOS capacitors with Ni-FUSI/SiN/HfO₂ gate stacks after 1,000 °C PDA

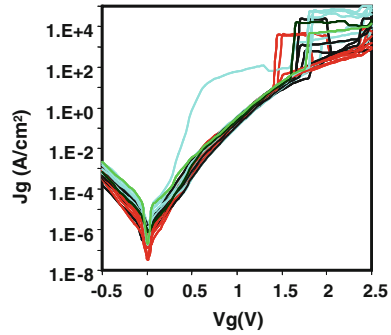
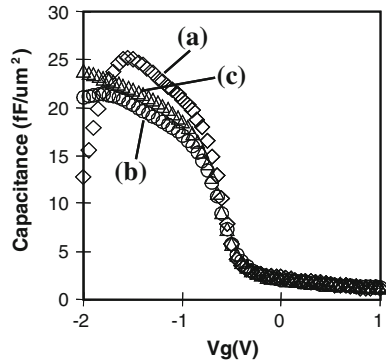


Fig. 4.47 CV of nMOS capacitors with NiSi-FUSI/HfO₂ gate stack: **a** w/o cap (EOT = 1.0 nm), **b** with SiN cap (EOT = 1.3 nm), PDA at 700 °C, while **c** with SiN cap (EOT = 1.2 nm), PDA at 1,000 °C

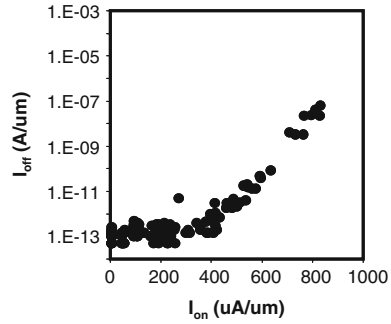


The EOT calculated from the CV curve of the Ni-FUSI/HfO₂ without the SiN cap is 1.0 nm and as is shown in Fig. 4.47; the EOT of Ni-FUSI/SiN/HfO₂ gate stacks after PDA is 1.3 nm for 700 °C treatment and 1.2 nm for 1,000 °C condition. As can be easily expected, the calculated EOT increases from 1.0 to 1.3 nm due to the SiN capping. The $I_{on} - I_{off}$ plots for the transistors with this elevated temperature PDA condition do not scatter as shown in Fig. 4.48 and the V_{th} has appropriate values. Thus, the $I_{on} - I_{off}$ characteristics of n-MOS transistors with Ni-FUSI/SiN/HfO₂ exhibit dramatic improvement due to the PDA optimization and SiN capping.

The carrier mobility is found to decrease a little by this treatment, however, the EOT is reduced by 0.1 nm (EOT = 1.2 nm). This EOT reduction can compensate the mobility degradation.

As discussed above, owing to these treatments, the gate leakage current is reduced and any splits in the $J_g - V_g$ curves are not observed. One more thing to note is that this wide dispersion can be seen for nFET rather than pFET. This implies that the dispersion is caused not only by the simple interfacial reaction discussed above but also a trap related issue which has polarity dependence. A different behavior might be observed for the Hf-silicate, due to a different charge trapping process [46].

Fig. 4.48 $I_{on} - I_{off}$ characteristics of nMOS transistors (NiSi-FUSI/SiN/HfO₂) treated by the new PDA condition (1,000 °C). Owing to SiN cap and PDA optimizations, higher drivability is obtained



4.4.4.2 Capping Process

Fully silicided (FUSI) gate is one of the promising candidates as a metal gate since this process is cost worthy because it can make use of the poly silicon facility and the work function can be well tuned depending on the degree of silicidation such as NiSi for NMOS and Ni-rich phase for the PMOS [47]. Furthermore, it may not necessarily suffer from the “ V_{th} roll-off” [48] seen for the gate first process Sect. 4.4.6.1. However, the shift of flat band voltage is not always enough for a band edge characteristic. In this respect, for the gate first process, a capping process is often introduced by slight doping of the material into the high-k dielectric to obtain the band edge work function with respect to N- and PMOSFET. Mechanism of this work function modulation has been discussed and considered as an electric dipole formation caused by the newly formed bond between Hf and the doping materials such as La for NMOS and Al for PMOS. This electric dipole moment produces a potential to modulate the initial work function. Figure 4.49 indicates the trends of V_{th} shift and areal density of oxygen atoms in various doped oxides [49]. The observed V_{th} shift for each oxide resulted in exactly the same trend as its areal oxygen density. This indicates that the oxygen density determines its direction and strength of the produced dipole as shown in Fig. 4.50. The oxygen moves toward lower density area leaving oxygen vacancy and this movement causes the electrical dipole. (The work function tuning is also discussed in Sect. 4.4.6.1.)

Figure 4.51 indicates a band diagram of the gate electrode (poly Si or metal)/high-k/IL/Si system for the case of the doped capping element. There are several factors to modulate the potential across the gate stack. Oxygen tends to move from high-k to poly Si, leaving the oxygen vacancy together with the electrical dipole at the lower interface which causes roll-off and due to the Fermi level pinning, the potential is modulated at the upper interface.

Also fixed charges in the high-k dielectric modulate the potential in the bulk according to Poisson’s equation. In case of the sheet charge distribution, the potential shape has a polygonal line (black solid line) and in case of uniform distribution, the band bends in a quadratic curve as indicated by the red line. Direction of the potential modulation is determined by the polarity of the charge in the high-k. This actual retrograded work function is called “Effective Work

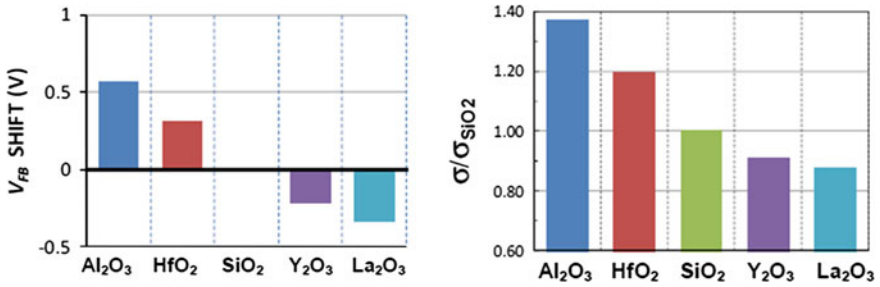


Fig. 4.49 Observed V_{th} shift (Left) and areal density of oxygen atoms (right) with respect to various oxide

Fig. 4.50 Formation of the electric dipole caused by oxygen transfer

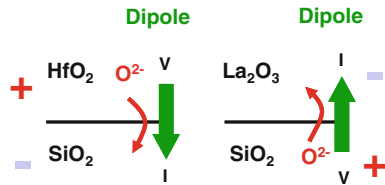
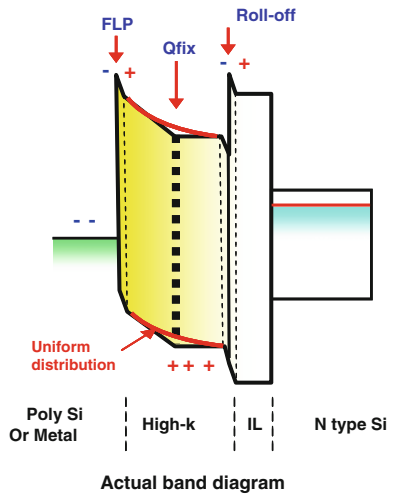


Fig. 4.51 Band diagram of gate/high-k/IL/Si system with capping material



Function (EWF)". How to locate the capping elements and retain them in the high-k dielectric against thermal treatment is a key issue for the "gate first process" and never for the "gate last process". The application of the capping layer for tuning the metal work function has been discussed in Chap. 5; the topic of the interface dipole has been analyzed in Chap. 6.

4.4.5 EOT Dependence on Gate Electrode

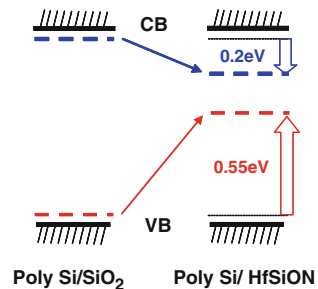
Along with the high-k dielectric, the gate electrode material is also a key issue for the high-k gate stack. Thanks to the intensive process development, in order to eliminate the depletion layer, pure metal gate is being introduced as the mainstream gate electrode by solving the various process problems. Study of the pure metal gate material is discussed in Chap. 5. In this section, gate electrode dependence on EOT is covered focusing on the interfacial reaction. And the fully silicided (FUSI) gate is considered as a metal gate electrode.

As is well known, when poly Si is used as gate electrode for Hf-based high-k gate dielectrics, Fermi level of both N- and P-type poly Si is pinned to a lower energy level approx. 0.2 eV below the conduction band edge and approx. 0.55 eV above the valence band edge, respectively, due to the Fermi level pinning (FLP) [50]. As is shown in Fig. 4.52, the pinning site is located more towards the CB side for both types.

For low power CMOS application, the effect of FLP at high-k/poly-Si interface strongly influences the device performance. The increase of threshold voltage due to the FLP leads to lower channel impurity concentration, which brings us better performance such as suppressed GIDL (gate induced drain leakage) as well as higher mobility. In addition, due to the mid-gap Fermi level (in other words, relatively higher threshold voltage) caused by the FLP, the electric field across the gate dielectric is effectively suppressed, hence the gate leakage current may be reduced [51]. By means of progressive application of FLP, the poly-Si/HfSiON gate stack is capable integration into the CMOSFET. This technique leads to suppression of the reverse narrow channel as well as superior cost performance [52].

It is worthwhile to understand the intrinsic phenomenon related to the interface between the gate electrode and the gate dielectric from the EOT-change point of view for metal gate and poly Si gate on the high-k gate dielectric. Figure 4.53 shows the CV curves for various combinations of gate electrode NiSi-FUSI [mono Ni silicide] indicated as “FUSI”, poly Si/nitride capping (denoted as “PS/SiN”) and gate dielectric (PVD-HfO₂ (denoted as “HfO₂”) and SiO₂) for both p- and nMOSFETs. Comparison of poly Si vs NiSi-FUSI/SiO₂ gate dielectric for pMOSFET is considered first. When the poly Si is replaced with NiSi-FUSI, the

Fig. 4.52 Fermi level pinning occurring at Poly Si/HfSiON



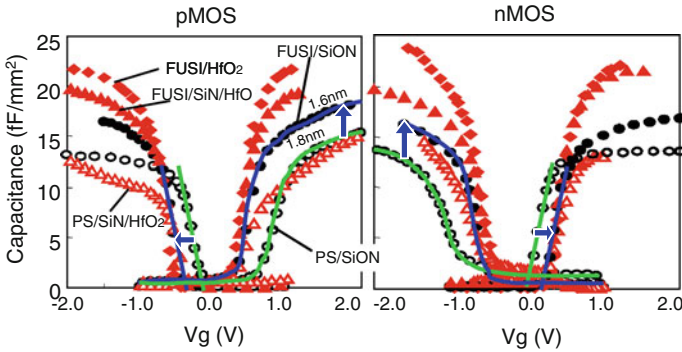


Fig. 4.53 Comparison between Poly Si and NiSi-FUSI on SiON among CV curves for a variety of gate stack: Ni-FUSI, Poly Si/(SiN)/SiON, and HfO₂ gate stack

EOT (under accumulation condition) obtained by Hauser fitting [53] decreases by 0.2 nm (from 1.8 to 1.6 nm) and CET (under inversion condition) by 0.5 nm. The reason is not yet well understood for this slight reduction in EOT which should not happen for both the gate electrodes. Concerning the CET reduction, considering the fact that the normal depletion layer thickness is approximately 0.3 nm, an additional unknown reduction by 0.2 nm seemed to exist under the inversion condition in addition to the depletion. Furthermore, the V_{th} is found to increase for FUSI/SiN/SiON. These results give an indication of the physical thickness reduction or changing of the k value of the SiON dielectric when the FUSI electrode is introduced. Further consideration is necessary to understand this mysterious phenomenon occurring in the PS, FUSI/SiN/SiON system.

On the other hand, changes in EOT and CET for the FUSI/SiN/HfO₂ seem to depend on the Hf concentration, i.e., density of Si–Hf bond at FUSI/SiN/HfO₂ interface. Figure 4.54 is the same as Fig. 4.53, but is focused on the HfO₂ dielectric with/without SiN capping (i.e., FUSI/(SiN)/HfO₂). In the case of SiN capped HfO₂, the EOT of PMOS decreases as well but by 0.5 nm (from 1.8 to 1.3 nm); in contrast, the V_{th} is found to be unchanged, which implies that it is not enough to unpin the Fermi Level Pinning (FLP) by the NiSi-FUSI [54]. For the case without the SiN cap, the EOT is decreased further by 0.7 nm (from 1.8 to 1.1 nm) and the corresponding V_{th} reveals unchanged value indicating NiSi-FUSI is not capable of unpinning the FLP regardless of the SiN capping on top of HfO₂. In case of Ni-rich FUSI electrode, the V_{th} can possibly be changed due to different pinning strength. Further reduction of the EOT by 0.2 nm (from 1.3 to 1.1 nm) is simply due to the absence of the SiN layer. Figure 4.55 indicates the possible phenomena for this “unexpected EOT reduction” [55]. Figure 4.55a shows the case when the interfacial reaction occurred at the upper interface for NiSi-FUSI gate stack. Due to a reaction at upper interface, EOT can be decreased. Figure 4.55b explains the case where an extra capacitance appeared due to a steep band bending caused by the FLP at upper interface for the case of poly Si gate

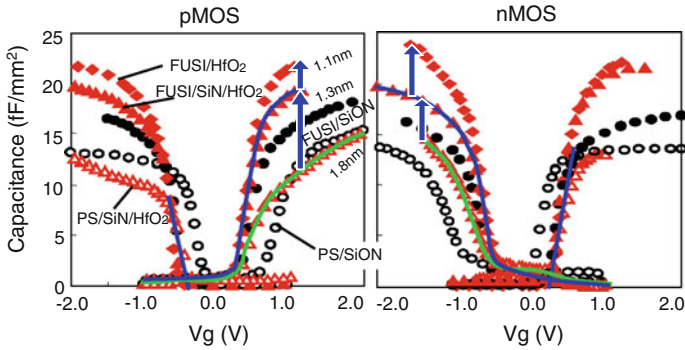


Fig. 4.54 Comparison between Poly Si and NiSi-FUSI on HfO₂ among CV curves for a variety of gate stack: Ni-FUSI, Poly Si/(SiN)/SiON, and HfO₂ gate stack

stack. Due to this additional capacitance, total C_{inv} is reduced, hence the CET increases. This hypothesis is contradictory to the CET decrease. However, this band bending caused by the FLP is likely to happen. These FLP related explanations can explain the unknown small EOT reduction for the NiSi-FUSI/HfO₂. However, these cannot explain the PS,FUSI/SiON stack. The third possible interpretation is the interface roughness as illustrated in Fig. 4.55c. Due to the roughness at the upper interface introduced during FUSI processing, the capacitance is increased, hence the EOT decreases. However, it is still open to question whether the total capacitance will increase by just increasing the roughness of one side of the electrode of the capacitor [56]. In any case, it should be noted that in addition to the poly depletion, an unknown additional reduction in EOT happens when the poly Si is replaced by NiSi-FUSI gate on SiON. Also the EOT reduction is more remarkable for HfO₂ gate dielectric than for SiON [54]. Although, these discussions related to the PMOS, similar trends are found for NMOS.

Apart from the complicated phenomena described above, accurate capacitance measurement including interfaces of the gate stack is necessary to obtain reliable EOT extraction and flat-band voltage shift [57]. Also, care should be taken for the flat-band voltage shift due to ionized dopant charge in the quantization layer [58].

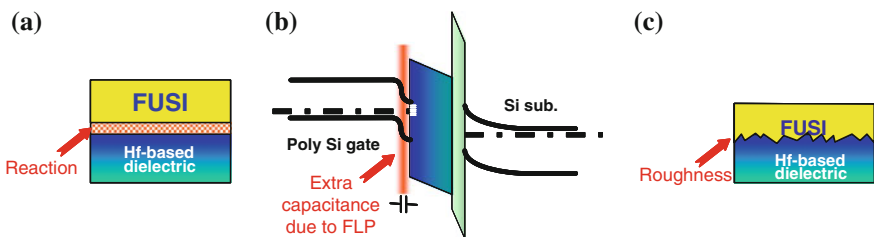


Fig. 4.55 Possible reasons for the unexpected EOT reduction

4.4.6 Influence of Processing on Device Performance

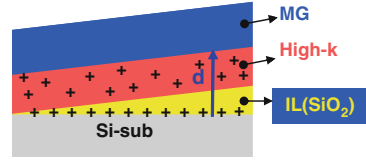
How will the intrinsic solid state property of Hf-based gate dielectric material such as crystallization and interfacial reaction influence the device performance? With aggressive scaling, the average channel electron energy increases and the electric field along the channel becomes stronger with the decreasing channel length. This leads to an increase of thermal noise of the carriers and flicker noise is generated by the trapping/detrapping behavior in the gate dielectric. The trap could be characterized by bias temperature instability (BTI) as well as $1/f$ and charge pumping (CP) measurement. The number of traps can be suppressed by introducing nitrogen into the gate oxide [59]. Furthermore, the carrier trapping becomes more serious when the high- k gate dielectric material is introduced. Number of the traps in the HfSiON for example is estimated to increase by three- to tenfold compared to those in SiO_2 , due to the increase of carrier trap centers introduced by Hf, which is enhanced by its relatively large physical thickness. Besides the process treatment, it is necessary to take measures to suppress the $1/f$ noise by appropriate layout modification for CMOS with high- k gate dielectric.

Nitrogen in the HfO_2 has a role to prevent its crystallization which leads to large gate leakage and Boron penetration into the channel as well as reliability degradation. It is demonstrated that when nitrogen is introduced into HfO_2 , the HfSiON (N = 20 %) obtained stays amorphous and keeps the high permittivity value even after a 1,000 °C anneal [15]. Also, by introducing the HfSiON, device function has been demonstrated with gate length of 50 nm and EOT of 1.2 nm by preventing silicidation at the bottom interface. Thanks to its higher k value with nitrogen, low gate leakage was achieved [60].

4.4.6.1 Work Function Control

From the device performance point of view, the threshold voltage (V_{th}) control is a crucial issue. For the gate first process, it is extremely important to control the oxygen vacancy behavior in the bulk HfO_2 . This is because the amount of oxygen (or oxygen vacancy) in the bulk HfO_2 modulates the work function and the oxygen amount is strongly influenced by the CMOS integration process. In order to control the V_{th} , optimization of the channel implantation condition as well as well implantation is a common maneuver. When the channel impurity concentration (N_{ch}) becomes higher, the V_{th} becomes larger; in contrast, short channel effect (SCE) will be a problem when N_{ch} is too low. In case of high- k gate stack, the V_{th} is fixed at a rather higher value due to the “Fermi level pinning” (FLP) [50]. In order to suppress the V_{th} values against the FLP, the N_{ch} should be as low as possible. This can also be achieved by non-doping or counter doping. This treatment, however, requires a reformation of the halo/extension implantation condition which leads to transistor performance degradation. And to make the

Fig. 4.56 Sample structure by the slant etch technique



matter worse, an immature dry etching during the gate patterning of high-k/metal gate stack makes this problem more complicated.

As discussed in Sect. 4.4.5, the “FLP” leads to flat band voltage shift. Due to the interfacial states at the PS/HfO₂ interface caused by the Hf–Si bond, an electrical dipole is formed at the interface which modulates the V_{fb} . And the strength of the dipole (dipole moment) is expressed by the fixed cation (+Q), anion (–Q) charge and the distance (d) between them. The dipole moment is expressed by the product of each value, “Qd” [61]. As shown in Fig. 4.56, the EOT can be changed intentionally by changing the interfacial oxide layer (IL) thickness, which is often called the slant etch method.

The measured flat band voltage V_{fb} could be expressed as an intrinsic flat band voltage and an additional potential ΔV_{fb} caused by the fixed charges density Q_{fix} in the high-k dielectric, which varies quadratically with the distance from the substrate surface, d as expressed in the following equations where S indicates the area of the corresponding electrode and κ is the permittivity of the dielectric.

$$V_{fb}(\text{measured}) = V_{fb}(\text{intrinsic}) + \Delta V_{fb}(Q_{fix}) \quad (4.2)$$

$$\Delta V_{fb} = dQ_{fix}/S\kappa + (1/2)d^2Q_{fix}/S\kappa \quad (4.3)$$

To obtain the intrinsic V_{fb} in the real device, the slant etch experiment is often introduced. Figure 4.57 shows the experimentally obtained EOT dependence of the measured flat band voltage V_{fb} (measured) with respect to each high-k material. Here, the sheet charge and the uniform charge distribution are assumed to be located at interface and in bulk high-k, respectively. The EOT is changed by changing the IL thickness and the intercept at y axes (EOT = 0 nm) indicates the intrinsic flat band voltage, V_{fb} (intrinsic) [62].

However, the actual V_{fb} obtained is found to deviate from the expected value at extremely small values of EOT which unfortunately corresponds to the EOT range of the gate dielectric of the real device. This undesirable degradation of V_{fb} is called “ V_{fb} roll-off”. In order to obtain the band edge work function, this roll-off should be suppressed as much as possible. The reason of this V_{fb} roll-off is considered to be due to the fix charges in the high-k bulk and the FLP.

Since the work function (WF) is closely related to V_{fb} , it behaves similarly as V_{fb} in addition to the influence of the FLP. Figure 4.58 illustrates how the WF behaves as EOT changes. The right hand axis corresponds to the empirical EOT dependence of V_{th} with respect to N and PMOS, indicating that –0.2 V corresponds to the VB (Valence Band) edge and +0.2 V corresponds to the CB (Conduction Band) edge [62].

Fig. 4.57 V_{fb} –EOT relation for various high-k gate dielectrics (experimental results)

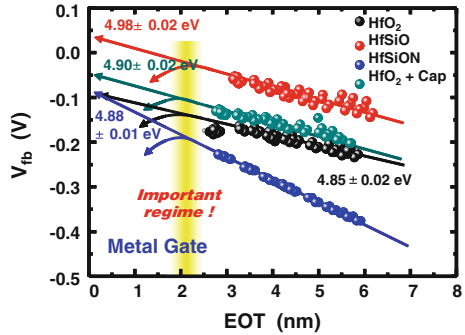
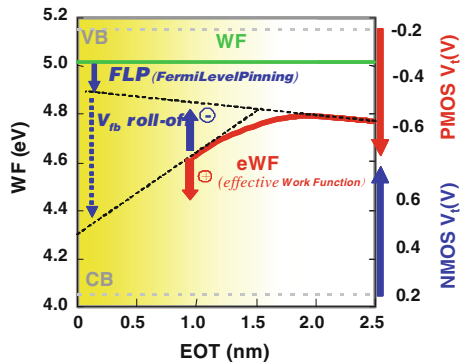


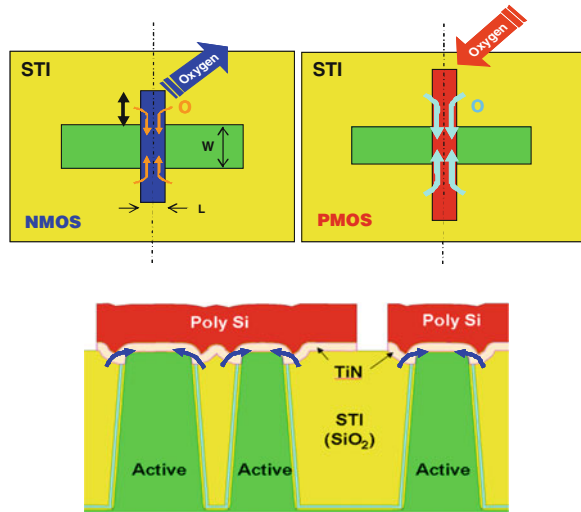
Fig. 4.58 Work function–EOT relation for high-k gate dielectric and the corresponding roll-off behavior together with the V_t trend [62]. “Gate last process” and “Gate first process” are indicated by green and red curves, respectively



Suppose that the green line indicates the net WF of the MG material, which is maintained as constant if it does not suffer from high temperature thermal treatment as is the case for the “Gate last process” which does not need high temperature thermal treatment. In contrast, for the conventional “Gate first process”, due to the interfacial reaction, the Fermi level is pinned and the WF varies linearly as indicated by the upward dotted line, with decreasing EOT. In addition, due to the fixed charge in the high-k dielectric, the WF obtained deteriorates as indicated by the downward dotted line, with decreasing EOT. Consequently, the effective WF obtained results in the V_{fb} -roll-off behavior. When (–) charge is increased in the high-k dielectric, the WF obtained tends to roll-up; in contrast, it tends to roll-off for more (+) charge such as oxygen vacancy, V_o^{2+} in the high-k dielectric. Fermi level pinning and V_{fb} roll-off have been analyzed in Chap. 5. Chapter 2 contains a theoretical treatment of the flat-band and threshold voltages in the case of the high-k gate stack.

In this way, compared to the “Gate last process”, the “Gate first process” often brings about undesirable work function degradation and improvement of the work function is extremely important for CMOS integration. The ideal band edge work function seems to be obtained by dual metal and dual dielectric for the “Gate first process”; however, these make the process extremely complicated for CMOS

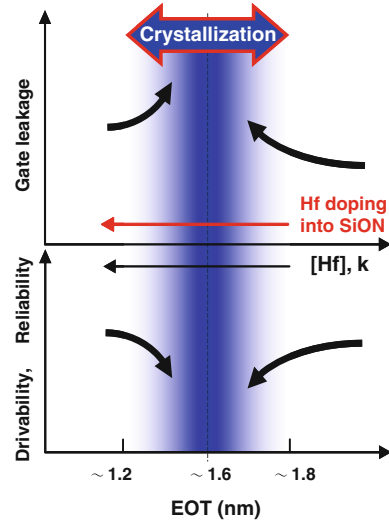
Fig. 4.59 Plan view (*upper side*) of N- and PMOSFETs formed by the “Gate first process” and cross-section (*lower side*) of respective MOSFETs surrounded by STI oxide for Poly Si/TiN/high-k gate stack structure



integration and leads to cost overrun. Thus, integration and V_{th} lowering are completely an antithetical. However, recently, by means of a variety of process ingenuities, the roll-off has been improved for the “Gate first process”. For example, thick (thin) TiN electrode provides higher (lower) work function, indicating work function can be tuned to some extent by changing the thickness of a single metal gate material. This type of additional tuning brings about significant advantage to achieve a target band edge work function.

On the basis of the above discussion, the CMOS integration issue is now discussed. It has been reported experimentally that the defect concentration in the gate stack could be modulated by the oxygenation over the gate sidewall after the Source/Drain activation. By introducing a lot of oxygen in the gate dielectric, the work function could be shifted towards the band edge, thus lowering V_{th} for PMOS [63]. This is consistent with the trend described in Fig. 4.58. When the density of oxygen vacancy in the PMOS gate dielectric was decreased, the V_{th} revealed a higher value and vice versa for NMOS. Figure 4.59 shows the plan view (upper part) of the respective N- and PMOS and the cross-section (lower part) of the MOSFETs. Yellow area indicates surrounding STI (Shallow Trench Isolation) which is made from SiO_2 . As is discussed above, a lot of oxygen is necessary for PMOS to keep the high WF and less oxygen is necessary for NMOS. From the process point of view, there is a concern that oxygen can invade into the gate from STI through the gate electrode and modulate the WF, hence V_{th} . To maintain the high functionality, effective process countermeasures to prevent invasion of oxygen into the NMOS gate stack and storing of the oxygen inside the PMOS gate stack are imperative for the “Gate first process”.

Fig. 4.60 EOT dependence of drivability, reliability, and gate leakage trend



4.4.6.2 Process Window

A more fundamental issue than the CMOS process lies in the realization of the MOSFET with the high-k/metal gate stack. That is the “crystallization” of the high-k layer, without which an MOSFET itself does not work and even more so for the CMOS realization. Rough prognostication based on the above discussion may give an insight into the guidelines for the high-k gate stack device development. Qualitative relation between EOT and key factors of FET such as I_{on} , reliability (Trapping, V_{th} shift, BTI, $1/f$), and gate leakage is roughly illustrated in Fig. 4.60 for the gate dielectric system consisting of Hf-based high-k. According to the k -[Hf] trend of Fig. 4.19 in Sect. 4.3.3, EOT increases with decreasing [Hf] and k value. When [Hf] is small, which indicates the case for thick EOT regime, the dielectric property approaches to that of SiON. Each respective phase can be realized by increasing/decreasing the HfO_2 thickness and/or increasing/decreasing the [Hf] in the SiON. By small amount of Hf doping into SiON, i.e., “thinner HfO_2 +thicker SiON”, the film nature approximates that of SiON; on the other hand, in case of large [Hf], i.e., thinner EOT, the dielectric property comes close to that of HfO_2 , which is formed by “thicker HfO_2 +thinner SiON”. And the regime in between these antithetical phases may induce crystallization. Empirically the crystallization appears at around $EOT = 1.6$ nm. This crystallization may cause the deterioration of electrical characteristics and this may also induce reliability degradation [64]. On the other hand, contrary to one’s expectations, from a precise analysis by EXAFS (Extended X-ray Absorption Fine Structure Spectroscopy), it is suggested that for a 1.4 nm-thick HfO_2 it is possible to have crystalline feature with polymorph transition [65].

As discussed above, the “ V_{fb} roll-off” and “Crystallization” are the serious intrinsic problems for the “gate first process” and these temperature process

related problems never happen in the “gate last process”. However, the electrical instability of “as deposited high-k dielectric” as well as the profile degradation of extension doping together with the complicated, high cost process may be a serious issues for the “gate last process”. Further study is necessary for these pros and cons.

4.5 Summary

Issues of material and processing of Hf-based high-k gate dielectric have been discussed. Different from the covalently-bonded SiO_2 gate dielectric, HfO_2 reveals a complex behavior. The root cause for this is based on its intrinsic solid state property. Due to the ionic-bond in HfO_2 , a large number of oxygen vacancies conduce unexpected phenomena and HfO_2 is thermodynamically unstable from the crystallographic point of view such as crystallization and phase separation.

To control these unfavorable phenomena and maintain homogeneity, the material properties of Hf-based high-k gate dielectric and its influence on the electrical characteristics including reliability are analyzed. Several intrinsic key issues such as interfacial control, optimization of the Hf-based high-k gate dielectric formation, breakdown issues as well as bulk trapping phenomena are discussed on the basis of the experimental results.

Crystallization of the Hf-based gate dielectric material, thermal treatment, and interfacial reaction are most important issues in the device fabrication process. Among them, nitrogen has an important role to prevent chemical reaction in the film. For the process control of Hf-based high-k gate dielectrics, oxidation of the Hf-metal has potential for controlling the interfacial layer thickness and EOT scaling. When FUSI gate is introduced, chemical reaction control by nitrogen is effective at the top interface as well as in the bulk. Gate electrode influence on EOT is also an issue analyzed.

From the device performance point of view, these processing/material considerations mentioned above can be interpreted as follows.

For the high-k gate stack with a metal gate electrode including the capping technique and its CMOS processing by the “gate first” process, achievement of the band edge work function rests critically on controlling the number of fixed charges, in other words, control of the oxygen vacancy in the high-k gate dielectric; this will determine the drivability of the high-k transistor and crystallization which will seriously influence the gate leakage performance.

Based on the discussions above, as the guideline for an optimum FET with Hf-based gate dielectric, the medium EOT range where the crystallization tends to happen should be avoided in order to avoid the crystallization of the bulk Hf-based high-k gate stack.

The pros and cons between the “gate first” and the “gate last” process are key issues and are relegated to [Chap. 5](#), where process complexity and cost in addition to performance improvement are considered in detail.

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