Chapter 11
Crystalline Oxides on Silicon

H. Jörg Osten

Abstract The ability to integrate crystalline metal oxide dielectric layers into silicon structures can open the way for a variety of novel applications which enhances the functionality and flexibility, ranging from high-k gate dielectric replacements in future Metal Oxide Semiconductor (MOS) devices to oxide/silicon/oxide heterostructures for nanoelectronic application in quantum-effect devices. We present results for crystalline gadolinium oxides on silicon in the cubic *bixbyite* structure grown by solid source molecular beam epitaxy. On Si (100) oriented surfaces, crystalline Gd_2O_3 grows as (110)-oriented domains, with two orthogonal in-plane orientations. Layers grown under best vacuum conditions often exhibit poor dielectric properties due to the formation of crystalline interfacial silicide inclusions. Additional oxygen supply during growth improves the dielectric properties significantly. Experimental results for Gd_2O_3-based MOS capacitors grown under optimized conditions show that these layers are excellent candidates for application as very thin high-k materials replacing SiO_2 in future MOS devices. Epitaxial growth of lanthanide oxides on silicon without any interfacial layer has the advantage of enabling defined interfaces engineering. We will show that the electrical properties of epitaxial Gd_2O_3 thin films on Si substrates can further be improved significantly by an atomic control of interfacial structures. The incorporation of few monolayers of Ge chemisorbed on the Si surface has been found to have significant impact on the electrical properties of crystalline Gd_2O_3 grown epitaxially on Si substrates. Efficient manipulation of Si(100) 4° miscut substrate surfaces can lead to single domain epitaxial Gd_2O_3 layer. Such epi-Gd_2O_3 layers exhibited significant lower leakage currents compared to the commonly obtained epitaxial layers with two orthogonal domains. For capacitance equivalent thicknesses below 1 nm, this difference disappears, indicating that for ultrathin layers, direct tunneling becomes dominant. Further, we investigate the effect of post-growth annealing on layer properties. We show that a

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standard forming gas anneal can eliminate flat-band voltage instabilities and hysteresis as well as reduce leakage currents by saturating the dangling bonds caused by the bonding mismatch. In addition, we investigated the impact of rapid thermal anneals on structural and electrical properties of crystalline Gd_2O_3 layers grown on Si. Finally, we will present a new approach for nanostructure formation which is based on solid-phase epitaxy of the Si quantum-well combined with simultaneous vapor-phase epitaxy of the insulator on top of the quantum-well. Ultra-thin single-crystalline Si buried in a single-crystalline insulator matrix with sharp interfaces was obtained by this approach on Si(111). In addition, structures consisting of a single-crystalline oxide layer with embedded Si nano-clusters for memory applications will also be demonstrated.

11.1 Introductory Remarks

Many materials systems are currently under consideration as potential replacements for Si-based gate dielectrics for sub-100-nm Complimentary MOS (CMOS) technology. The gate leakage current, at least for direct quantum–mechanical tunneling, is exponentially dependent upon the thickness of the dielectric, while the capacitance is only linearly dependent on the thickness. Short-channel performance degradation is caused by the fringing fields from the gate to the S/D (Source/Drain) regions, depending on the gate dielectric thickness-to-length aspect ratio. Therefore, materials with too high dielectric constant will create additional problems. A desirable alternative gate insulator material should have a dielectric constant of five to ten times higher than SiO_2 that is between 20 and 40. The use of such high-k dielectrics would provide scaled-down values of Equivalent Oxide Thickness (EOT) required to maintain the Field Effect Transistor (FET) current drive, while reducing tunneling current through an increase in the film thickness [1]. At first glance, this would seem to be a winning proposal, since a substantial reduction in the current should be possible with only small increases in thickness. There is, however, another exponentially dependent term in the tunneling current—the barrier height between the semiconductor and the conduction band of the insulator. The tunnel current is exponentially dependent upon the barrier height. Therefore, not only is a material with higher dielectric constant required, but this material must also have a suitably large barrier height, to keep the gate leakage currents within reasonable limits. However, physical thickness and interfacial band alignment are only two factors that affect the device performance. Other basic limitations for high-k gate dielectric substitutions include those associated with the chemical and the physical bonding constrains. Bonding at the Si–SiO_2 (and also Si–Si_3N_4) interface is *isovalent* with bond charge exactly matching the nuclear charge. Each dangling bond on a Si surface has one electron, and this contributes to an interfacial two electron pair bond with an oxygen (or nitrogen) atom. Most high-k materials such as the binary metal oxides are generally more ionic, and

additionally more highly coordinated on the average than SiO_2. In a simple picture, one would expect, that these dielectrics will form *heterovalent* interfaces with Si with a quantitative mismatch between bond and nuclear charge. This mismatch can give rise to interfacial traps and/or fixed charges.

Another limitation on the material choice concerns stability problems [2]. The alternative gate dielectrics have to be compatible with a CMOS process flow. That poses severe restrictions on the materials due to the post-growth processing steps (like thermal stability, or manufacturability). The high-k dielectric will most likely be deposited on a Si channel. Therefore, it should not show any tendency to form silicides, silicates, silicon dioxides, or mixtures of those during post-deposition annealing. Thermodynamic stability consideration reduces the number of possible candidates significantly.

Many dielectrics appear favorable in some of these fields, but very few materials are promising with respect to all of these guidelines. The most promising of these are the simple binary metal oxides. Unfortunately, a number of these materials are not thermally stable on silicon [2]. The formation of SiO_2 and/or metal silicate interfacial layers often occurs when these materials are deposited upon silicon. Further growth of silicon dioxide or a silicate at the interface takes place during subsequent annealing steps. It is important to note, however, that the occurrence of any interfacial layer of SiO_2 or another low permittivity material, will limit the highest possible gate stack capacitance, or equivalently, the lowest achievable EOT value. This effect of reduced capacitance can be seen by noting that when the structure contains several dielectrics in series, the lowest capacitance layer will dominate the overall capacitance and also set a limit on the minimum achievable t_{eq} value. For example, the total capacitance of two dielectrics in series is given by

$$1/C_{tot} = 1/C_1 + 1/C_2, \tag{11.1}$$

where C_1 and C_2 are the capacitances of the two layers, respectively. If one considers a dielectric stack structure such that the bottom layer (layer 1) of the stack is SiO_2, and the top layer (layer 2) is the high-k alternative gate dielectric (11.1) is simplified (assuming equal areas) to

$$t_{eq} = t_{SiO2} + \left(k_{ox}/\, k_{high-k}\right) t_{high-k}. \tag{11.2}$$

For example, to obtain an EOT of 1.2 nm one could use a hypothetical 7.7 nm thick layer with k = 30. The presence of a 0.8 nm interfacial SiO_2 layer would reduce this thickness down to only 1.5 nm. For the same required EOT the physical thickness of the high-k material decreases significantly due to the interfacial layers; thus, the leakage current through the film also increases substantially. Therefore, much of the expected increase in the gate capacitance associated with the high-k dielectric is compromised.

The common approach for alternative high-k gate dielectrics has involved the amorphous metal oxides. In general, attempts have been made to keep these materials amorphous, in particular, after post-deposition high temperature

processing in order to avoid increased surface roughness and additional leakage due to the formation of grain boundaries. Generally, all known high-k materials are highly ionic. There are some general trends related to the ionicity of an oxide: The crystallization temperature decreases and the dielectric constant increases with the ionic character. Due to the relatively low re-crystallization temperature of highly ionic materials, these materials are often not compatible to a CMOS process. It is possible to reduce the ionicity (and thereby increase the crystallization temperature) by alloying the metal oxides with Al or Si. These aluminates or silicates are thermally more stable on silicon but have lower dielectric constants. Consequently, for a given EOT, the physical layer thickness has to be reduced, leading to an increase in the leakage current.

The upcoming generation of high-k dielectrics will most likely be formed by amorphous hafnium-based alloys. As discussed above, however, the existence of an interfacial layer of SiO_2 or another low permittivity material, will limit the highest possible gate stack capacitance, or equivalently, the lowest achievable EOT value (see 11.2). Thus, any interfacial lower-permittivity layer should be minimized in the future generations. However, it is essential to keep the channel carrier mobility high. In addition, the increased process complexity for the deposition and control of additional ultrathin dielectric layers, as well as scalability to later technology nodes, remains a concern.

The 2nd generation of high-k materials have to be formed without any interfacial layer to realize EOT <0.8 nm. In such a case, the high-k dielectric/Si interface properties influence the device performance significantly. A good interface requires either that the oxide is amorphous, or that it is epitaxial and lattice-matched to the underlying silicon. Amorphous dielectrics are expected to be able to adjust the local bonding to minimize the number of Si dangling bonds at the interface. The alternative is to use an epitaxial oxide. This involves more effort, but it has the advantage of enabling defined interface engineering. Generally, there are two groups of possible candidates for epitaxial growth on Si, namely (a) perovskite-type structures and (b) binary metal oxides, in particular lanthanide oxides [3, 4]. In the following, we will concentrate on the binary lanthanide oxides.

11.2 Lanthanide Oxides on Silicon

Lanthanide oxides (LnO's) form a very interesting group of insulators for epitaxial growth on silicon [5]. It is extremely important and desirable to integrate these highly functional metal oxides into mature semiconductor technologies. The LnO's can have different oxygen compositions LnO_x, with x ranging from 1 to 2 due to the multiple oxidation states (+2, +3, and +4) of the rare-earth metals [6, 7]. This leads to oxides with different stoichiometries (LnO, Ln_2O_3, LnO_2). All known Ln (II) oxides, like EuO, are not insulating. Therefore, they will not be considered here any further. For application in a Si-based device fabrication process, all lanthanide oxides exhibiting more than one valence state (+3 and +4) are not the

best choice as epitaxial high-k materials because of the coexistence of phases with different oxygen content. For example, cerium(IV) oxide (CeO_2) can release oxygen under reducing conditions forming a series of reduced oxides with stoichiometric cerium(III) oxide (Ce_2O_3) as an end product, which in its turn easily takes up oxygen under oxidizing conditions, turning the cerium(III) oxide back into CeO_2. In addition, stable mixed valence-state structures can occur for some LnO's. For example, the mixed valence-state Pr_6O_{11} is the most stable phase for praseodymium oxide.

For the highly ionic oxides, the position of the charge neutrality level depends strongly on the stoichiometry [8]. Thus, also the band alignment to silicon and, finally, the leakage behavior becomes strongly dependent on the oxygen content. All lanthanide oxides displaying only one valence state are easier to handle due to the absence of transitions between phases with different oxygen content. Based on that argument, we will focus our discussion mainly on lanthanide (III) oxides (occurring as Ln_2O_3).

The Ln_2O_3 oxides can occur in different structural phases, like the manganese oxide (Mn_2O_3) or *bixbyite* structure. Some of these oxides also crystallize in the hexagonal lanthanum oxide structure, which is suitable for epitaxy only on Si(111). Also, monoclinic phases are known for various lanthanide(III) oxides. Different crystallographic structures are accompanied by different dielectric properties. Several lanthanide oxides can undergo structural phase transformation within a temperature range, typical for CMOS processing [9], see Fig. 11.1; these oxides are not very well suited for technological applications.

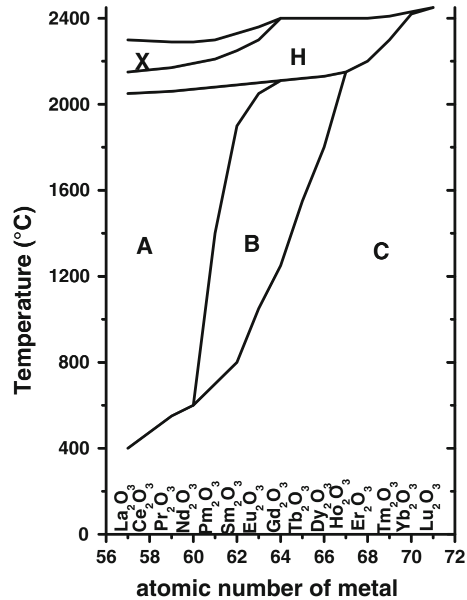

Fig. 11.1 Structural phase transitions in lanthanide oxides (based on Ref. [9]): *A*: hexagonal (P63/m) *B*: monoclinic (C2/m) *C*: cubic (Ia-3) *H*, *X* high-T modifications

Epitaxial growth on a clean surface requires matching in symmetry as well as in atomic spacing. Here, we will present results for crystalline gadolinium oxide on silicon with the Gd_2O_3 composition in the cubic *bixbyite* structure which has a large band gap of about 6 eV and nearly symmetrical band offsets to Si [10] as well as a low lattice mismatch of about 0.5 %. The *bixbyite* structure is based on the calcium fluorite structure, where 1/4 of the oxygen atoms have been removed from specific lattice sites. That structure has a lattice symmetry suitable for epitaxial growth on Si(100) and Si(111).

Commonly, epitaxial heterostructures are evaluated on the basis of lattice matching, with the misfit defined as the relative difference in the lattice constants (a_{film} and a_{Si}). Here, the lattice mismatch would be identical for all three epitaxial relationships, i.e. (100)//(100), (110)//(110), and (111)//(111). All other combinations violate symmetry matching. This concept is misleading, because epitaxial growth is also governed by the surface and interface energetics. In the case of the rare-earth oxides, the surface energy of the (100) surface is much higher than that of the Si(100) surface [11]. That could result in a 3-dimensional growth mode or in a change of the growth direction towards a low-energy surface orientation. The latter is observed for the growth on Si(100) for most of the lanthanide oxides, where the oxides were found to grow in the (110) orientation. For the understanding of the Ln_2O_3(110)/Si(100) interface formation we have to consider that the lattice is made up of metal atoms occupying the positions of a face-centered cubic lattice with a lattice constant a_{film}, where the tetrahedral holes are occupied by the oxygen atoms. However, the growth of LnO's is based on the deposition of metal oxide molecules. Due to the existence of highly ionic Ln–O bonds in combination with the high bonding strength of the covalent Si–O bonds, we can assume that the interface is predominantly formed by Si–O–Ln bonds. Therefore, the matching of the oxygen atoms is the important parameter (Fig. 11.2).

The complete crystallographic structure can also be described by two non-identical metal and oxygen lattices, respectively. The arrangement of the oxygen atoms forms a simple cubic lattice with a lattice constant of $a_{film}/2$. Thus, the interesting matching condition for epitaxial growth is the Ln_2O_3(110)[100]//

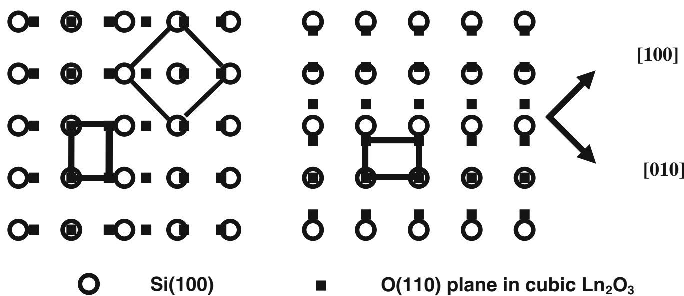

Fig. 11.2 Ln_2O_3(110)//Si(100) alignment (schematically): 1:1 matching occurs along one direction. In the other direction, there is roughly a 3:2 matching relation. Two types of (110)-oriented domains are possible, with two orthogonal in-plane orientations

Si(100)[110] relation. In that case, nearly 1:1 matching should occur along one direction. In the other direction, there would be roughly a 3:2 matching relation. As shown schematically in Fig. 11.2, layers grown in this orientation exhibit mostly two types of (110)-oriented domains, with two orthogonal in-plane orientations (found experimentally for a large variety of binary metal oxides on Si(100), like Er_2O_3 [12], Sm_2O_3 [13], Lu_2O_3 [14, 15], Sc_2O_3 [16], Gd_2O_3 and Y_2O_3 [17]). That is even enforced by the Si(100) dimer (2×1) surface reconstruction. Dimer rows on adjacent terraces are oriented perpendicular to each other and nucleation of the oxide on Si(100) follows the dimer orientation, which results in the domains on stepped surfaces [18]. Due to the 45° rotation of the (110) plane relative to the substrate, the mismatch for the 1:1 matching is identical to that one obtained from applying the lattice constant concept.

11.3 Epitaxial Growth of Lanthanide Oxides on Silicon

All experiments were performed in a multi-chamber ultrahigh-vacuum system (*DCA Instruments*) capable of handling 8” wafers. This system includes a growth, an annealing, and an analysis chamber connected by an ultra-high vacuum (UHV) transfer system. The layers were grown on 4” Si substrates with different orientations. Substrates were cleaned *ex situ* using as the last step diluted HF etch ($HF:H_2O = 1:10$) followed by a dilution rinse, and then were immediately inserted into the vacuum system. Substrates were annealed in situ to transform the initial hydrogen-terminated (1×1) surface structure into the (2×1) superstructure indicating a clean and well-ordered surface. Commercially available, granular Gd_2O_3 material was evaporated using an electron-beam evaporator. Growth temperatures were in the range 800–1,000 K. Typical growth rates were 0.005–0.01 nm/sec. The surface and layer structure was evaluated during the growth by reflection of high energy electron diffraction (RHEED).

After growth, the wafers can be transferred into the analysis chamber without leaving the UHV to perform x-ray photoelectron spectroscopy (XPS) investigations. Non-monochromatized Al Kα radiation ($h\upsilon = 1{,}486.6$ eV) was used for the excitation of photoelectrons. All measured wafers were electrically grounded to eliminate charging effects during long-time measurements. To minimize experimental uncertainties associated with energy variations caused by spectrometer instabilities and to improve the signal to noise ratio, the XPS data were collected by repeatedly scanning the silicon, the lanthanide, and the oxygen level. A multipeak Gaussian deconvolution procedure was used to extract the exact line position and intensities.

The layer thickness was measured *ex vacuo* by X-ray reflectivity (XRR) using a standard single crystal diffractometer with graphite monochromator in front of the detector. Layers were also characterized by X-ray diffraction (XRD) ($\Theta/2\Theta$, ω and Φ-scans) and transmission electron microscopy (TEM), i.e., high resolution cross-section and plan-view images combined with selected area diffraction (SAD).

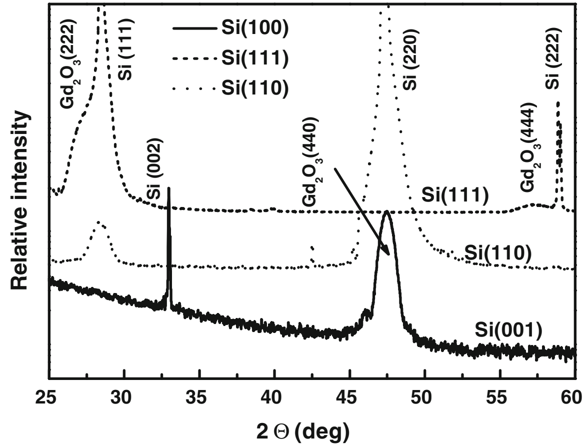

Fig. 11.3 X-ray diffraction patterns of Gd_2O_3 thin films grown on silicon substrates with different orientations at a substrate temperature of 700 °C

On the Si(100) substrate, the grown layers exhibit the known two types of (110)-oriented domains, with two orthogonal in-plane orientations [19]. On (111) oriented Si surface, *bixbyite* Gd_2O_3 grows epitaxially when the substrate temperature is above 600 °C. Here, the oxide exhibits an A/B twining relationship where B is related to the substrate twinning orientation A by a 180° rotation around the Si(111) surface normal. On a Si(110) surface, grown layers exhibit pronounced faceting by the development of low-energy {111} facets [20].

Figure 11.3 shows the X-ray ($\Theta - 2\Theta$ scan) diffraction patterns of Gd_2O_3 thin films grown on different Si substrates. Gd_2O_3 layer on the Si(100) surface exhibits a distinct peak at $2\theta = 46.4^{\circ}$ corresponding to the d(440) inter planar spacing of cubic Gd_2O_3 along the [110] orientation. The layers on the Si(111) substrate also exhibit single orientation without any indication of disoriented crystallites. The peaks at 28.5° and 59.4° corresponding to d(222) and d(444) interplanar spacing are hidden under the appropriate Si peaks. The $\Theta - 2\Theta$ scan for Gd_2O_3 thin films grown on Si(110) displays a peak at 28.5° confirming the preferential growth along the (111) direction as observed in RHEED images (not shown).

11.4 Electrical Characterization

Figure 11.4 compares the capacitance versus voltage (C–V) characteristics of Gd_2O_3 thin films deposited on Si substrates with different orientations. For the comparison, films with similar thickness in the range of 4–5 nm have been chosen [20]. As demonstrated in the C–V characteristics, there is no distinct difference in the accumulation capacitance for the films grown on differently oriented Si substrates. Despite having a different crystalline layer structure, the films on Si(110) substrate exhibit electrical properties similar to other orientations. The accumulation capacitance measured for Gd_2O_3 on Si(110) was close to the value of those

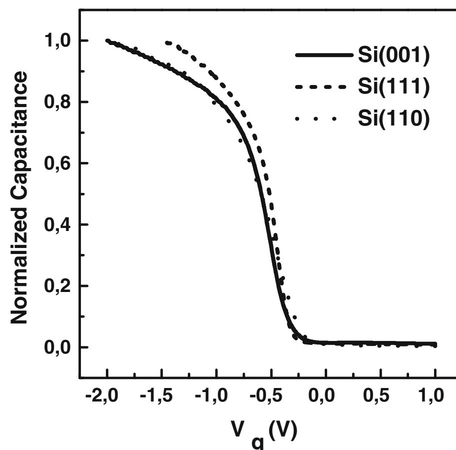

Fig. 11.4 Normalized capacitance–voltage characteristics of epitaxial Gd_2O_3 thin films on different silicon substrates

grown on other two substrates. The capacitance equivalent thicknesses (CET) estimated for all three films were around 0.9 nm. No hysteresis was observed in the C–V measurements. The normalized capacitance for all three cases shows also no differences in the flat band voltage (~ -0.25 V). The flat-band voltage shift is generally due to the flat-band interface charge, to which both the fixed charge as well as the flat-band interface trap charge contributes. It infers that the same amount of positive charges is involved in each case, i.e. that the substrate orientation has also no significant influence on fixed charge concentration.

Interface trap density (D_{it}) and leakage current density (J) are also important parameters which characterize the gate dielectrics (Figs. 11.5 and 11.6). Among the various techniques available, we have used the conductance method for evaluating the D_{it}. This method is generally considered to be most sensitive for this purpose. The equivalent parallel conductance (G_p) of MOS capacitor is measured as a function of the gate bias and the frequency ($2\pi f$), the details of which are described in Ref. [21]. G_p calculated from the measured conductance, shown in Fig. 11.6 as a function of the frequency, displays a maximum at a particular

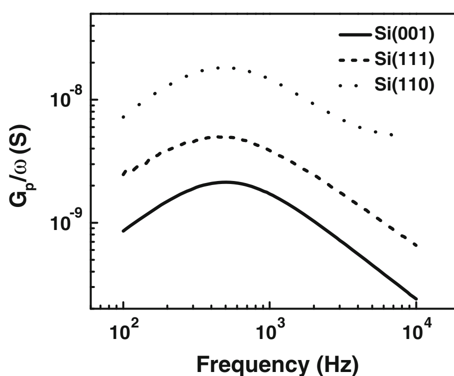

Fig. 11.5 Equivalent parallel conductance (G_p/ω) estimated from measured conductance (G_m) as a function of frequency at $V_g = -0.5$ V for three different substrates

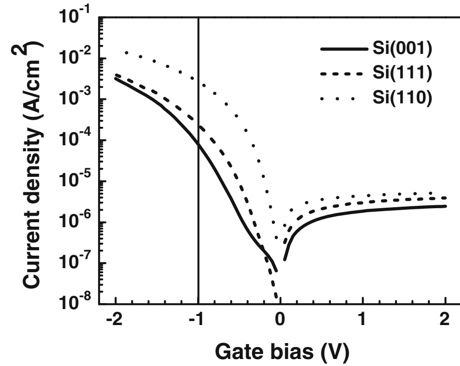

Fig. 11.6 Leakage current characteristics of epitaxial Gd_2O_3 thin films grown on different silicon substrates

frequency. The values of D_{it} estimated from the peak in the G_p/ω versus ω plot are $1.0 \cdot 10^{12}$, $2.4 \cdot 10^{12}$ and $9.0 \cdot 10^{12}$ $cm^{-2}eV^{-1}$ for Si(100), Si(111) and Si(110), respectively. However, broadening in the peak could be attributed to the interface traps having distribution of relaxation times. The current density in Pt/Gd_2O_3/Si(110) MOS structure is found to be slightly higher in comparison to other substrates; nevertheless, the value is much lower than the expected value for SiO_2 capacitor with the same equivalent thickness. We suppose that the larger leakage current in Gd_2O_3/Si(110) capacitor could be due to structural defects in the bulk and at the interface. Reference [10] contains further investigations of the electronic structure at interfaces of crystalline and amorphous Gd_2O_3 thin layers with silicon substrates of different orientations.

11.5 Impact of Oxygen Concentration on Layer Properties

Recently, we investigated the interface and the layer formation processes of Ln_2O_3 films on Si(100) grown under ultra-clean ultra-high vacuum (UHV) conditions of Molecular Beam Epitaxy (MBE) [22]. Layers grown under best vacuum conditions often exhibit very high leakage currents. We found that the partial oxygen pressure during the interface formation and during the growth is a very crucial parameter. Too low oxygen content can lead to the formation of silicide-like inclusions. For Ln_2O_3 growth, the formation and stability of the silicide-like phase depends on the oxygen chemical potential [23]. Considering the low oxygen partial pressure under the UHV conditions (as used in MBE growth), the chemical potential of oxygen can become negative. Thus, silicide formation will be favorable compared to oxide formation. That is one of the most crucial points for the growth of dielectric layers, because the silicide growth can continue as long as the oxygen content remains low enough or the oxygen chemical potential remains strongly negative. This occurs even faster at a surface or interface region where the thermodynamic equilibrium is distorted, for example, due to stress. The appearance of silicide inclusions seems to be a serious drawback for a lot of possible material candidates

for future high-k applications. For the epitaxial growth of Ln_2O_3 oxides, a well-controlled interface and appropriate engineered growth procedures are necessary to realize the required electrical properties. The available oxygen concentration can be controlled by modifying the MBE growth processes using an additional oxygen supply. We found, that MBE growth under defined oxygen partial pressures during the interface formation and/or during the subsequent growth can prevent any kind of silicide inclusions and void formation [24]. On the other hand, too high oxygen content might oxidize the Si surface, leading to a lower-k interfacial SiO_x layer, which finally limits the achievable minimal equivalent oxide thickness.

In a set of experiments, we varied the growth temperature while keeping all the other parameters constant. Figure 11.7 shows the extracted CET values versus the physical oxide thickness. The oxygen partial pressure during growth was kept at $1 \cdot 10^{-7}$ mbar. In a simple picture, a system including an interfacial layer and a high-k layer can be described by a linear relation between CET and the physical thickness (11.2).

The experimental results shown in Fig. 11.7 follow that relation. The slope for all three temperatures is nearly equal resulting in an intrinsic dielectric constant of around 20 for the high-k layer in all the three cases. Only the intercept for $t = 0$ varies with the growth temperature, yielding 0.4, 0.9, and 1.4 nm, respectively. Based on (11.2), this intercept is often attributed to the physical thickness of an interfacial layer only. However, an increase of the thickness with the increasing growth temperature was not supported by XRR and XTEM (Cross-sectional TEM) investigations. Instead, we suppose that the dielectric constant (k_{IF}) at the interface decreases due to the transformation of the interfacial layer from a silicate-like type to a more silicon-oxide like layer. That can be explained by the fact that gadolinium, in contrast to cerium or praseodymium, can only exist in the +3 oxidation state. Thus under equilibrium conditions, the Gd_2O_3 bulk cannot act as an effective source for oxygen supply to the Si/dielectric interface. For an interfacial layer other than silicon dioxide (11.2) transforms into

$$CET = t_{IF}(3.9/k_{IF}) + \left(3.9/k_{high-k}\right)t_{high-k}. \tag{11.3}$$

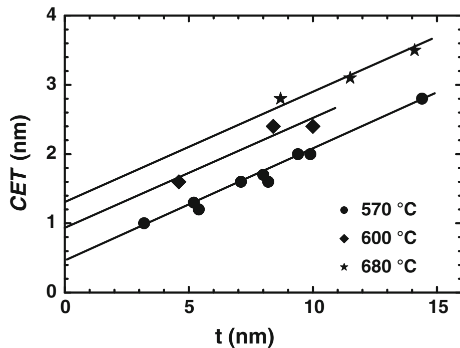

Fig. 11.7 CET as a function of the physical layer thickness for Gd_2O_3 layers grown on p- and n-type Si(100) at 570, 600, and 680 °C, respectively. The oxygen partial pressure during growth was kept at $1 \cdot 10^{-7}$ mbar

Next, we investigated the influence of different oxygen partial pressures. The results are very similar for all investigated growth temperatures. For the layer grown with the lowest oxygen pressure ($1 \cdot 10^{-7}$ mbar), we always found strong hysteresis which we attribute to the presence of oxygen vacancies. Increasing the oxygen pressure to $5 \cdot 10^{-7}$ mbar results in a significant reduction of the hysteresis. Further increase in oxygen partial pressure p_{O2} does not lead to a further improvement of the electrical properties of the layer, but increases the physical thickness of the interfacial layer, as detected by XTEM. At this pressure, the oxygen concentration becomes supersaturated at the growth front, and oxygen atoms diffuse to the interface.

We obtained the best electrical results for growth at 600 °C and $p_{O2} = 5 \cdot 10^{-7}$ mbar. Figure 11.8 shows a cross-sectional TEM micrograph of a sample with a 15 nm thick Gd_2O_3 layer grown under these conditions on Si(100). No pronounced interfacial layer between the Si and the oxide layer can be detected.

Layers grown by an optimized MBE process display a sufficiently high-k value to achieve equivalent oxide thickness values <1 nm (Fig. 11.9), combined with ultra-low leakage current densities, good reliability, and high electrical breakdown voltage. This makes epitaxial Gd_2O_3 layers excellent alternative for replacing SiO_2 as a gate dielectric. First electrical characteristics of fully-depleted n- and p-type Silicon On Insulator (SOI)-MOSFETs with epitaxial Gd_2O_3 and TiN metal gate electrodes demonstrate the feasibility of this novel gate insulator [25]. Electrical properties of the gate stack have been extracted from the devices and CMOS process compatibility has been addressed. The oxide interface state density has

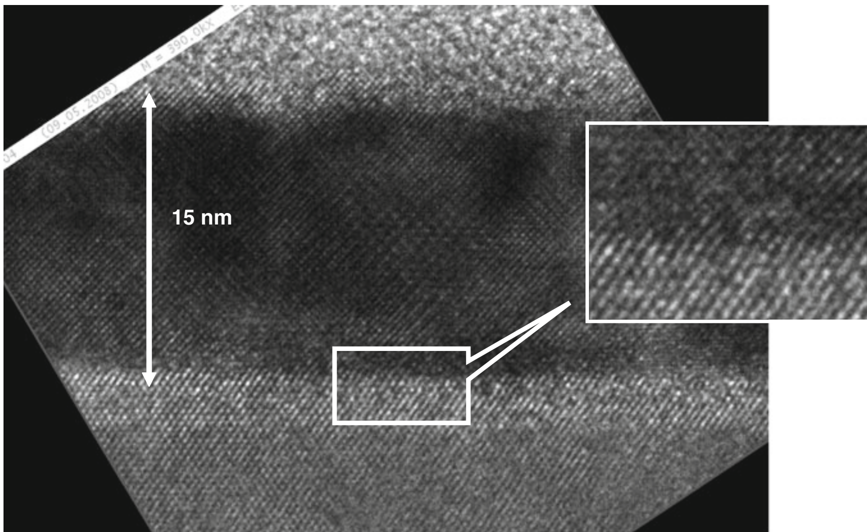

Fig. 11.8 High-resolution cross-sectional TEM image of a Gd_2O_3/Si(100) stack. The oxide layer was grown at 600 °C and $p_{O2} = 5 \cdot 10^{-7}$ mbar. No pronounced interfacial layer is visible

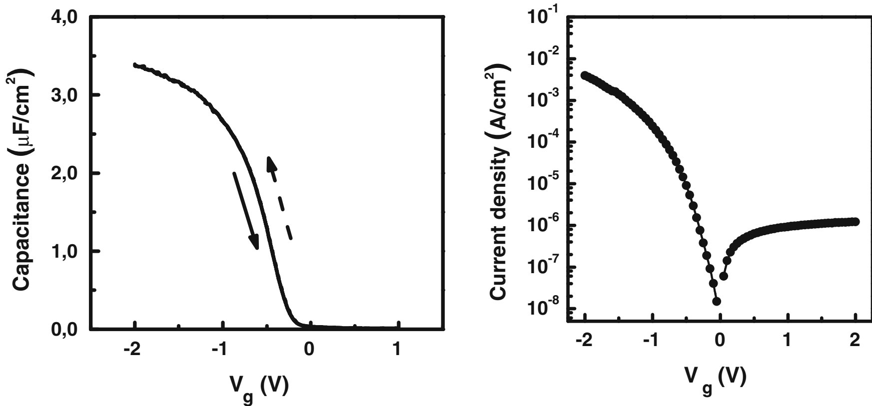

Fig. 11.9 MOS capacitor with Gd_2O_3 on p-Si(100): EOT <0.7 nm, hysteresis <10 mV, J @ (V_{FB} − 1 V) = 0.5 mA/cm^2

been found to decrease after rapid thermal annealing. On the other hand, mobile oxide charges and oxide traps have been significantly reduced by Rapid Thermal Annealing (RTA). The p-MOSFETs exhibit higher saturation currents compared to n-MOSFETs as they were accumulation-mode transistors with a p^+–p^-–p^+ doping structure.

In accumulation-mode p-MOSFETs, higher drain currents can be achieved as conduction appears at the front interface as well as in the body region below compared to an inversion channel which is confined at the front interface [25]. In order to minimize process induced oxide damage, MOSFET's with W/Gd_2O_3 gate stack have been fabricated in a virtually damage-free damascene metal process [26]. The major process steps of the replacement gate process are the following: Initially, dummy gate stacks are formed followed by self-aligned S/D ion implantation. An alignment-oxide is deposited by chemical vapor deposition (CVD), annealed and planarized by chemical–mechanical polishing (CMP) down to the gate level. The dummy gates are removed completely by wet chemical etching, leaving a self-aligned imprint of the gate stack on the Si-wafer. Subsequently, the gate dielectric (Gd_2O_3) is grown. A metal layer is deposited on top of the gate dielectric and CMP is used to pattern the damascene metal gates. Standard back-end processing completes the fabrication. This was the first successful attempt to integrate crystalline high-k dielectrics into a "gentle" damascene metal gate process in order to reduce process induced oxide damages.

The lattice parameters of Gd_2O_3 and Nd_2O_3 in their *bixbyite* phase are 1.081 and 1.108 nm, respectively. Thus, $2a_{si}$ is 0.5 % larger than Gd_2O_3 and 2.1 % smaller than Nd_2O_3, respectively. Therefore, a combination of these two oxides would create a system exhibiting exact lattice matching with Si especially at the deposition temperature. Therefore, such a ternary system would provide much more flexibility in choosing the epitaxial high-k oxide for next generation CMOS devices. Recently, we reported the growth and electrical properties of crystalline

mixed $(Nd_{1-x}Gd_x)_2O_3$ thin films and compared the results with those of binary Gd_2O_3 and Nd_2O_3 thin films, respectively [27]. Also the ternary films show excellent electrical properties with the CET values far below 1 nm, and associated leakage currents below 1 mA/cm^2, respectively. The electrical properties of the multi component oxides are comparable to those of the binary oxides. This work reveals that such mixed oxides would enlarge the window for material selection suitable for the upcoming generations of CMOS devices.

11.6 Effect of Domain Boundaries

Despite having a suitable crystalline structure, epitaxial rare earth oxides, when grown on Si(100) substrates, usually exhibit two (110) oriented orthogonal domains and hence, one could anticipate a great impact of domain boundaries on the final electrical performance. However, to elucidate the impact of such domain boundaries is more complicated because the growth of epitaxial lanthanide oxides in the common *bixbyite* structure on standard Si(100) substrates always leads to the formation of these two types of [110]-oriented domains, with two orthogonal in-plane orientation, each of them exhibiting two fold symmetry. It was suggested by Kwo et al. [17, 28] that the use of vicinal (4° miscut along <110>azimuth) Si(100) substrate could be a viable way to grow single-domain (SD) epitaxial layer, thus to eliminate domain boundary effect on electrical properties similar to what was also known from the growth of III–V compounds on Si(100) [29].

Recently, we showed that not only the use of vicinal surface is necessary but also the preparation of silicon surface prior to the layer growth is a very important step to achieve single domain epitaxial Ln_2O_3 layer on vicinal (4° miscut) Si(100) substrates [30]. The reason could be understood in the following way. It was reported earlier that the presence of dimers on a (2 × 1) reconstructed Si(100) surface forces the overgrown lanthanide oxide layer to form orthogonal oriented ad-dimers in line with Si dimer rows [31]. Normally, dimer rows on adjacent terraces are oriented perpendicular to each other and nucleation of the oxide on (2 × 1) Si(100) follows the dimer orientation, which results in the domains. If, this makes an arguable explanation; then, it seems to be possible to grow a single domain (SD) epi-layer on Si substrate if and only if all dimers on the surface are parallel to each other. Obviously, the next question is how to achieve such Si(100) surfaces with only one dimer orientation? Double-atomic steps result in the Si-dimers arranged only in one orientation across the whole surface. Such steps are easier to achieve on 4°-miscut surface; however, it demands a careful preparation of the Si(100) surface (details can be found in Ref. [30]).

Various layers were grown under identical deposition conditions (substrate temperature of 675 °C with oxygen partial pressure of $5 \cdot 10^{-7}$ mbar) on Si(100) 4° off substrates with and without surface preparation. The detailed structural quality of the layers was investigated by x-ray diffraction technique. The asymmetric 360° x-ray phi (Φ) scans (azimuthal rotation) were carried out to determine

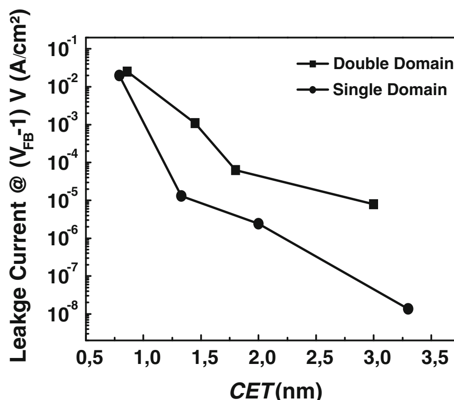

Fig. 11.10 Leakage current density of as-grown Gd_2O_3 SD and DD layers as a function of capacitance equivalent oxide thickness (CET)

the in-plane symmetries of the Gd_2O_3 layers and therefore, to confirm the presence of only a single or/and double domains in the layers. From these investigations (and additional TEM investigations) we can confirm that domain boundaries could be eliminated completely in the epitaxial single crystalline lanthanide oxide grown on carefully prepared 4°-off oriented Si(100) substrates. Next we performed electrical evaluations on those layers (Fig. 11.10). They clearly demonstrate that the as-grown SD Gd_2O_3 layers exhibit much lower leakage current for similar CET values, inferring that the domain boundaries in double domain Gd_2O_3 layers act as the leakage paths for the charge carriers. However, this disparity in the leakage current could only be observed for the thicker layers (>6 nm). For capacitance equivalent thickness below 1 nm, such differences disappear, indicating that for ultra thin layers, direct tunneling becomes dominating.

11.7 Influence of Interface Engineering

Epitaxial growth of lanthanide oxides on silicon without any interfacial layer has the advantage of enabling defined interface engineering. Here, we will show that a controlled preparation of the clean (2 × 1) reconstructed silicon surface prior to the Gd_2O_3 growth can create two completely different interfaces; one of them we call as "oxygen-enriched or oxide-like" interface while the other is a "stoichiometric or silicate-like" interface. The influence of the two different interfaces on the electrical properties of the metal/oxide/silicon stacks will be demonstrated [32].

Oxide-like interfaces were prepared as follows. The substrate temperature was increased to 650 °C and once the surface was clean, i.e. (2 × 1) reconstructed, molecular oxygen was introduced into the deposition chamber to adjust the background partial oxygen pressure to $2 \cdot 10^{-7}$ mbar. During this procedure the substrate temperature was held at 650 °C. Just after the (2 × 1) reconstruction was converted to (1 × 1), the Gd_2O_3 was grown with a growth rate of 0.006 nm/sec

under an oxygen partial pressure of $5 \cdot 10^{-7}$ mbar. For the formation of silicate-like interfaces, we performed the following steps: After appearance of the (2 × 1) reconstruction the substrate temperature was reduced from 650 to 300 °C. Once the temperature was stabilized, Gd_2O_3 was deposited with very slow deposition rate. The deposition was interrupted when the (2 × 1) reconstruction was converted into (1 × 1) after a sub-monolayer growth of Gd_2O_3. The substrate temperature was then increased back to 650 °C with ramp rate of 50 deg/min under an oxygen partial background pressure of $1 \cdot 10^{-7}$ mbar to stabilize the oxide surface. At 650 °C, growth of Gd_2O_3 was continued with the growth rate of 0.006 nm/sec under an oxygen partial pressure of $5 \cdot 10^{-7}$ mbar. The diffraction patterns for the epitaxial Gd_2O_3 films grown do not show any differences for the two types of surface modifications.

Figure 11.11 shows the XPS Si *2p* core-level spectra for thin Gd_2O_3 films grown on the two Si surfaces. The spectra exhibit two peaks, the Si bulk peak with the maximum intensity at around 100 eV and a second peak at higher energy corresponding to interfacial silicon. The peak position of the second peak is at higher energy for the oxide-like surface in comparison to the layer grown on the silicate-like silicon substrate. This confirms an oxygen-rich (oxide–like) bonding configuration at the interface for the first case and a metal-O–Si (silicate-like) bonding in the second case [22]. We also investigated the O *1s* and Gd *4d* spectra of Gd_2O_3 thin films with two different interfaces (not shown). Although the interface has minimum impact on those spectra, however, these confirm that Gd metal (140.0 eV) is fully oxidized (Gd^{+3}, 143.5 eV) with corresponding chemical shift of 3.5 eV toward higher binding energy. Results of ab initio model calculations for these two interfacial structures can be found in Ref. [33]. From the corresponding valence band spectra, the valence band maximum (VBM) was estimated following a procedure described elsewhere [12]. The VBM was found to be greater by 0.6 eV in case of the silicate-like interface, which is in complete agreement with a previously reported result [33].

Figure 11.12 shows the capacitance–voltage (C–V) characteristics of two epitaxial 4.2 nm thick Gd_2O_3 films with oxide-like and silicate-like interfaces, respectively, measured at 10 kHz. As anticipated, an epi-Gd_2O_3 film with silicate-like interface layer exhibits much higher accumulation capacitance and hence shows lower capacitance equivalent thickness. The CET values estimated from accumulation capacitance are 1.1 and 0.76 nm for the films with oxide- and silicate-like interface, respectively, while calculated effective dielectric constants are 12.0 and 18.9, respectively. The disparity in the dielectric constants for two differently processed thin films can be understood from the parasitic effect of interfacial layers where oxide-like interface has much lower dielectric constant than silicate-like. The EOT value (including quantum–mechanical corrections) is always significantly lower than *CET*, thus, one would finally be able to achieve an ultra-low EOT for such epitaxial Gd_2O_3 layer with a silicate-like interface. We also compare the leakage current density of epitaxial Gd_2O_3 thin films grown on the two surfaces. The current density estimated at $(Vg - V_{FB}) = 1$ V for two 4.2 nm thick films are 15.0 and 30.5 mA/cm^2 with silicate-like and oxide-like

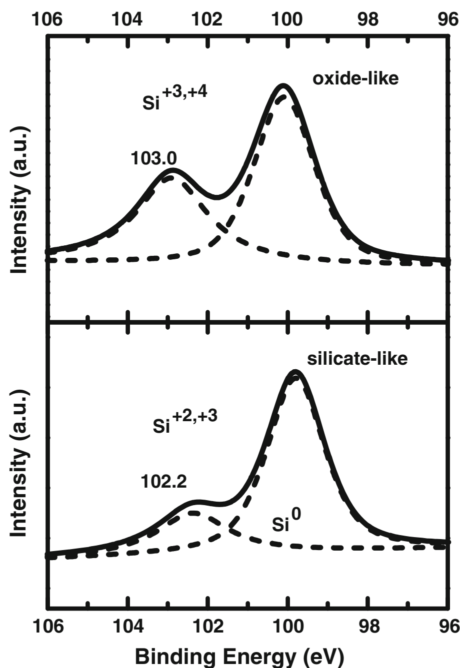

Fig. 11.11 Core-level XPS spectra of Si-2*p*, for Gd_2O_3 layers grown on the two differently prepared Si surfaces

interface, respectively. The films with silicate-like interface show reasonably lower leakage current compared to the films with oxide-like interface. That behavior can be understood from the formation of dipoles at the Gd_2O_3/Si interface originating from the accumulation and/or depletion of oxygen atoms for two the different growth procedures. Hence, the difference in stoichiometry at the interface eventually influences the band offset values [18, 34]. For example, the valence band offset for epi-Pr_2O_3 layer with silicate-like interface was found to be larger than that with oxide-like interface [18]. This likely resulted in a reduced hole current observed in our layers.

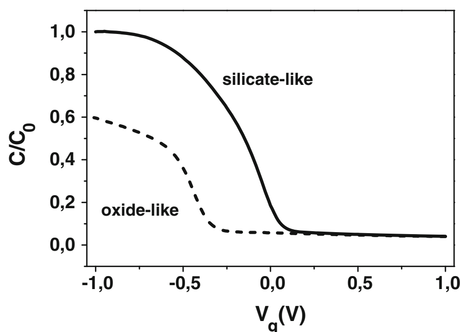

Fig. 11.12 Capacitance–Voltage (C–V) characteristics of epitaxial 4.2 nm thick Gd_2O_3 thin films with oxide- and silicate-like interfaces on p-type Si substrates, measured at 10 kHz

The incorporation of few monolayers of Ge chemisorbed on the Si surface has been found to have significant impact on the electrical properties of crystalline Gd_2O_3 grown epitaxially on Si substrates [35]. Although the Ge coverage on Si surface does not show any influence on the epitaxial quality of Gd_2O_3 layers, however, it exhibits a strong impact on their electrical properties (Fig. 11.13). We show that by incorporating few monolayers of Ge at the interface between Gd_2O_3 and Si, the capacitance–voltage characteristics, fixed charge and density of interface traps of Pt/Gd_2O_3/Si capacitor are much superior to those layers grown on clean Si surfaces.

Summarizing, we have shown that the electrical properties of epitaxial Gd_2O_3 thin films on Si substrates were improved significantly by an atomic control of interfacial structures due to a proper treatment of silicon surface prior to the Gd_2O_3 growth. The interface structure and its chemical composition play therefore the key role on the electrical performance of any MOS devices also in the future.

Recently, we reported on the effect of carbon doping on electrical properties of epitaxial gadolinium oxide grown on Si substrates [36]. The incorporation of small amounts of carbon (0.2–0.5 vol. %) into epitaxial Gd_2O_3 has been found to be very useful in improving the electrical properties especially by reducing the leakage current behavior. The doping has a negligible impact on the structural quality of the oxide layer. We also showed that the very often found adverse effect of oxygen vacancy induced defects in oxides grown at higher temperature can be eliminated by moderate amount of carbon doping during growth. The incorporated C amount should be below 1 % as higher C concentrations (>2 %) into Gd_2O_3 degrades the electrical properties by forming additional type of defects.

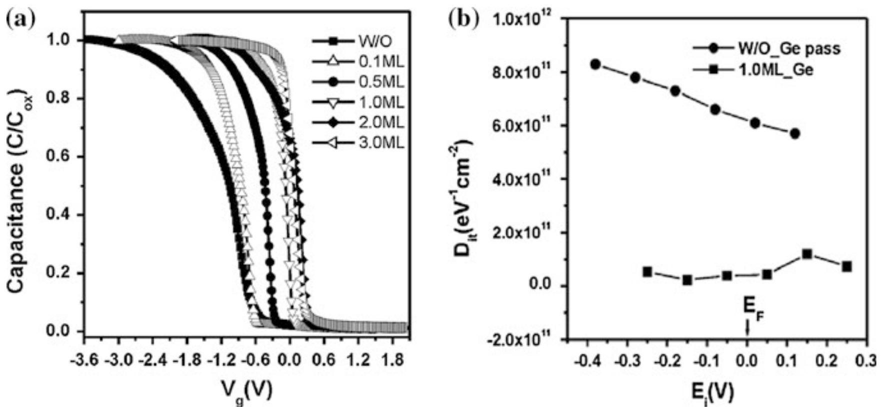

Fig. 11.13 **a** The C–V characteristics of Pt/Gd_2O_3/Si(111) MOS capacitors as a function of Ge coverage. The flat band voltage increases monotonically with increasing Ge coverage, inferring a strong influence of Ge adatoms on Si surface. **b** Density of interface traps of capacitors fabricated on clean and Ge passivated wafers, exhibiting significant improvement on D_{it} values

11.8 Impact of Post-Growth Processing

The *bixbyite* structure of Gd_2O_3 is based on the calcium fluorite structure, where 1/4 of the oxygen atoms have been removed from specific lattice sites. That structure has a lattice symmetry suitable for epitaxial growth on Si(100) with a lattice mismatch of ~0.5 %. Although the mismatch is small, we have to face a bonding mismatch, i.e. a large number of dangling bonds. Recently, we introduced the traditional forming gas anneal to study its impact when applying to the novel single crystalline gate stacks [37].

To fabricate MOS structures, tungsten metal electrodes with an area of 10^{-3} cm^2 were evaporated by e-beam evaporation through a shadow mask in a separate chamber. The wafer was cut into small pieces for the annealing experiments. All structures were annealed in forming gas for 10 min at 450 °C. Electrical characterizations such as *C–V* and *I–V* measurements were performed at room temperature.

Figure 11.14 shows the normalized capacitance–voltage (*C–V*) characteristics of single crystalline Gd_2O_3 on Si(100) substrate with W as top electrode. Although the accumulation and depletion regions are clearly visible, the curves suffer from flat-band voltage instabilities. The flat-band voltage is determined by the slope of $d[1/(C_{hf}/C_{ox})^2]/dV_G$. From sweep 1 to the sweep 8, the flat-band voltage reduced from −0.44 to −1.36 V. A big amount of positive fixed charge is created during the *C–V* sweeping.

Unlike as-grown samples, the V_{FB} of the forming gas annealed samples is quite stable (−0.44 V) indicating the passivation of the slow interface states. The fixed oxide charges are calculated to be $2.3 \cdot 10^{12}$/cm^2 based on the equation: $Q_f = C_{ox} \cdot (\Phi_{ms} - V_{FB})$. Figure 11.15 depicts the hysteresis of the structure. The cycles are completed by from 1.5 to −2.5 V and −2.5 to 1.5 V with the step of 10 mV for 5 times. As we can see from the figure, there is almost no hysteresis (<10 mV) detectable during the five sweeps (only the first sweep is shown in

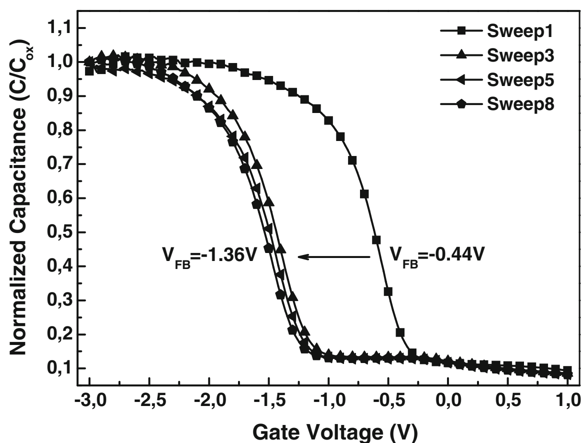

Fig. 11.14 Normalized Capacitance-Voltage (*C–V*) characteristics of single crystalline Gd_2O_3 on Si(100) substrate with W as top electrode. The flat-band voltage reduced from −0.44 to −1.36 V with the number of sweeps

Fig. 11.14 for clarity). Based on above results, the conventional forming gas annealing is compatible to novel single crystalline W/Gd_2O_3/Si(100) structure.

The leakage current of W/Gd_2O_3/Si(100) (with CET = 2.2 nm) is only $2 \cdot 10^{-6}$ A/cm_2 at $V_{FB} - 1$ V, four orders of magnitude lower than the as-grown samples, which is also much lower than that of SiO_2 at the same CET.

To evaluate D_{it} we measured the equivalent parallel conductance (G_p) of MOS capacitor as a function of gate bias and frequency (the details of the calculation method have been described elsewhere [21]). The conductance in the present case was measured at flat-band voltage condition. D_{it} was calculated to be only $8.8 \cdot 10^{11}$/cm^2 eV after the forming gas anneal.

In summary, the as-grown single crystalline Gd_2O_3 thin film on Si(100) substrate suffers from flat-band voltage instability and large hysteresis which are possibly due to the intrinsic dangling bonds induced by the existing bonding mismatch at the oxide/silicon interface. The instability of flat-band voltage and hysteresis can be fully eliminated by the introduction of traditional forming gas annealing.

In the following, we will discuss changes in structural and dielectric properties of uncapped and capped crystalline Gd_2O_3 layers on Si as the result of different rapid thermal annealing (RTA) process conditions commonly used in MOSFET fabrication [38]. Layers of different thicknesses were grown on p-type Si(100) and Si(111) substrates. On Si(100) substrate, the grown layers exhibit the known two types of (110)-oriented domains, with two orthogonal in-plane orientations. On (111) oriented Si surface, *bixbyite* Gd_2O_3 can grow single crystalline. After growth, the wafers were cut into smaller pieces. Each piece was first structurally characterized in the as-grown state using x-ray techniques. All variations across a wafer were found to be within the error ranges of the used techniques, thus, we have a sufficiently high homogeneity. Then, the uncapped pieces were annealed in different ambients for 30 s in a commercial RTA system. For each annealing batch, we used pieces from the same wafer. The layer thickness was measured by x-ray reflectivity (XRR). To obtain the best fit, we used a three layer model, where

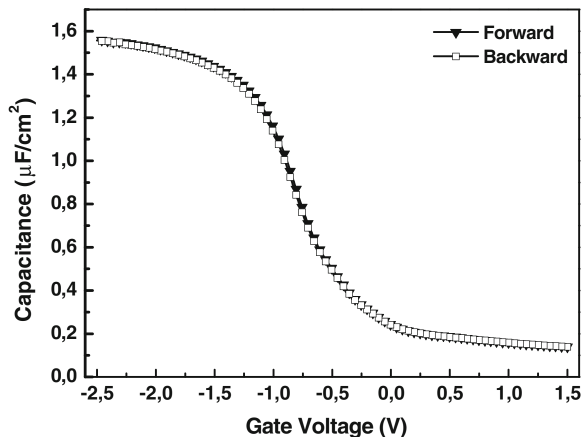

Fig. 11.15 Hysteresis characteristics of single crystalline Gd_2O_3 on Si(100) substrate after forming gas anneal at 450 °C for 10 min with W as top electrode. V_{FB} is stabilized at −0.44 V. Only the first sweep is shown for clarity

the first layer describes the interfacial transition between substrate and the gadolinium oxide layer, the second the high-k layer, and the third considers possible reactions of the oxide with atmospheric H_2O and CO_2 [39]. We always used the overall thickness of all three layers for evaluating annealing effects on layer thicknesses. Figure 11.16 summarizes the results for annealing the uncapped films in pure nitrogen. Up to 800 °C, we do not observe any changes in the overall layer thickness. At higher temperature, the layer thickness increases with annealing temperature. Below 1,000 °C RTA, substrate orientation has no effect on the observed thickness changes.

Layers were also characterized by X-ray diffraction (XRD) and transmission electron microscopy (TEM). Figure 11.17a shows XRD $\theta/2\theta$ scans for a 8 nm thick layer grown on Si(100) and annealed at different temperatures in nitrogen. Besides the substrate peaks (not shown), the only detectable peak around 47.4° can be assigned to the (440) reflection of Gd_2O_3 in the *bixbyite* structure. Up to 900 °C, we observe only minor changes in that peak caused most likely by relaxation effects.

The corresponding cross-sectional TEM images (not shown) reveal the following: In contrast to the as-grown crystalline Gd_2O_3 film, this layer shows an amorphous region between the silicon and the crystalline Gd_2O_3 after RTA at 900 °C. That structureless transition region consists of two layers with different contrast in TEM; the lower one can be attributed to a silicon oxide-like phase, whereas the upper one is most likely a silicate-like phase. For even higher annealing temperatures, the crystalline structure of the layer disappears completely. Thus, the high-k layer will be completely structurally degraded after annealing at 1,000 °C.

The formation of silicon oxide-like and/or silicate-like transition regions requires the presence of additional oxygen. Gadolinium, however, can only exist in the +3 oxidation state [40]. Thus under equilibrium conditions, the Gd_2O_3 bulk layer cannot act as an effective source for oxygen supply to the Si/dielectric

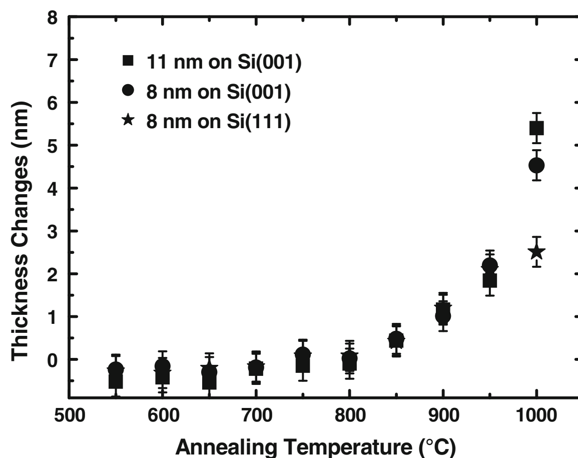

Fig. 11.16 Change in layer thickness (evaluated by XRR) for crystalline Gd_2O_3 layers grown on Si after an RTA in nitrogen for 30 s

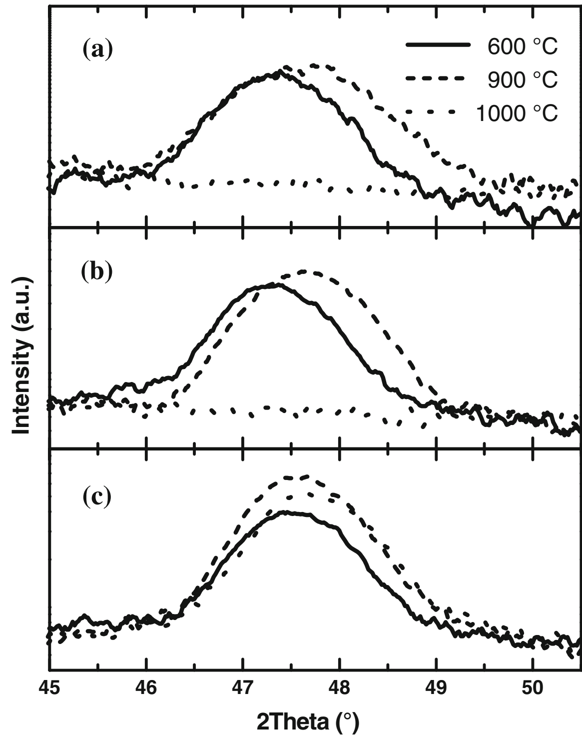

Fig. 11.17 XRD scans for Gd_2O_3 layers on Si(001) annealed at different temperatures for 30 s. in **a** nitrogen, **b** oxygen, and **c** nitrogen (with an a-Si capping layer)

interface. The observed changes can therefore only be attributed to oxygen supplied by the annealing ambient. To verify that hypothesis, we repeated the same annealing experiments in pure oxygen. In another set of experiments, we sealed the high-k layer by an amorphous, 100 nm thick Si layer in order to suppress oxygen supply from the ambient. For experiments with Si capping layer we used a four layer model for the XRR evaluation. Figure 11.18 summarizes the layer thickness variation for these two series.

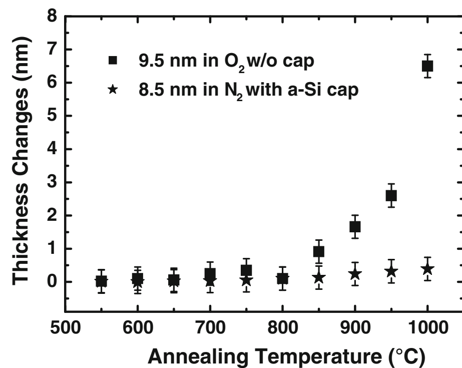

Fig. 11.18 Change in layer thickness (evaluated by XRR) for an open crystalline Gd_2O_3 layer grown on Si after a 30 s RTA in oxygen and for a layer capped with 100 nm a-Si and annealed in nitrogen

Similar to RTA in nitrogen, the layer thickness remains constant up to 800 °C also for the oxygen anneal. For higher temperature, it increases nearly exponentially with temperature. However, for the capped layers, we do not see any significant increase in layer thicknesses with temperature even up to 1,000 °C. Figure 11.16b and c show corresponding XRD measurements. Analogous to N_2 RTA, the (440) peak of the Gd_2O_3 layer disappears completely after the 1,000 °C anneal in oxygen. In contrast, the sealed high-k layer remains fully crystalline after such high temperature RTA. Here, an additional peak at 28.4° occurs (not shown in Fig 11.17c) which originates from the crystallization of the Si cap layer. All structural results support our hypothesis of oxygen supply from the annealing environment. Avoiding such oxygen in-diffusion leads to a significant stabilization of the grown layers.

For the electrical characterization of the high-k films, we prepared fully silicided (FUSI) NiSi metal electrodes on the annealed samples as described in detail elsewhere [41]. We extracted the capacitance equivalent thicknesses (CET) for the various layers from the accumulation capacitance measured at 100 kHz (Fig. 11.19). For the open layer, the CET increases as a function of annealing temperature. At the same time, the extracted effective dielectric constant remains constant within the error limits. Such behavior can be explained in two ways: Either the dielectric properties of the high-k layer degrade due to annealing or the impact of the interfacial transition increases. If a structure contains several dielectrics in series, the lowest capacitance layer will dominate the overall capacitance, and also set a limit on the minimum achievable CET value.

Electrical measurements of such a multilayer stack with the total thickness t_{total} will yield always an effective dielectric constant, k_{eff}. Detailed evaluations of the XRR measurements yield also the electronic density of the individual layers. Up to 800 °C anneals, that density of the high-k layer does not change. Let us assume that $k_{high\text{-}k}$ also does not change within that temperature range. Also from the XRR evaluation (and various cross-sectional TEM investigations, not shown here), the interfacial layer thickness remains constant around 1.5 nm up to 800 °C. The as-grown layers did not show any pronounced interfacial layer.

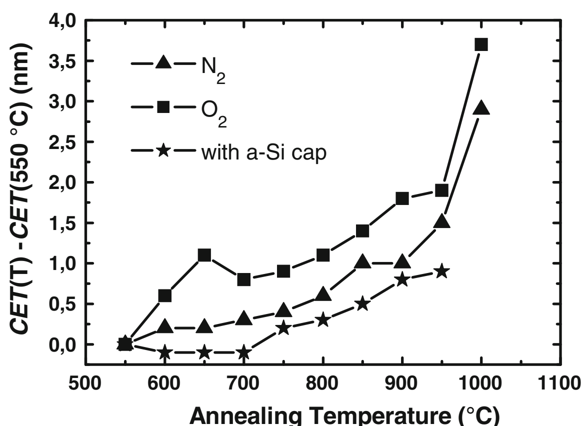

Fig. 11.19 Changes in the capacitance equivalent thickness (*CET*) extracted from C–V measurements after different annealing

Summarizing, the observed structural and electrical results up to 800 °C RTA can only be understood by a gradual transformation of parts of the crystalline oxide into a structure-less silicate-like phase with lower permittivity. The situation looks different for the sealed layers. Here the effective permittivity is nearly twice as high compared to the open systems annealed in nitrogen or oxygen, and CET increases only slightly due to annealing. The exclusion of additional oxygen retards the transformation of the Gd_2O_3 layer into a silicate layer.

11.9 Further Applications of Crystalline Lanthanide Oxides

There are several attempts to increase the material variety that is compatible with Si technologies. The ability to integrate crystalline dielectric barrier layers into silicon structures can open the way for a variety of novel applications ranging from high-k replacements in future MOS devices to oxide/silicon/oxide heterostructures for nano-electronic application in quantum-effect devices. Quantum-effect devices based on silicon are promising for future nanoelectronic application. Here, double-barrier structures using epitaxial insulators as barriers and Si as quantum-well are particularly interesting for resonant tunneling devices. The fabrication of such an epitaxial insulator/Si/insulator heterostructure requires the growth of ultra-thin, atomically flat and defect-free insulator barriers on Si, and the growth of epitaxial Si quantum-well layers on the insulator. However, this can not be achieved straightforward because of the differences in the surface free energy between the insulator and silicon. Often, the surface free energy of the insulator is much lower than that of silicon leading to Si cluster formation on the insulator. In our case, the growth of Si under common epitaxial conditions on Gd_2O_3 leads to island formation.

To obtain smooth layers, the growth process has to be modified. First, we tested low temperature deposition and surfactant-mediated epitaxy using boron, followed by a subsequent solid phase epitaxy (SPE). Our experiments clearly showed that Si does not wet the oxide layer and that Si island formation can not be prevented using conventional SPE. Also different modifications of surfactant-mediated epitaxy lead to Si islanding. We developed a new approach for nanostructure formation which is based on solid-phase epitaxy of the Si quantum-well combined with simultaneous vapor-phase epitaxy of the insulator on top of the quantum-well [42]. Ultra-thin single-crystalline Si buried in a single-crystalline insulator matrix with sharp interfaces was obtained by this approach on Si(111). Successful fabrication of single crystalline oxide/Si/oxide double-barrier nanostructure enable us to design Si-based resonant tunneling diodes (RTD), which might open up an exciting opportunity to integrate advanced quantum device functionalities into mainstream silicon based technology. Such devices utilizing epi-Gd_2O_3 as an insulator and Si as the quantum well offer many more functionalities in the future.

Apart from application of thin epitaxial layers, lanthanide oxides could also find another application in silicon nano-cluster (Si–NC) flash memories due to their thermodynamic stability on Si substrates at higher temperatures. Such nano-crystal memories represent one of the most promising candidates for future nonvolatile, high density, and low operating-voltage memory applications. Originally, the concept of Si-NC flash memories has been based upon embedding single crystalline Si clusters of few nanometers in size into the insulating gate oxide (SiO_2) of field effect transistor (FET), where Si–NCs could be used as deliberately generated trap centers for electrons and/or holes [43]. The entrapment of the charges (e.g. electrons) by these clusters embedded in the gate oxide eventually shifts the threshold voltage during the device operation by screening the gate charges and hence reduces conduction in the channel inversion layer. Electrical performance of these clusters strongly depends on their physical properties such as their size, density, and spatial distributions into the oxide as well. Thus, the most challenging task to improve the device performance has been the formation of nano-clusters with constant size, high density and uniform distribution. There are several approaches reported recently to form Si–NCs into SiO_2 and also into high-k oxides [44–46]. Replacing SiO_2 with high-k oxide in floating gate memory is advantageous since the larger capacitance enhances the drive current while high breakdown voltage and low leakage current could be maintained [27, 47] due to thicker physical thickness.

Recently, we demonstrated the controlled growth of Si-NCs incorporated into epitaxial rare earth oxide using MBE [48]. Exploiting the advantages of different thin film growth mechanisms, we were able to control the size and density of Si–NCs embedded in epitaxial Gd_2O_3 grown on Si substrates. The epitaxial rare earth oxide, if deposited by MBE, exhibits superior crystal quality and therefore allows better control over the scaling in future devices [49]. C–V characteristics of Pt/Gd_2O_3/Si MOS capacitors with embedded Si–NCs grown on different silicon substrates were measured at different frequencies. Significant shift of flat band voltage (ΔV_{FB}) due to a large number of electrons and holes captured by the Si–NCs could be observed for all cases. The positive shift in V_{FB} (for n-substrates) observed after charging of clusters indicates the trapping of electrons, which effectively screen the electric field at the gate and hence the measured flat band voltage is shifted. The reverse effect is observed for p-type substrates where the majority of trapped charges are holes. It is worth to remember here that the Gd_2O_3 layers with no Si-NCs display negligible hysteresis in C–V measurements. The density of the nano-cluster estimated from the flat band shift is about $4.2 \cdot 10^{12}\ cm^{-2}$ assuming one electron per cluster. This value turns out to be twice than that estimated from Atomic Force Microscopy (AFM) investigation, implying that the one-electron per cluster assumption does not fit to our devices. However, if we assume that the average number of electrons captured by one single cluster is two, it would result in a cluster density of around $2.1 \cdot 10^{12}\ cm^{-2}$, in good agreement with the AFM results.

In Ref. [49], we showed in detail structural and electrical properties of high performance nonvolatile Si nano-cluster memories with epitaxial Gd_2O_3 as a

control and tunneling layer. Clusters with average size of 5 nm and density of $2 \cdot 10^{12}$ cm^{-2} exhibit excellent charge storage capacity with competent retention ($\sim 10^5$ s) and endurance (10^5 write/erase cycles) characteristics. The Pt/Gd_2O_3/Si MOS capacitors comprised with Si nano-clusters displays large hysteresis ($\sim$1.5–2 V) in capacitance–voltage measurements. These Si nano-clusters are bonded via Gd–O–Si bonds to the metal oxide. Thus, Si nano-clusters embedded in an epitaxial rare earth oxide could be a potential contender for future non-volatile memory devices.

So far we have demonstrated the major areas where rare earth oxide thin films could offer optimistic solution for future devices with ultra-scaled dimension. However, there are many more areas where these oxide thin films could find potential application too. Here, we will briefly overview some of the devices, which also could be realized with crystalline lanthanide oxide thin films: (a) for spintronics: The presence of localized strongly correlated 4f electrons is responsible for the magnetic behavior. Thus, rare earth materials can be considered as candidates for future spin based electronic devices [50–52]. The strong exchange coupling between the localized rare earth 4f spins and valence and conduction electrons leads to interesting magnetic properties [53, 54]. However, such coupling may often be destroyed by the presence of any impurity inside the crystal. Recent demonstration of single crystalline thin films grown by molecular beam epitaxy on semiconductor substrates may pave the way to build the future devices utilizing rare earth compounds. Combining the advantage of large dielectric constant and high magnetic moment of rare earth materials one could able to design a system, which might exhibits high magnetic moment in coexistence with large dielectric constant. (b) For optical application: Materials combining selective emission with thermo-structural properties such as a good resistance to thermal shocks or to large temperature cycles are very interesting for a variety of different applications ranging from aerospace to energy conversion [55]. Among the most effective materials with selective emission properties at high temperature (1,000–2,000 °C), rare earth oxides are certainly the most interesting ones, thanks to their high melting temperature and to peculiar electronic properties of rare earth elements that have particularly empty 4f levels inside the 5p and 5s shells and the 6s valence states and therefore retain some atomic like optical properties in a variety of different bonding environments. As rare oxide materials emit thermal radiation in narrow spectral region, they can be used for a variety of different high temperature application such as generation of electricity by thermo photovoltaic conversion of thermal radiation.

11.10 Summary and Outlook

We described the use of molecular beam epitaxy to grow epitaxially lanthanide oxide thin films on silicon. We presented results for crystalline gadolinium oxide in the cubic *bixbyite* structure. On Si(100) oriented surfaces, crystalline Gd_2O_3 grows

as (110)-oriented domains, with two orthogonal in-plane orientations. We obtain perfect epitaxial growth of cubic Gd_2O_3 on Si(111) substrates. Layers grown under best vacuum conditions often exhibit very high leakage currents. Deliberate oxygen supply during growth improves the dielectric properties significantly; however, too high oxygen partial pressures lead to an increase in the lower permittivity interfacial layer thickness, and finally limit the achievable minimal equivalent oxide thickness. Experimental results for Gd_2O_3-based MOS capacitors grown under optimized conditions show that these layers are excellent candidates for application as very thin high-k materials replacing SiO_2 in future MOS devices.

We also reported the impact of interface layer composition on the electrical properties of epitaxial Gd_2O_3 thin films on Si(100) substrates. The electrical properties of epitaxial Gd_2O_3 thin films were improved significantly by controlled modification of the interface layer composition. The minimum capacitance equivalent thickness estimated for Pt/Gd_2O_3/Si MOS structures was as low as 0.76 nm with leakage current density of 15 mA/cm^2 at $(V_g - V_{FB}) = 1$ V.

We investigated the effect of post-growth annealings on the layer properties. We showed that a standard forming gas anneal can eliminate flat-band voltage instabilities and hysteresis as well as reduce leakage currents by saturating the dangling bonds caused by the bonding mismatch. In addition, we investigated the impact of rapid thermal anneals on structural and electrical properties of crystalline Gd_2O_3 layers grown on Si with different orientations. The degradation of layers can be significantly reduced by sealing the layer with a-Si prior to annealing. For the capped layers, the effective capacitance equivalent thickness increases only slightly even after a 1,000 °C anneal.

Finally, we demonstrated that the epitaxial rare earth lanthanide layers can be successfully used to realize several novel devices. Double-barrier insulator/Si/insulator nanostructures on Si(111) have been grown using a new approach which is based on solid-phase epitaxy of the Si quantum-well combined with simultaneous vapor-phase epitaxy of the insulator on top of the quantum-well. Other interesting structures are formed by single-crystalline high-k oxide layers with embedded Si nano-clusters. They present one of the most promising candidates for future nonvolatile, high density, and low operating-voltage memory applications.

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