Design and Implementation of Dynamic Reliable Virtual Channel for Network-on-Chip

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Abstract. Reliability issue such as soft error due to scaling IC technology, low voltage supply and heavy thermal effects, has caused fault tolerant design be a challenge for NoC(Network-on-Chip). The router is a core element of the NoC, and the virtual channel based on flip-flop which occupies most of the area is the most sensitive element to soft error of the router. Focus on this problem, a dynamic reliable virtual channel architecture is proposed in this paper. It can detect the utilization of the virtual channel to adjust physical configuration to support for no-protection, dual redundancy and TMR (triple modular redundancy) requirements in flexibility. Compared with typical TMR virtual channel design, the synthesis results show that our method can achieve several fault tolerant structures switch with near 3 times resource utilization in ideal case and only 13.8% extra area cost.

Keywords: NoC, reliable, virtual channel, dynamic structure.

1 Introduction

With the rapid development of IC technology, more and more IP cores will be integrated on one chip. But the traditional bus based SoC design will meet many problems, such as the integration and reusability of IP cores. An efficient solution to these problems is NoC, which has regular structure and much higher bandwidth due to multiple concurrent connections. But the shrinking feature size makes more transient faults, including crosstalk, charge sharing and SEU (Single Event Upset) [1], which will degrade the NoC performance even result in system crash. So reliability research has become a hot spot of NoC design.

The router is one of the core elements of NoC, because the packet transmits in NoC through the router. Virtual channel, which is the main buffer of the router, is the most sensitive element of the router. We find that reliable virtual channel has become a challenge for NoC design since that virtual channel consumes about 46% of power [2] and 75% of area of the router [3]. At the same time, different applications or even the same application such as H.264 may have different reliability requirements. So it is important to design a reliable virtual channel which can support different reliability requirements.

In this paper, we propose a reliable virtual channel design, which can detect the utilization of the virtual channel to adjust the redundancy structure to support for

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no-protection, dual redundancy and TMR requirements. Major benefit of the proposed design over its counterparts is: it can exploit the inherent redundancy to meet different fault tolerant requirement.

The rest of this paper is organized as follows. Related work will be described in Section 2. Basic background and router structure will be described in Section 3. The proposed reliable virtual channel design will be described in Section 4. The results and comparison is presented in Section 5. Conclusion is drawn in Section 6.

2 Related Work

Reliability research of NoC has become a hot spot from different aspects, including retransmission mixed with error detection, spare link or router, triple modular voting structure and fault tolerant routing algorithm. Murali etc [4] proposed an error detection and recovery scheme for NoC design based on area, power and performance constraints. Yung-Chang Chang etc [5] proposed a fault tolerant NoC architecture using spare routers. Fault tolerant routing algorithms, including stochastic and adaptive, have been suggested in many papers [6-7].

The research and design above are mostly based on system level, and analyzed by the simulator. There are also some researches aiming at implementation of the element of NoC. Shih-Hsun Hsu etc implemented a router for ANoC [8]. M. H Neishaburi etc [9] proposed an enhanced reliability aware NoC router for permanent error.

In this paper, different from previous works, we design and implement a virtual channel support for different reliability requirements by the Verilog HDL and compare the area cost with the traditional designs.

3 Basic Router Architecture

In order to introduce proposed virtual channel design, we give the basic router microarchitecture as Fig 1 shows. In most of wormhole flow control mechanism based

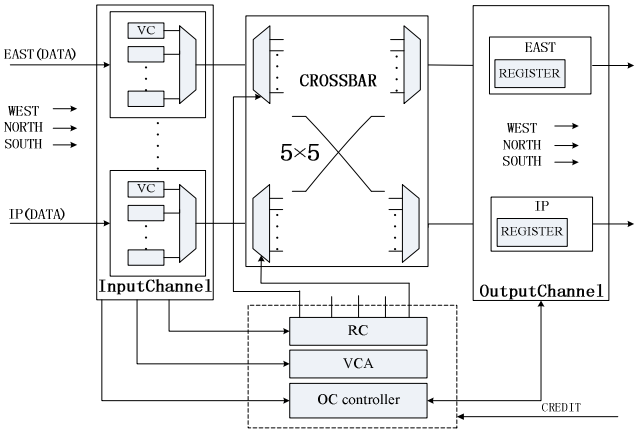

Fig. 1. Basic router microarchitecture

design, virtual channel is allocated in input channel. And it is the main buffer in the router. There are also some combinational logic part, such as routing computer part (RC), virtual channel allocator (VCA) and crossbar. The data packet will be divided into many flits to transmit in NoC, and one head flit will be added to control the data flow. The head flit will work in RC and VCA to decide which port and which virtual channel to flow. But the data flit, which carries the data payload, will stay in virtual channel for several cycles. So the virtual channel needs to be protected.

4 Proposed Reliable Virtual Channel Design

Our virtual channel design includes three aspects: 1) Flit format needs to be modified, which demands 3 extra bits. Two of them denote RR (Redundancy-Requirement), 00 means that the flit has no reliability requirement, 10 means the flit is dual redundancy data, 11 means the flit has TMR requirement. The other bit is parity check bit, which is support for dual redundancy data. And the new flit format also needs extended link, crossbar and FIFO bandwidth support. 2) The virtual channel needs to be re-designed, which is shown in Fig 2, including extra status registers (VC-Org and Friend-VC) to generate the redundancy structure signals and two auxiliary pointers to maintain two or three copies read and written in one cycle. 3) The router pipeline needs to be changed, which requires two stages, VC-in-configure and VC-out-configure to control the write and read of the virtual channel.

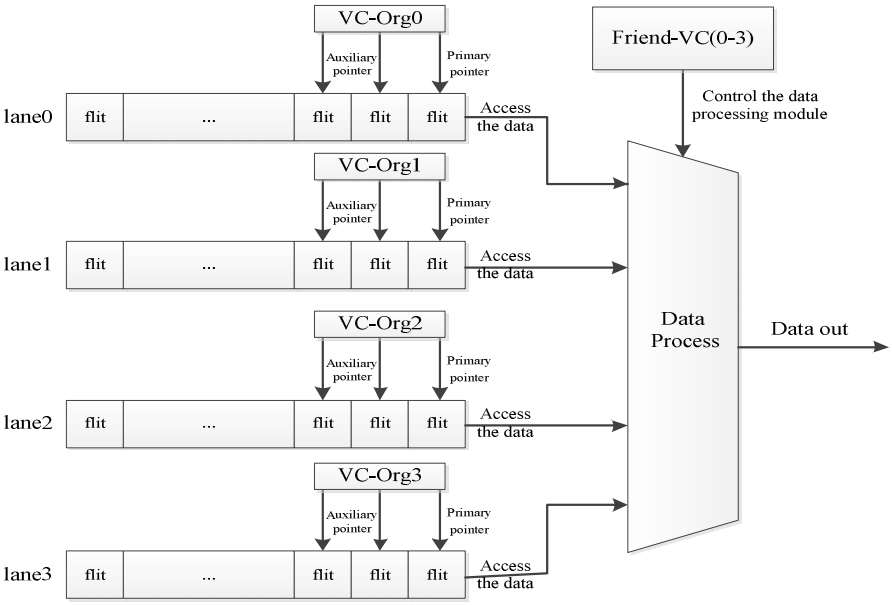

Fig. 2. Proposed Virtual Channel Architecture

VC-in-Configure: The function of this stage is to determine the redundancy structure of the virtual channel when the flit writes. The flowchart of the stage is shown in Fig 3. When a head flit will be written into the virtual channel, RR will be decoded at first.

- If RR is 00, which is region 1 in Fig 3. It means the packet (all flits after the head flit and before another head flit) has no reliability requirement. The flit will be stored in the virtual channel lane which is be allocated in the VCA, and the status registers of the lane will be the initial value.
- If RR is 10, which is region 2 in Fig 3. It means the packet has dual redundancy requirement (with parity check). Then we will check if there are two empty lanes in the virtual channel, just because only the empty lane is available in the wormhole flow control mechanism. If there are two empty lanes in the virtual channel, the flit will be stored in the two lanes. And each lane has a status register called Friend-VC as shown in Fig 2, which record the lane that stores the same flit with this lane. It achieves the transverse redundancy structure. If there is only one empty lane in the virtual channel, the flit will be stored in this lane twice with the help of the two auxiliary pointers of the FIFO as shown in Fig 2. It means the continuous two flits save the same data and it achieves the longitudinal redundancy structure, which is recorded in VC-Org.
- If RR is 10, which is region 3 in Fig 3. It means the packet has TMR requirement. Similar to dual redundancy, if there are three empty lanes in the virtual channel, the flit will be stored in the three lanes, otherwise the flit will be stored in the lane for three times. At the same time, Friend-VC and VC-Org will be update to record the redundancy structure of the virtual channel.

VC-Out-Configure: The function of this stage is to export the protected data when there is a read request of the virtual channel, as shows in Fig 4. When there is a read request of a lane, we will check its VC-Org at first.

- If VC-Org is 00, which is region 1 in Fig 4. It means it is single mode state. Then we will check the RR, if it is 00, it means the data has no reliability requirement, and export the data of lane directly. If RR is 10, it means the data is dual redundancy data, but the lane is single mode, so its redundancy data is in another lane. We will check the Friend-VC to take the redundancy data and use a dual mode voter and the parity check bit to get the protected data. If RR is 11, it means it is TMR data. We will check the Friend-VC to get other two redundancy data and use a triple mode voter to get the protected data.
- If VC-Org is 10, which is region 2 in Fig 4. It means the lane is dual mode state. We will use one auxiliary pointer to get two data in one cycle. Then we will use a dual mode voter and the parity check bit to check and export the protected data.
- If VC-Org is 11, which is region 3 in Fig 4. It means the lane is triple mode state. We will use the two auxiliary pointers to get three data in one cycle. Then we will use a triple mode voter to arbiter and export the protected data.

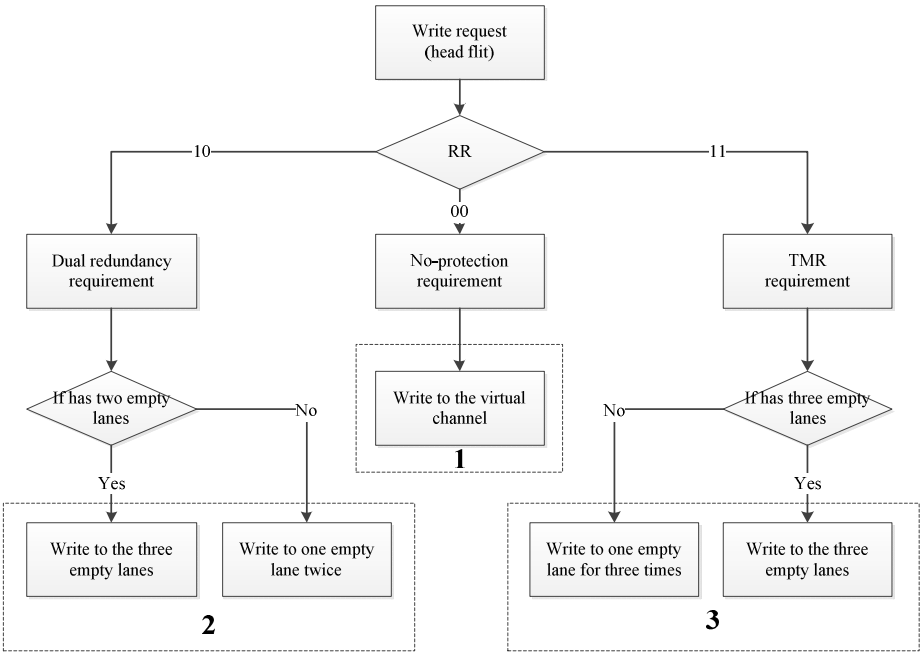

Fig. 3. VC-in-configure flowchart

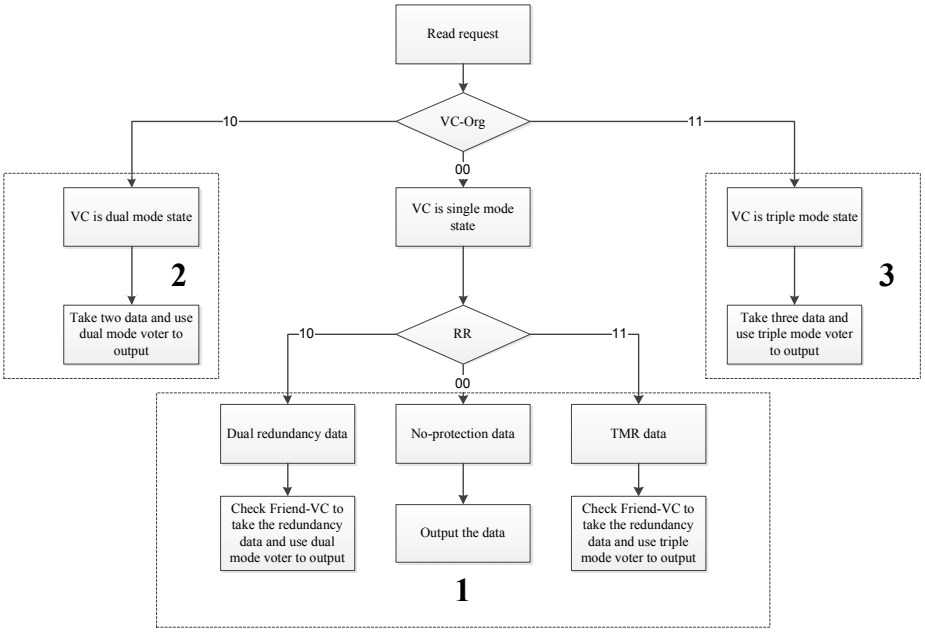

Fig. 4. VC-out-configure flowchart

5 Experimental Result

5.1 Efficiency Analysis

We have implemented three kinds of virtual channel by Verilog HDL, the basic design which has no protection [8], the typical TMR virtual channel and the proposed design. The typical TMR virtual channel uses three lanes to support TMR requirement. In our all designs, there are 4 lanes in one input port, and each size is 6 flits.

To evaluate reliability of the proposed design, we use the single error model, which means there is only one error at the same time. But the error can be one bit or several bits. Simulated by ModelSim, we find dual redundancy requirement can protect the data from the one bit error, and TMR requirement can protect the data from the multi-bit error in one flit. It confirms that proposed design has the expected goal.

At the same time, the proposed design can use transverse structure when the load of NoC is low to improve the throughput, and when the load is high it can be switched to vertical structure to reduce the congestion. For example, in ideal case, if the load is low enough, the typical TMR design based vertical structure need two more flits in the virtual channel to store the redundancy data, but at the same time the proposed design can be switched to transverse structure to get better performance. We extended cycle accurate simulator Nirgam [10] to support the proposed design. We select 4x4Mesh with typical XY routing. The packet accruing strategy is CBR (Constant Bit Rate). And each port includes 4 VCs and the buffer size per VC is 6. At the low load, the typical TMR design is like each VC size is 2 and the proposed design will be still 6. The simulation result shows that at low load the throughput of the proposed design is about 2.66 times of the typical TMR design and the average flit latency of the proposed design is about 41.1% of the typical TMR design. It means the resource utilization of our design may be near 3 times of the typical TMR design in ideal case.

5.2 Cost Evaluation

After verifying the fault tolerant performance of the proposed design, we synthesize the three Verilog RTL model based on TSMC 130nm cell library by Synopsys Design Compile. In the corner of typical operation, we have set up the constraint, with rise time, fall time and skew value of the clock of 0.1 ns, and input delay and output delay of 0.2ns, also we set the set_max_area of 0 to get the least area of the frequency, and compared with the traditional router design, we set the frequency as 200MHz and the buffer size is 6 flits. The parameters are shown in Table 1. We can find that the typical TMR virtual channel needs about 11.1% extra area cost to support the reliability requirement. And the proposed design achieves the dynamic structure to get better performance with about 13.9% area cost compared with the typical design.

Table 1. Synthesize parameter results

	Frequency	Buffer size	Area
Basic VC design	200MHz	6 flits	$89428.625\mu m^2$
Typical TMR VC	200MHz	6 flits	$99376.414\mu m^2$
Proposed design	200MHz	6 flits	$113127.18\mu m^2$

6 Conclusion

In this paper, we design and implement a new virtual channel of NoC which can achieve different reliability requirements with dynamic redundancy structure. The main contribution of the proposed design is it can detect the utilization of the NoC to adjust the redundancy structure to get better performance.

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