Variation-Aware Circuit Macromodeling and Design Based on Surrogate Models

Ting Zhu, Mustafa Berke Yelten, Michael B. Steer, and Paul D. Franzon

Department of Electrical and Computer Engineering,
North Carolina State University, Raleigh, NC 27695, U.S.A.
{tzhu,mbyelten,mbs,paulf}@ncsu.edu

Abstract. This paper presents surrogate model-based methods to generate circuit performance models, device models, and high-speed IO buffer macromodels. Circuit performance models are built with design parameters and parametric variations, and they can be used for fast and systematic design space exploration and yield analysis. Surrogate models of the main device characteristics are generated in order to assess the effects of variability in analog circuits. A new variation-aware IO buffer macromodel is developed by integrating surrogate modeling and a physically-based model structure. The new IO model provides both good accuracy and scalability for signal integrity analysis.

Keywords: Surrogate Modeling, Macromodel, Variation-Aware, Circuit, Device Model, Design Exploration, IO Buffer.

1 Introduction

Advances in integrated circuit (IC) technologies have enabled the single-chip integration of multiple analog and digital functions, resulting in complex mixed-signal Systems-on-a-Chip (SoCs). However, as the IC technology further scales, process variations become increasingly critical and lead to large variances in the important transistor parameters. As a result, circuit performance varies significantly, and some circuits may even fail to work. The large process uncertainties have caused significant performance yield loss. In addition, reliability issues and environmental variations (such as supply voltage and temperature) contribute to further yield reduction and make it more challenging to create a reliable, robust design. In handling this problem, it is important to consider the effects of variations in circuit modeling and design analysis at an early stage. However, this is a nontrivial task. In this paper, we apply surrogate modeling to handle the complexities in variation-aware circuit macromodeling, design analysis, and device modeling. We demonstrate the benefits of using surrogate modeling in enhancing the accuracy, flexibility, and efficiency in those applications.

2 Circuit Performance Macromodeling with Variations

2.1 Overview of the Method

Circuit designers are confronted with large design spaces and many design variables whose relationships need to be analyzed. In this situation, tasks such as sensitivity

N. Pina et al. (Eds.): *Simulation & Modeling Methodologies, Technologies & Appl.*, AISC 197, pp. 255–269.
DOI: 10.1007/978-3-642-34336-0_17

analysis, design space exploration, and visualization become difficult, even if a single simulation takes only a short period of time. The analyses are getting impractical as when some of the circuit simulations are computationally expensive and time-consuming. Moreover, when variations are considered in a circuit design, the situation becomes even more complex. One way to reduce the design complexities and costs is to build performance models which can be used as replacements for the real circuit performance responses.

In this work, performance models are built by directly approximating circuit performance parameters (e.g. S-parameter, gain, power consumption, noise figure, etc.) with design variables (e.g. transistor size, bias voltage, current, etc.) and parametric variations (e.g. V_{th}, t_{ox}, L_{eff}). The idea is illustrated in Fig. 1. This method is data-driven and black-box by nature, and thus it can be applied to a wide range of circuit design problems.

2.2 Model Construction

Techniques. Global surrogate modeling [1] is used to create performance models with good accuracy over the complete design space. This is different from building local surrogate model for the purpose of optimization [2].

Surrogate modeling accuracy and efficiency are determined by several key factors including the sampling plan, model template, and validation. These factors are the three steps in surrogate modeling. Multiple techniques are available and they need to be carefully selected according to the nature of the problem and computational complexity.

In the first step, the key question in designing the sampling plan is how to efficiently choose samples for fitting models, considering that the number of samples is limited by the computational expense. Traditionally, methods such as Latin Hypercube sampling or orthogonal arrays, is used for one-shot sampling [3]. Recently, adaptive sampling techniques were developed in order to achieve better efficiency in sampling [4, 5]. Adaptive sampling is an iterative sampling process which analyzes the data from previous iterations in order to select new samples in the areas that are more difficult to fit.

In the model template selection step, the surrogate model type needs to be determined. Popular surrogate model types include Rational Functions, Kriging models, Radial Basis Function (RBF) models, Artificial Neural Networks (ANNs), and Support Vector Machines (SVMs). After the model type has been selected, model complexity also needs to be decided. Model complexity is controlled by a set of hyper-parameters which would be optimized during a modeling process.

The step of model validation establishes the predictive capabilities of the models and estimates their accuracy. One popular method is five-fold cross-validation [6] in which the training data are divided into five subsets. A surrogate model is constructed five times, each time four subsets are used for model construction and one subset is used for error measurement. Model error can be measured as a relative error, for example Root Relative Square Error (RRSE), Bayesian Estimation Error Quotient (BEEQ), etc., or an absolute error, e.g. Maximum Absolute Error (MAE), Root Mean Square Error (RMSE), etc.

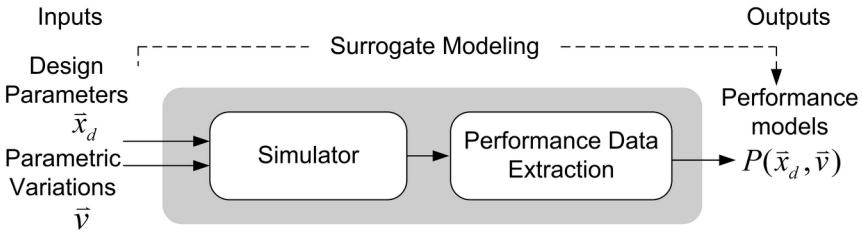


Fig. 1. Circuit performance modeling

Automatic Modeling Flow. In this work, we constructed an automatic modeling flow that is able to generate performance models from transistor-level circuit simulations, as shown in Fig. 2. Before the modeling starts, a set of input and output parameters are defined. The modeling techniques are also configured, including the model template, adaptive sampling strategy, and accuracy measurement. An accuracy target is defined as well. At the beginning of the modeling process, a small set of initial samples are generated. Then transistor-level SPICE simulations are performed using this initial set, and the corresponding responses are collected and used as the modeling data. Surrogate models are then constructed and their parameters optimized. The model accuracy is measured and the optimization continues until only negligible improvements can be made by changing the model parameters. If the desired accuracy is not reached, the adaptive sampling is evoked to add a new set of samples. The process continues until the fit reaches the targeted accuracy. When the process finishes, the model expressions are be exported and used in the follow design steps.

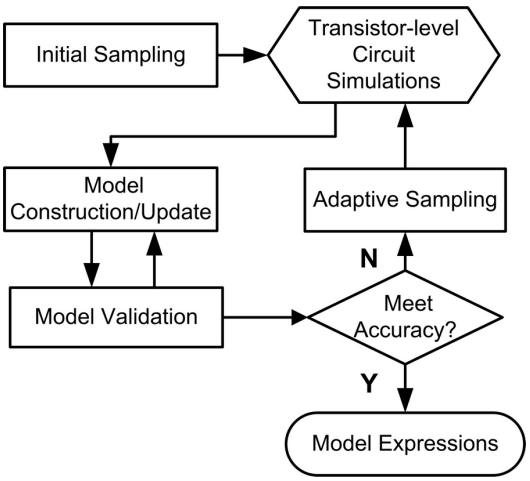


Fig. 2. Automatic adaptive performance surrogate modeling flow

In the examples presented in this section, the modeling techniques are explored using the SUrrogate MOdeling (SUMO) Matlab Toolbox [7]. SUMO is a plug in-based, adaptive platform that can be customized flexibly. The toolbox makes it feasible to test a variety of modeling techniques. Transient circuit simulators, including Cadence Virtuoso Spectre®, and Synopsys HSPICE®, are used here for performing transistor-level circuit simulations.

2.3 Circuit Case Demonstration

Performance models are very helpful for visualizing the design space and gaining insight into circuit behavior. In this section, a low-noise-amplifier (LNA) circuit is designed in a 0.13 μm CMOS process [8], the simplified circuit schematic of which is shown in Fig.3.

In this example, we consider the transistors' driving strength (*tr_strengh*) as a main source of process variations. Transistor strength describes the variations in the tran sistor speed and the current. The data is provided by the foundry and it is set between -3σ and +3σ. Additionally, temperature is considered as an environmental variation, and it varies in the range of -20°C to 60°C. Two design parameters are considered. One is reference current I_{ref} which is used to generate the input DC bias. I_{ref} is set in the range of 50 μA to 200 μA. The other parameter is mlna which is the multiple of the widths of the amplifier transistors M1and M2. mlna is in the range of 0.5 to 2. Here the performance of interest is the voltage gain at the center frequency (*maxlnagain*).

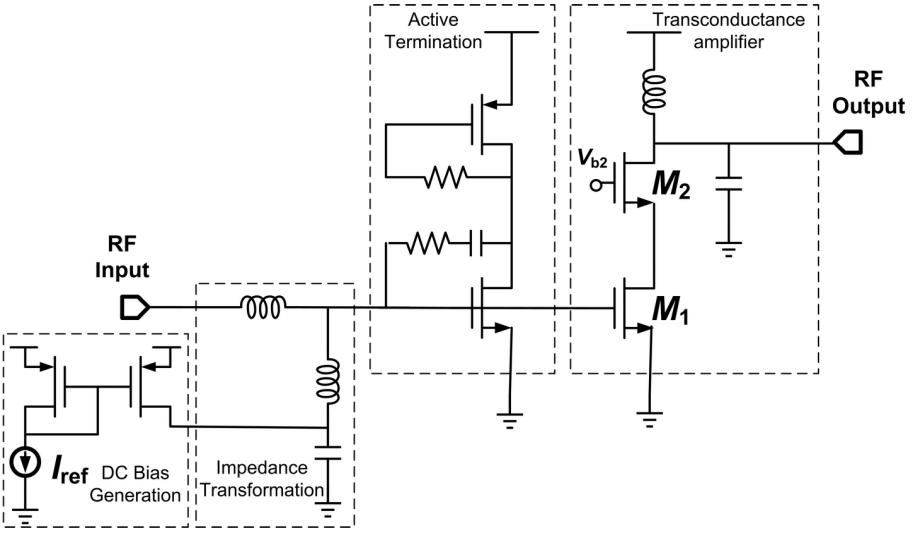


Fig. 3. Simplified low-noise-amplifier circuit schematic

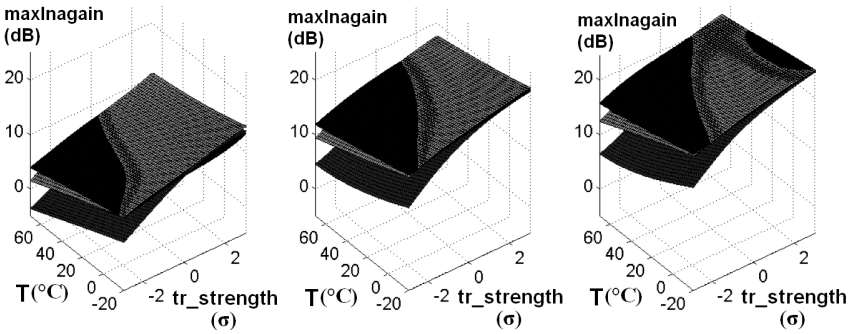
The Kriging performance model *maxlnagain*(*tr_strength*, *T*, *mlna,* I_{ref}) was constructed using the data obtained from transistor-level simulations in HSPICE®. Latin Hypercube sampling with corner points was used as the initial sampling strategy.

The adaptive sampling method LOLA-Voronoi [5] determined the non-linear regions of the true response and sampled those more densely. 5-fold cross validation with root-relative-square-error (RRSE) was used for the model validation. The definition of RRSE is defined as

$$\mathrm{RRSE} = \sqrt{\frac{\sum_{i=1}^{n}(y_i - \tilde{y}_i)^2}{\sum_{i=1}^{n}(y_i - \tilde{y})^2}} \tag{1}$$

where y_i, $\tilde{y}_i$ and $\tilde{y}$ are the actual, predicted, and mean actual response values.

The constructed model has an RRSE of 4.72%. Fig. 4 shows the plots of the model surfaces used to explore the design space. The results show the effects of the design parameters and the parametric variations. It is seen that both transistor variations and temperature variations can significantly impact performance. It is possible to modulate the design parameters, in order to achieve an optimal gain value under the specific variations.



(a) mlna=0.5 (b)mlna=1.25 (c)mlna=2

Fig. 4. Plot of the model surfaces. (a)—(c) are for different mlna values. The three slices in each plot are for three I_{ref} values. Black is for 50 μA, light grey is for 125μA, and dark grey is for 200μA.

3 Scalable and Variation-Sensitive IO Macromodel

Good macromodels of input/output circuits are essential for fast timing, signal-integrity, and power-integrity analysis in high-speed digital systems. The most popular approach to IO modelling is to use the traditional table-based input-output buffer information specification (IBIS) [9]. IBIS models are simple, portable, IP-protected, and fast in simulation. However, they are unable to simulate continuous PVT variations and unsuitable for statistical analysis. We propose a new type of macromodel, called the surrogate IBIS model, to solve the problem [10]. In the new method, an equivalent circuit structure is used to capture the static and dynamic circuit behaviors, while surrogate modeling is used to approximate each element over a range of Process-Voltage-Temperature (PVT) parameters, so that the macromodel is able to dynamically adapt to the PVT variations in analysis.

3.1 Proposed Macromodel Structure

Fig. 5 shows the proposed macromodel structure that is composed of physically-based equivalent model elements [10]. I_{pu} and I_{pd} represent the nonlinear output current. Time-variant coefficients K_{pu} and K_{pd} determine the partial turn-on of the pull-up/down networks during switching transitions. C_{power} and C_{gnd} represent the nonlinear parasitic capacitance between the output and the supply rails. Surrogate models of these model elements are constructed, to capture the effects of supply voltage, terminal voltages, semiconductor process, and temperature.

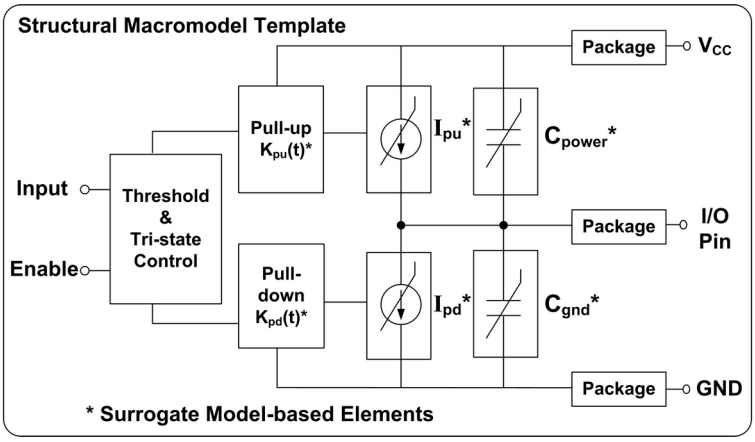


Fig. 5. Structural IO buffer macromodel template with surrogate model elements

3.2 Macromodel Construction

The automatic modeling process described in Section 2 was used to construct surrogate models for the model elements in Fig. 5. The method is demonstrated with the single-ended output buffer circuit shown in Fig. 6. The circuit is designed in 180 nm CMOS process with a 3.3 V normal supply voltage. The threshold voltage variations ΔV_{th} in the MOS transistors are considered as the main process variations and they are assumed to be within ±20% of the nominal value V_{th0}. The parameter $P = \Delta V_{th}/V_{th0}$ is used to describe the threshold voltage variation. The supply voltage Vs is assumed to fluctuate within ±30% of the nominal supply (3.3 V) and temperature (T) is set in the range of 0 to 100°C. In the modeling process, those PVT-related parameters are sampled adaptively in their ranges.

Here modeling data was extracted from transistor-level SPICE circuit simulations. Fig. 7 (a) shows the circuit test-bench to extract the pull-up output current I_{pu} (V_S, V_{pu}, T, ΔV_{th}). The parameter V_{pu} is defined as the voltage difference between the power supply rail and the output, and it ranges from $-V_{CC}$ to $+2V_{CC}$ covering the maximum reflection case [11]. Transient simulations were performed and the simulation time was long enough (in this case it was 1 ms with 1 ns step size) to record a stable output current I_{pu}.

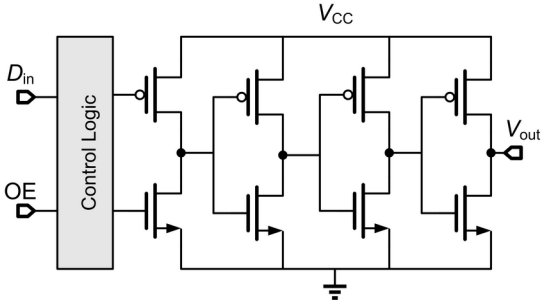
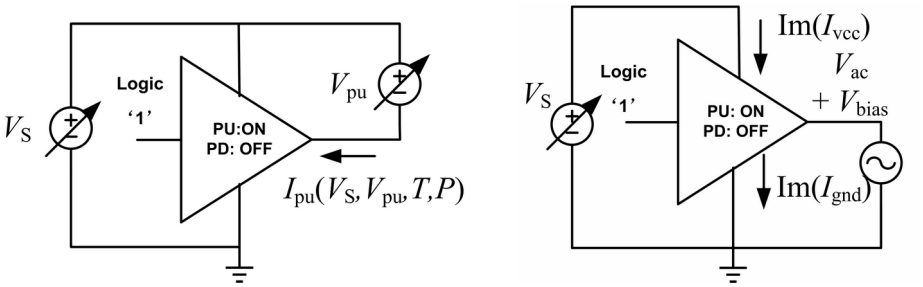


Fig. 6. Simplified schematic of the driver circuit



(a) I_{pu} (b) Capacitance

Fig. 7. Test-benches for extracting model elements: (a) pull-up current I_{pu} (a) output capacitance C_{gnd} and C_{power}

The data was used to fit rational function models in the form:

$$f(X) = \frac{P(X)}{Q(X)} \tag{2}$$

where P and Q are polynomial functions in $X=\{x_1,x_2,\ldots,x_n\}$and Q is non zero. P and Q have no common factor of positive degree.

Similarly, the pull-down current model I_{pd} was extracted by turning on the pull-down network and turning off the pull-up network. I_{pd} was extracted as a model function of PVT variations and V_{pd}, where V_{pd} is defined as the voltage difference between the output and the ground.

The test setup for extracting the output parasitic capacitance is shown in Fig. 7(b). An AC signal is attached to the output ports and the imaginary currents in the power and the ground ports are measured. The capacitances C_{power} and C_{gnd} were derived using

$$C_{power} = \frac{\Im(I_{VCC})}{2\pi f V_{AC}}, \qquad C_{gnd} = \frac{-\Im(I_{gnd})}{2\pi f V_{AC}} \tag{3}$$

where $\Im(I_{VCC})$ and $\Im(I_{gnd})$ are the imaginary parts of the measured currents, f is the frequency of the AC source, and V_{AC} is the AC voltage amplitude. The time-variant transition coefficients K_{pu} and K_{pd} were obtained according to the 2EQ/2UK

algorithm [12]. Fig. 8(a) shows the test to obtain the switching output voltage waveforms. A simplified circuit to illustrate the 2EQ/2UK algorithm is shown in Fig. 8(b). The switching output voltage waveforms wfm_1 and wfm_2 were obtained with different terminal voltage V_{term}, and the unknown coefficients K_{pu} and K_{pd} are derived using the equations

$$\begin{aligned} K_{pu}(t)I_{pu}(V_{wfm_1}(t)) - K_{pd}(t)I_{pd}(V_{wfm_1}(t)) - I_{out} = 0 \\ K_{pu}(t)I_{pu}(V_{wfm_2}(t)) - K_{pd}(t)I_{pd}(V_{wfm_2}(t)) - I_{out} = 0 \end{aligned} \tag{4}$$

where $I_{out} = (V_{out} - V_{term}) / R_{load}$. I_{pu} and I_{pd} are the output current models.

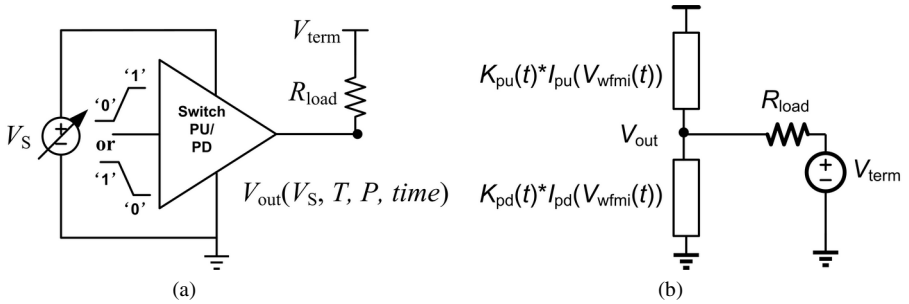


Fig. 8. (a) Test-benches for extracting model elements output capacitance C_{gnd} and C_{power} (b) illustration of 2EQ/2UK algorithm.

To implement the new model, we modified the Verilog-A behavioral version of the IBIS model [13] and applied the surrogate model expressions for the model elements. The surrogate models were implemented in the form of analog functions.

3.3 Test Results

In this section the surrogate IBIS model is compared to the reference provided by the transistor-level simulation, and to the traditional IBIS model extracted from SPICE using the S2IBIS3 v1.0 tool [14].

The test setup is shown in Fig. 9 where the driver is connected to a 0.75-m long lossy transmission line (RLGC model) with a loading resistor. The characteristic impedance of the transmission line is 50 Ω. The loading resistor is 75 Ω. Two test cases were examined. The results are shown in Fig. 10.

1. Case 1, used a 250 MHz square wave as a test input signal. The input data has the pattern "01010" with a 0.1-ns rise/fall time and 2-ns bit-period. The supply voltage varied from 2.8 to 3.8 V.
2. Case 2, used a data pattern with a 1024 bit long pseudorandom bit sequence (PRBS) with 2-ns bit time. The power supply voltage was constant.

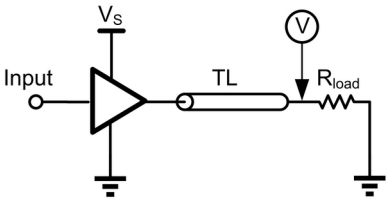
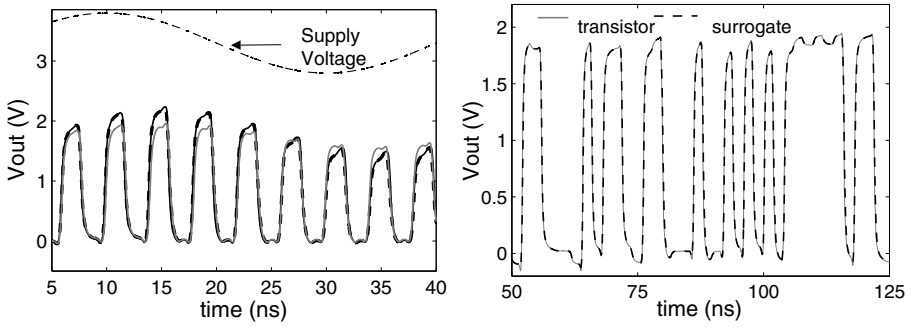


Fig. 9. Test setup for model validation



(a) Case 1 (b) Case 2

Fig. 10. Output voltage at the far end of the transmission line, (a) Case 1, black solid line—transistor-model, grey solid line—traditional IBIS, black dash line—proposed surrogate IBIS. Black dash-dot line—supply voltage. (b) Case 2, grey solid line—transistor, black dashed line—macromodel.

The accuracy of the macromodels is quantified by computing the timing error and the maximum relative voltage error. The timing error is defined as the time difference between the reference and the macromodel voltage responses measured for crossing half of the output voltage swing. The maximum relative voltage error is defined as the maximum error between the reference and macromodel voltage responses divided by the voltage swing.

The results show that in Case 1 when there are large variations of the supply voltage, the surrogate IBIS model has much better accuracy both of the timing error and of the relative voltage error than the traditional IBIS model. The maximum timing error of the surrogate-IBIS model is 79 ps, and the maximum relative voltage error is 6.77%. The surrogate IBIS model achieves the improved accuracy by capturing the complex output capacitance characteristics, the effects of the supply voltage, and gate modulation effects on the output current [15]. In Case 2, the result shows that the surrogate-IBIS achieves good accuracy. In this case, the maximum timing error is 70 ps (3.5% of the bit-time) and the maximum relative voltage error is 6.45%. We also analyze the eye-diagram of the output in Case 2. The eye-width (W) was measured when the eye-height (H) was equal to 1 V. The results under different PVT conditions show that the eye-width differences within 0.04 ns (2% of the bit-time).

In summary, the proposed surrogate-IBIS macromodel achieves good accuracy in the analysis. The macromodels obtained show good accuracy in capturing the effects of reflections and variations, and their scalability makes flexible design analysis possible.

4 Surrogate-Based Device Modeling

Scaling of device sizes induced high variability of transistor parameters. There are two major reasons for this. Firstly, quantum mechanics-based phenomena such as the drain induced barrier lowering (DIBL) or gate tunnelling which are negligible in long-channel devices become more significant. Additional physics-based effects increased the dependence of many circuit design quantities including the drain current, I_{ds}, and device transconductance, g_m, on the transistor process parameters such as the oxide thickness, t_{ox}. Furthermore, the tolerance of semiconductor manufacturing components did not scale down as the transistor sizes shrink [16]. As a consequence, the amount of uncertainty in the design quantities remained constant while device sizes become smaller leading to higher percentages of variability with respect to the nominal values of the transistor process parameters. The experimental data revealed that the traditional process corner analysis might not reflect the real distribution of the critical transistor parameters such as the threshold voltage V_{th} [17] while the Monte Carlo analysis become more computationally intensive with increasing number of variability factors.

The response surface of design quantities which become more complex with the presence of extreme process variations can be accurately captured by surrogate modelling. Surrogate modelling aims to express the output quantity in terms of a few input parameters by evaluating a limited number of samples. These samples are used by the basis functions which establish the response surface of the desired output. Coefficients of the basis functions should be optimized to minimize the modelling error. This approach has been applied to the problem of I_{ds} modelling in order to assess the effects of variability in analogue circuit building blocks, in particular, the differential amplifiers [18]. In this section, the modeling of g_m of n-channel transistors will be discussed.

The transconductance g_m is an important quantity for analog circuits, particularly in determining the AC performance of amplifiers, mixers, and voltage controlled oscillators. The modeling here is based on 65 nm device technology (IBM 10SF design kit) and uses six process parameters (t_{ox}, intrinsic threshold voltage $V_{th,0}$, intrinsic drain-source resistance $R_{ds,0}$, intrinsic mobility μ_0, channel length variation ΔL_{eff}, and channel doping N_{ch}) as input to the model in addition to the terminal voltages of the transistor (gate-source voltage V_{gs}, drain-source voltage V_{ds} , and bulk-source voltage V_{bs}) and the temperature T. The choice of these process parameters is based on their physical origin which ensures a weak correlation between each parameter. BSIM model I_{ds} equations are analytically differentiated to yield g_m [19]:

$$g_m = \partial I_{ds} / \partial V_{gs} . \tag{5}$$

The g_m expression is validated by extensive SPICE circuit simulations over the process corners and at temperature extremes so that it can be used to evaluate the

samples, each a function of the ten parameters described above. Although an analytic equation for g_m is used in this work, the modelling methodology is general and can employ simulations or measurement results given that they have the same input and output parameters.

Kriging basis functions are used to construct the surrogate model with the necessary coefficients being optimized using the MATLAB toolbox Design and Analysis of Computer Experiments (DACE) [20]. The device width is assumed to be 10 µm. The finalized model is tested for accuracy using the root relative square error (RRSE) metric where RRSE can be given by Equation (1).

The g_m model is constructed using a total number of 2560 input samples, and tested with 6400 samples other than the input samples. The resulting model yields an RRSE of 3.96% indicating to a high level of accuracy.

The model can be used to observe the changes in g_m with respect to its input parameters. Examples of this are provided in Figure 8. The graphs provide critical insight to the designer about the fundamental relations and trade-offs between the chosen process parameters, terminal voltages, and temperature. Higher g_m values are obtained with smaller $V_{th,0}$, L_{eff}, and t_{ox}, as well as larger μ_0. This information becomes especially vital when variability of the circuit performance that depends on g_m must be considered. In the example of an RF cascode low-noise amplifier , voltage gain A_v, input and output return ratios, S_{11} and S_{22}, as well as the optimum noise impedance, Z_{opt}, are complex functions of the g_m value of the common source transistor [21]. Any

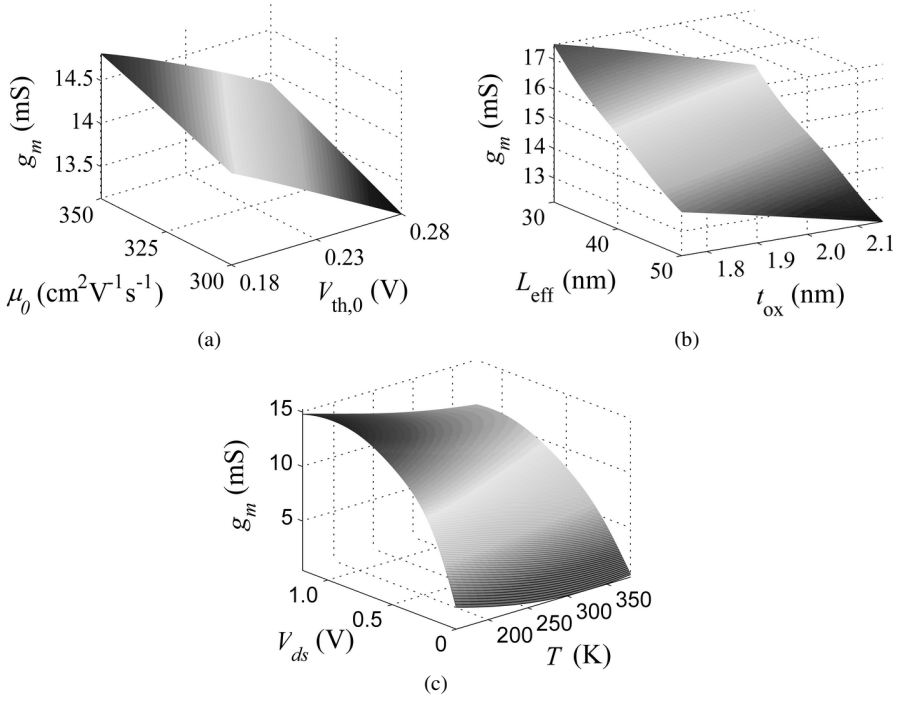


Fig. 11. 3D graphs showing the trade-offs between the different inputs on the modeled g_m

variability of the process parameters of this transistor may push the design outside of the specification range. In this case, information presented in Fig.11 (a)—(c) can be used to change the matching network of the amplifier such that it can yield the desired design metrics in all cases of process variability.

Finally, it should be noted that surrogate model-based device modeling is not limited to one single design quantity. Response surface models of other important design metrics can also be developed by using the methodology described here. As an example, consider the bandwidth of a single-stage amplifier. The bandwidth is both a function of process parameters used in g_m modeling and a function of the junction capacitances of the transistor. However, these junction capacitances depend also on some process parameters. The exact relationships can be quantified by analytical expressions as given in the device model equations [19]. Once the additionally required parameters are determined, then the surrogate modeling process can be applied as in g_m modeling.

5 Surrogate Model-Based Circuit Design

5.1 Yield-Aware Circuit Optimization

As IC technologies scale down to 65 nm and beyond, it is more challenging to create reliable and robust designs in the presence of large process (P) and environmental variations (e.g. supply voltage (V), temperature (T)) [22]. Without considering PVT fluctuations, the optimal circuit design would possibly minimize the cost functions by pushing many performance constraints to their boundaries, and result in a design that is very sensitive to process variations. Therefore, we need to not only search for the optimal case at the nominal conditions, but also carefully consider the circuit robustness in the presence of variations. However, the fulfillment of all these requirements introduces more complications in circuit design.

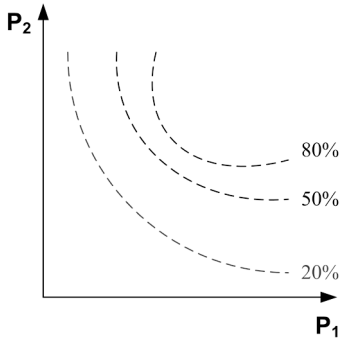


Fig. 12. Illustration of Pareto fronts with different yield levels

Yield is defined as the number of dies per wafer that meet all predefined performance metrics. Monte Carlo analysis of a circuit is an important technique used for yield estimation. However, this method requires a large number of sampling points to achieve sufficient accuracy and therefore it is very time-consuming. One solution to

reduce computational cost is to use the performance surrogate models proposed in Section 2. As performance models are constructed as a function of selected design parameters and parametric variations, they can be used instead of using circuit-level simulations. Therefore, yield estimation can be achieved without large computational cost.

One application of a variation-aware performance model is to obtain the yield-aware Pareto fronts [23] which is best trade-offs of the overall circuit performance and yield. In this application, in addition to searching for the general Pareto-optimal designs, performance yield at those design points is evaluated by using the variation-aware performance model. As a result, the yield-aware Pareto fronts can be generated. An illustration is shown in Fig. 12. P_1 and P_2 are the performance parameters to trade-off, and the curves are the Pareto fronts with different yield levels. The yield-aware Pareto fronts of sub-blocks could be further used in yield-aware system design.

5.2 Surrogate-Based Circuit Optimization

Simulation-based circuit optimization is a very good application of surrogate modeling, as the process requires a great number of iterative evaluations of objective functions. In an optimization process, surrogate models are used to guide the search instead of achieving the global accuracy.

In the surrogate-based optimization process, generally there are two types of simulation models, a low-fidelity and a high-fidelity model. In our circuit design problems, the transistor-level circuit simulation is used as a high-fidelity model while the built surrogate model is used as the low-fidelity model. The general surrogate-based optimization process is shown in Fig. 13 [24].

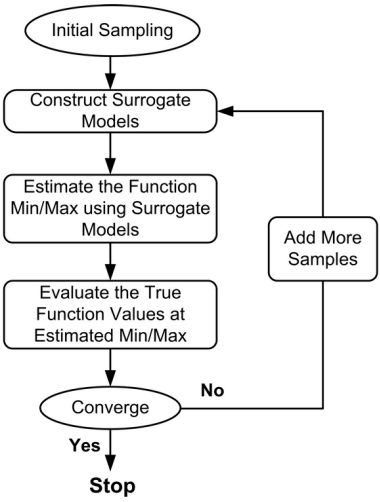


Fig. 13. General surrogate-based optimization flow

The Gaussian-based Kriging model can be used as an approximation method since this model is able to provide estimation of the uncertainty in the prediction. Adaptive sampling methods (e.g. [3]) can be used to balance exploration (improving the general accuracy of the surrogate model) and exploitation (improving the accuracy of the surrogate model in the local optimum area) during optimization. An alternative method, space mapping [25], maps the input/output space of a low-fidelity model to the input/output space of the high-fidelity model. These methods can significantly improve the optimization efficiency when physically-based and computational efficient low-fidelity models are available.

6 Summary

This work presents the applications of surrogate modeling in variation-aware circuit macromodeling and design analysis. Surrogate modeling can facilitate the design exploration and optimization with variation-aware performance models. Also, surrogate modeling can be used to enhance the accuracy and scalability of IO macromodels. Moreover, the surrogate model-based method is able to generate device models with critical variability parameters. The surrogate-based method greatly reduces the complexities and costs of variation-aware macromodeling and circuit design.

Acknowledgements. This material is based up on the work supported by the Self-HEALing mixed signal Integrated Circuits (HEALICs) program of the Department of Defense Advanced Research Projects Agency (DARPA) and AFRL under contract number: FA8650-09-C-7925. Approved for Public Release. Distribution Unlimited. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government. The authors T. Zhu, Dr. P. D. Franzon, and Dr. M. B. Steer would like to thank Dr. T. Dhaene of Ghent University, Belgium, for providing the SUrrogate MOdeling (SUMO) Toolbox and for helpful discussion.

References

1. Gorissen, D., Turck, F.D., Dhaene, T.: Evolutionary Model Type Selection for Global Surrogate Modeling. Journal of Machine Learning Research 10(1), 2039–2078 (2009)
2. Eldred, M.S., Dunlavy, D.M.: Formulations for Surrogate-based Optimization with Data Fit, Multifidelity, and Reduced-order models. In: 11th AIAA/ISSMO Multidisciplinary Analysis and Optimization Conference, AIAA-2006-7117, Protsmouth, Virginia (2006)
3. Forrester, A., Sobester, A., Keane, A.: Engineering Design via Surrogate Moldeling: A Practical Guide. John Wiley & Sons (2008)
4. Kleijnen, J.: Design and Analysis of Simulation Experiments. Springer (2008)
5. Crombecq, K., Couckuyt, I., Gorissen, D., Dhaene, T.: Space-Filling Sequential Design Strategies for Adaptive Surrogate Modelling. In: 1st International Conference on Soft Computing Technology in Civil, Structural and Environmental Engineering, Paper 50, Civil-Comp Press, Stirlingshire (2009)
6. Meckesheimer, M., Booker, A.J., Barton, R., Simpson, T.: Computationally Inexpensive Metamodel Assessment Strategies. AIAA Journal 40(10), 2053–2060 (2002)

7. Gorissen, D., Crombecq, K., Couckuyt, I., Dhaene, T., Demeester, P.: A Surrogate Modeling and Adaptive Sampling Toolbox for Computer Based Design. Journal of Machine Learning Research 11, 2051–2055 (2010)
8. Jeon, S., Wang, Y., Wang, H., Bohn, F., Natarajan, A., Babakhani, A., Hajimiri, A.: A Scalable 6-to-18 GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS. IEEE Journal of Solid-State Circuits 43(12), 2660–2673 (2008)
9. IO Buffer Information Specification, http://www.eigroup.org/ibis/ibis.htm
10. Zhu, T., Steer, M.B., Franzon, P.D.: Accurate and Scalable IO Buffer Macromodel Based on Surrogate Modeling. IEEE Transactions on Components, Packaging and Manufacturing Technology 1(8), 1240–1249 (2011)
11. IBIS Modeling Cookbook, http://www.vhdl.org/pub/ibis/cookbook/cookbook-v4.pdf.
12. Muranyi, A.: Accuracy of IBIS models with reactive loads, http://www.eda.org/pub/ibis/summits/feb06/muranyi2.pdf
13. LaBonte, M., Muranyi, A.: IBIS Advanced Technology Modeling Task Group Work-achievement: Verilog-A element library HSPICE test, http://www.vhdl.org/pub/ibis/macromodel_wip/archive-date.html
14. Varma, A., Glaser, A., Lipa, S., Steer, M.B., Franzon, P.D.: The Development of A Macro-modeling Tool to Develop IBIS Models. In: 12th Tropical Meeting on Electrical Performance Electronic Packaging, pp. 277–280. Princeton, New Jersey (2003)
15. Varma, A.K., Steer, M.B., Franzon, P.D.: Improving Behavioral IO buffer modeling based on IBIS. IEEE Transactions on Advanced Packaging 31(4), 711–721 (2008)
16. Orshansky, M., Nassif, S.R., Boning, D.: Design for Manufacturability and Statistical Design: A Constructive Approach. Springer, New York (2008)
17. Saha, S.K.: Modeling process variability in scaled CMOS technology. IEEE Design and Test of Computers 27(2), 8–16 (2010)
18. Yelten, M.B., Franzon, P.D., Steer, M.B.: Surrogate Model-based Analysis of Analog Circuits—Part I: Variability Analysis. IEEE Transactions on Device and Material Reliability 11(3), 458–465 (2011)
19. Morshed, T.H., Yang, W., Dunga, M.V., Xi, X., He, J., Liu, W., Yu, K., Cao, M., Jin, X., Ou, J.J., Chan, M., Niknejad, A.M., Hu, C.: BSIM4.6.4 MOSFET model- User's manual (April 2009), http://www-device.eecs.berkeley.edu/~bsim3/BSIM4/BSIM470/BSIM470_Manual.pdf
20. Lophaven, S.N., Nielsen, H.B., Sondergaard, J.: A MATLAB Kriging toolbox 2.0 (August 2002), http://www2.imm.dtu.dk/?hbn/dace/dace.pdf
21. Yelten, M.B., Gard, K.G.: A Novel Design Methodology for Tunable of Low Noise Amplifiers. In: Wireless and Microwave Conference (WAMICON 2009), Florida, USA, pp. 1–5 (2009)
22. Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS)
23. Tiwary, S.K., Tiwary, P.K., Rutenbar, R.A.: Generation of Yield-aware Pareto Surfaces for Hierarchical Circuit Design Space Exploration. In: 43rd ACM/IEEE Design Automation Conference, San Francisco, CA, U.S.A. (2006)
24. Queipo, N.V., Haftka, R.T., Shyy, W., Goel, T., Vaidyanathan, R., Tucker, P.K.: Surrogate-based Analysis and Optimization. Progress in Aerospace Sciences 41, 1–28 (2005)
25. Koziel, S., Cheng, Q.S., Bandler, J.W.: Space mapping. IEEE Microwave Magazine 9(6), 105–122 (2008)