# Chapter 5
# Piezotronic Logic Circuits and Operations

**Abstract** In this chapter, by utilizing the gating effect produced by the piezopotential in a nanowire under externally applied deformation, piezotronic transistors have been fabricated; one can use them for the universal logic operations such as NAND, NOR and XOR gates as has been demonstrated for performing piezotronic logic operations. The mechanical–electronic logic units are an important step toward the basic design of complex systems in human–CMOS interfacing, touch pad technology and active flexible, nanorobotics, active flexible electronics, microfluidics and MEMS.

A self-powered [1] autonomous intelligent nanoscale system should consist of ultrasensitive nanowire (NW)-based sensors [2–5], integrated high-performance memory and logic computing components for data storage and processing as well as decision making [6–12], and an energy scavenging unit for sustainable, self-sufficient and independent operation [1, 13–20]. The existing semiconductor NW logic devices are based on electrically gated field-effect transistors, which function as both the drivers and the active loads of the logic units by adjusting the conducting channel width [21, 22]. Moreover, the currently existing logic units are "static" and are almost completely triggered or agitated by electric signals, while the "dynamic" movable mechanical actuation is carried out by another unit possibly made of different materials.

In this chapter, we present the piezoelectric trigged mechanical–electronic logic operation using the piezotronic effect, through which the integrated mechanical electrical coupled and controlled logic computation is achieved using only ZnO NWs [23]. By utilizing the piezoelectric potential created in a ZnO NW under externally applied deformation, strain-gated transistors (SGTs) have been fabricated, using which universal logic components such as inverters, NAND, NOR, XOR gates have been demonstrated for performing piezotronic logic calculations, which have the potential to be integrated with the NEMS technology for achieving advanced and complex functional actions in applications of vital importance in portable electronics, medical sciences and defense technology, such as in nanorobotics for sensing and actuating, in microfluidics [24] for controlling the circuitry of the fluid flow, and in other micro/nanosystems for intelligent control and action.

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## 5.1 Strain-Gated Transistor

The piezopotential created inside a ZnO NW under strain can be effectively used as a gate voltage, which has been applied for fabricating a range of piezotronic nanodevices [25–28], and, therefore, the mechanic-electrical coupled and controlled actions can be performed in one structure unit made of a single material. Mechanical straining can create a piezopotential inside ZnO due to the polarization of the non-mobile ions, owing to the piezoelectric effect. In addition, the piezopotential can act as a "controller" for gating the transport behavior of the charge carriers, which is the fundamental principle for strain-gated electronic devices, based on which the ZnO-NW electromechanical switch has been fabricated [28].

### *5.1.1 Device Fabrication*

A strain-gated transistor (SGT) is made of a single ZnO NW with its two ends, which are the source and drain electrodes, being fixed by metal contact on a polymer substrate (Fig. 5.1(a)). The SGI was fabricated by bonding two ZnO NWs laterally on a Dura–Lar film. The thickness of the Dura–Lar film is 0.5 mm. The ZnO NWs were synthesized via a physical vapor deposition method and typically have diameters of 300 nm and lengths of 400 μm (Fig. 5.1(a)). The films were first cleaned with acetone, isopropyl alcohol and DI water by sonication, after which the Dura–Lar films were dried by nitrogen gas blowing. One ZnO NW was placed flat on the top surface of the Dura–Lar film first using a probe station (Cascade Microtech, Inc.) under an optical microscope (Leica Microsystems, Inc.). Silver paint (Ted Pella, Inc.) was applied at both ends of the ZnO NW for electrical contacts. The second ZnO NW was placed on the bottom surface of the Dura–Lar film in the same way.

Once the substrate is bent, a tensile/compressive strain is created in the NW since the mechanical behavior of the entire structure is determined by the substrate. Utilizing the piezopotential created inside the NW, the gate input for a NW SGT is an externally applied strain rather than an electrical signal. $I_{DS}$–$V_{DS}$ characteristic for each single ZnO-NW SGT is obtained as a function of the strain created in the SGT (Fig. 5.1(a)) before further assembly into logic devices. A NW SGT is defined as forward biased if the applied bias is connected to the drain electrode (Fig. 5.1(a)).

For a SGT, the external mechanical perturbation induced strain ($\varepsilon_g$) acts as the gate input for controlling the "on"/"off" state of the NW SGT. The positive/negative strain is created when the NW is stretched/compressed (see SI for the calculation of the strain in the NW SGT). The $I_{DS}$–$\varepsilon_g$ curves at a fixed $V_{DS}$ show that $I_{DS}$ increases as the gate strain $\varepsilon_g$ increases and the threshold gate strain $\varepsilon_T$ is around 0.08 % (Fig. 5.1(b)), which show that the SGT behaves in a similar way to a $n$-channel enhancement-mode MOSFET. The threshold gate strain $\varepsilon_T$ is determined from the intercept (on the $\varepsilon_g$ axis) of the tangent of the maximum slope region (shown as the black dashed line in Fig. 5.1(b)) of the $I_{DS}$–$\varepsilon_g$ curve. The $I_{DS}$–$\varepsilon_g$ transfer curve obtained for drain bias voltage $V_{DS} = 1$ V (Fig. 5.2) demonstrates that

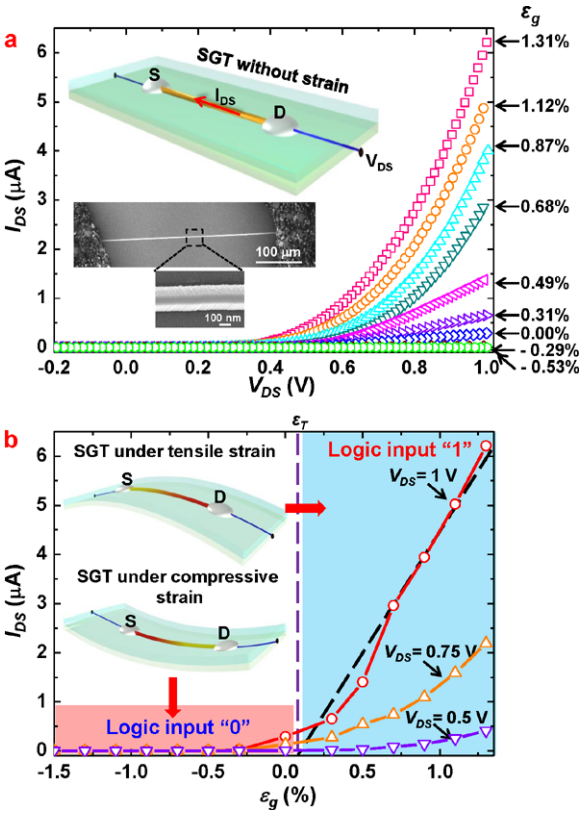


**Fig. 5.1** Single ZnO NW strain-gated transistor (SGT). (**a**) $I_{DS}$–$V_{DS}$ output characteristic for a ZnO SGT device with strain sweeping from $\varepsilon_g = -0.53$ % to 1.31 % at a step of 0.2 %. (*Insets*) *Top*: schematic of a single ZnO NW SGT under bias without strain. Current flows from drain to source electrode with external bias applied at the drain side. *Bottom*: top-view SEM image of the active part of a ZnO SGT ($L = 70$ μm, diameter = 300 nm), with both ends of the ZnO NW fixed by silver paste. (**b**) $I_{DS}$–$\varepsilon_g$ transfer characteristic for the same ZnO SGT device under three different $V_{DS}$ bias values: 1, 0.75 and 0.5 V, respectively. The threshold gate strain $\varepsilon_T$ is determined as around 0.08 % from the intercept (on the $\varepsilon_g$ axis) of the tangent of the maximum slope region (shown as the *black dashed line*) of the $I_{DS}$–$\varepsilon_g$ curve. (*Insets*) *Top*, schematic of a ZnO SGT under tensile strain and the corresponding $I_{DS}$–$\varepsilon_g$ characteristic curve (*blueish region*), which is the logic "1" strain input region for the SGT. *Bottom*, schematic of a ZnO SGT under compressive strain and the corresponding $I_{DS} - \varepsilon_g$ characteristic curve (*red region*), which is the logic "0" strain input region of the SGT. As in the NW, the piezopotential created by strain is negative in the red color region and positive in the yellow color region [23]

the NW SGT has a peak pseudo transconductance, $g_m = dI_{DS}(V_{DS})/d\varepsilon_g$, which is 6 μA for a strain change of $\Delta\varepsilon_g = 1$ %. The on and off currents $I_{on}$ and $I_{off}$ for the NW SGT can be determined as the values obtained at $\varepsilon_{g(on)} = \varepsilon_g - 0.3$ % and $\varepsilon_{g(off)} = \varepsilon_g + 0.7$ %, so that 70 % of the $\varepsilon_g$ swing above the threshold strain $\varepsilon_g$ turns the ZnO NW SGT on, while the remaining 30 % defines the "off" operation range,

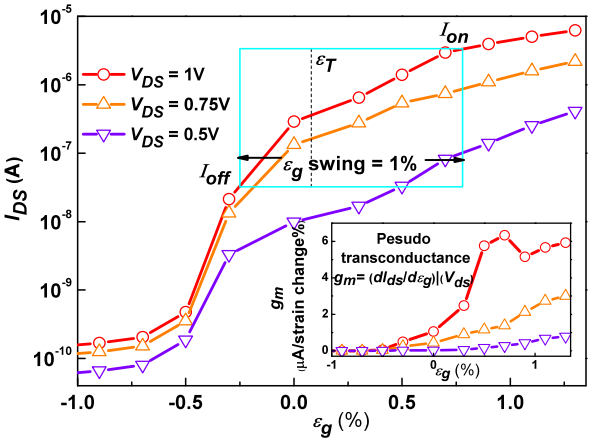


**Fig. 5.2** $I_{DS}$–$\varepsilon_g$ transfer characteristic for ZnO NW SGT. $I_{DS}$–$\varepsilon_g$ transfer characteristic for the ZnO SGT device under three different $V_{DS}$ bias values: 1, 0.75 and 0.5 V, respectively. The *blue square* defines the 1 % gate strain window. On and off currents are defined as the values obtained at $\varepsilon_{g(on)} = \varepsilon_g - 0.3$ % and $\varepsilon_{g(off)} = \varepsilon_g + 0.7$ %, so that 70 % of the $\varepsilon_g$ swing above the threshold strain $\varepsilon_g$ turns the ZnO NW SGT on, while the remaining 30 % defines the "off" operation range. (*Inset*) Pseudo transconductance for this ZnO NW SGT with $V_{DS}$ bias values of 1, 0.75 and 0.5 V, respectively, from top to bottom [23]

which is demonstrated in Fig. 5.3. $I_{on} = 3.38$ μA and $I_{off} = 0.03$ μA are hence obtained with $I_{on}/I_{off}$ ratio of 112 for $V_{DS} = 1$ V; this ratio is comparable to the reported value for the Ge/Si NW-based device that was electrically driven [22]. It can also be foreseen from the $I_{DS}$–$\varepsilon g$ transfer curves (Fig. 5.3) that the ZnO-NW SGT-based electromechanical amplifier can be realized by integrating with nanoscale electromechanical transducing units [6].

### 5.1.2 Fundamental Principle

The working principle of a SGT is illustrated by the band structure of the device. A strain–free ZnO NW has Schottky contacts at the two ends with the source and drain electrodes but with different barrier heights of $\Phi_S$ and $\Phi_D$, respectively (Fig. 5.3(a)). The Fermi level inside the ZnO NW is considered flat here for illustration purpose, which is valid in our devices since the most of the bias falls at the reversed biased junction [28]. When the drain is forward biased, the quasi-Fermi levels at the source ($E_{F,S}$) and drain ($E_{F,D}$) are different by the value of $eV_{bias}$, where $V_{bias}$ is the applied bias (Fig. 5.3(b)). An externally applied mechanical strain ($\varepsilon_g$) results in both the band structure change and piezoelectric potential field inside a ZnO NW [28]. The change in band structure leads to the piezoresistance effect, which is a non-polar and symmetric effect at both the source and drain contacts. Since ZnO is a polar structure along $c$-axis, straining in axial direction ($c$-axis) creates a polarization of cations and anions in the NW growth direction, resulting in

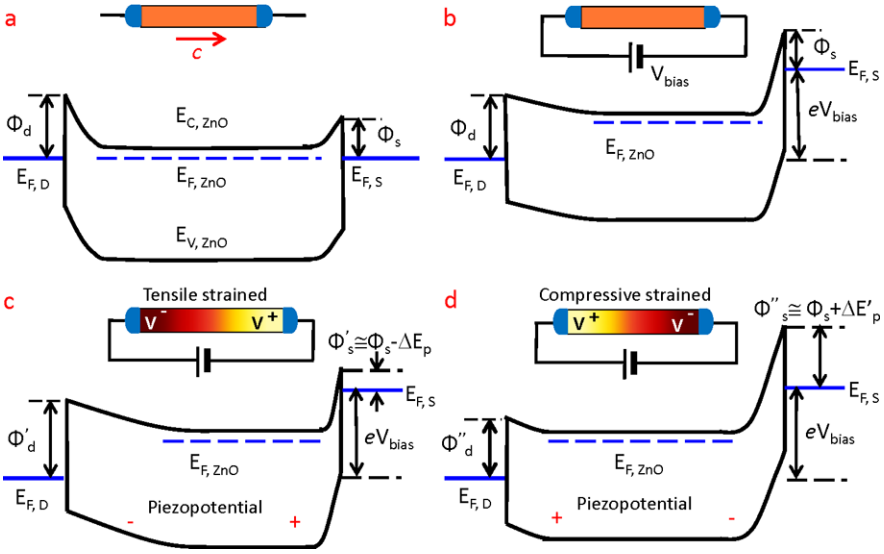


**Fig. 5.3** The band structures of the ZnO NW SGT under different conditions for illustrating the mechanism of the strain-gated transistor (SGT). The crystallographic $c$-axis of the nanowire directs from drain to source. (**a**) The band structure of a strain–free ZnO NW SGT at equilibrium with different barrier heights of $\Phi_S$ and $\Phi_D$ at the source and drain electrodes, respectively. (**b**) The quasi-Fermi levels at the source ($E_{F,S}$) and drain ($E_{F,D}$) of the ZnO SGT are split by the applied bias voltage $V_{\text{bias}}$. (**c**) With tensile strain applied, the SBH at the source side is reduced from $\Phi_S$ to $\Phi'_S \cong \Phi_S - \Delta E_P$. (**d**) With compressive strain applied, the SBH at the source side is raised from $\Phi_S$ to $\Phi''_S \cong \Phi_S + \Delta E'_P$ [23]

a piezopotential drop from $V^+$ to $V^-$ inside the NW (Fig. 5.3), which produces an asymmetric effect on the changes in the Schottky barrier heights (SBHs) at the drain and source electrodes. Under tensile strain, the SBH at the source side reduces from $\Phi_S$ to $\Phi'_S \cong \Phi_S - \Delta E_P$ (Fig. 5.3(c)), where $\Delta E_P$ denotes the change from the locally created piezopotential, and it is a function of the applied strain, resulting in increased $I_{\text{DS}}$. For the compressively strained SGT, the sign of the piezopotential is reversed, and thus the SBH at the source side is raised from $\Phi_S$ to $\Phi''_S \cong \Phi_S + \Delta E'_P$ (Fig. 5.3(d)), where $\Delta E'_P$ denotes the piezopotential effect on the SBH at source side, resulting in a large decrease in $I_{\text{DS}}$. Therefore, as the strain $\varepsilon_g$ is swept from compressive to tensile regions, the $I_{\text{DS}}$ current can be effectively turned from "off" to "on" while $V_{\text{DS}}$ remains constant. This is the fundamental operating principle of the SGT.

## 5.2 Strain-Gated Invertor

The piezotronic strain-gated complementary logic gates are built using back-to-back packaged $n$-type ZnO NW SGTs on the top and bottom surfaces of a flexible substrate. Our first example is to illustrate the ZnO-NW strain-gated inverter (SGI)

(Fig. 5.4). When the substrate is bent downward (Fig. 5.4(a1)), a tensile strain of 0.05–1.5 % is created in SGT 1, while a compressive strain with the same magnitude is simultaneously produced in SGT 2, which results in a complementary "on" and "off" status in the two SGTs, respectively. Alternatively, if the substrate is bent upward (Figs. 5.4(a3)), the two SGTs have a complementary "off" and "on" status, respectively. Therefore, these two SGTs behave in a similar way to the operation of the NMOS and PMOS transistors in the conventional complementary-metal-oxide-semiconductor (CMOS) inverters [29].

The strain–voltage transfer characteristic (SVTC) and noise margins of the NW SGI are obtained by plotting the measured output voltages versus corresponding gate strains (Fig. 5.4(b)). $V_{OH}$ and $V_{OL}$ represent the high and low output voltages of the SGI, with ideal values of $V_{OH} = V_{DS} = 1$ V and $V_{OL} = 0$ V. The experimental values for $V_{OH}$ and $V_{OL}$ are 0.98 V and 0.0001 V, respectively. The measured value for $V_{OH}$, smaller than the applied 1 V, is due to the voltage drop across the SGT that is at "on" status. The logic swing of the SGI defined by $(V_{OH} - V_{OL})$ is 0.98 V. The switching threshold strain of the SGI, $\varepsilon_I$, at which the output of the SGI switches between logic high and low status, is obtained at point C with a strain value of $-0.6$ % in Fig. 5.4(b). The slope value of the dashed line connecting the point of the origin and point C in Fig. 5.4(b) is 1. In order to characterize the effect of the input gate strain on the SGI output, the largest input strain for generating output logic "1", $\varepsilon_{IL}$, and the smallest input strain for inducing output logic "0", $\varepsilon_{IH}$, are determined at the pseudo unit gain points A and B (see Fig. 5.4(b) and SI) with strain values of $-0.8$ % and $-0.38$ %, respectively. The slopes of the SVTC curve (red line) at points A and B are both $-1$. The input strain zone with $\varepsilon < \varepsilon_{IL}$ $(= -0.8$ %) (purple color zone in Fig. 5.4(b)) induces the logic output of "1" for the SGI, while input strain zone with $\varepsilon > \varepsilon_{IH}$ $(= -0.38$ %) (the bluish color zone in Fig. 5.4(b)) induces logic output "0" for the SGI. The negative values for $\varepsilon_{IL}$ and $\varepsilon_{IH}$ may be due to the fact that some initial strains were unpurposeful introduced in the SGTs during the fabrication process [30]. In the logic low input region (purple color region in Fig. 5.4(b)), SGT 1 is on and SGT 2 is off; while in the logic high input region (bluish color region in Fig. 5.4(b)), SGT 1 is off and SGT 2 is on. The response time of the SGI is dictated by the straining rate, which is an application-dependent factor and the transient property can be investigated for ZnO NW SGI. The strain-gated logic devices are designed to interface with the ambient environment, which is associated with low-frequency mechanical actions, and the aim and targeting applications are different from those of conventional silicon devices which aim at speed. Switching frequency is not the critical issue as long as the strain-gated logic devices can respond to and process the mechanical signals in a timely manner, such as in applications of nanorobotics, transducers and micro-machine. The applications of SGTs are complementary to those of the CMOS technology. Unlike the conventional CMOS inverter, there is no electrical gate in the ZnO-NW SGT and hence the gate leakage current can be ignored in the ZnO-NW SGI.

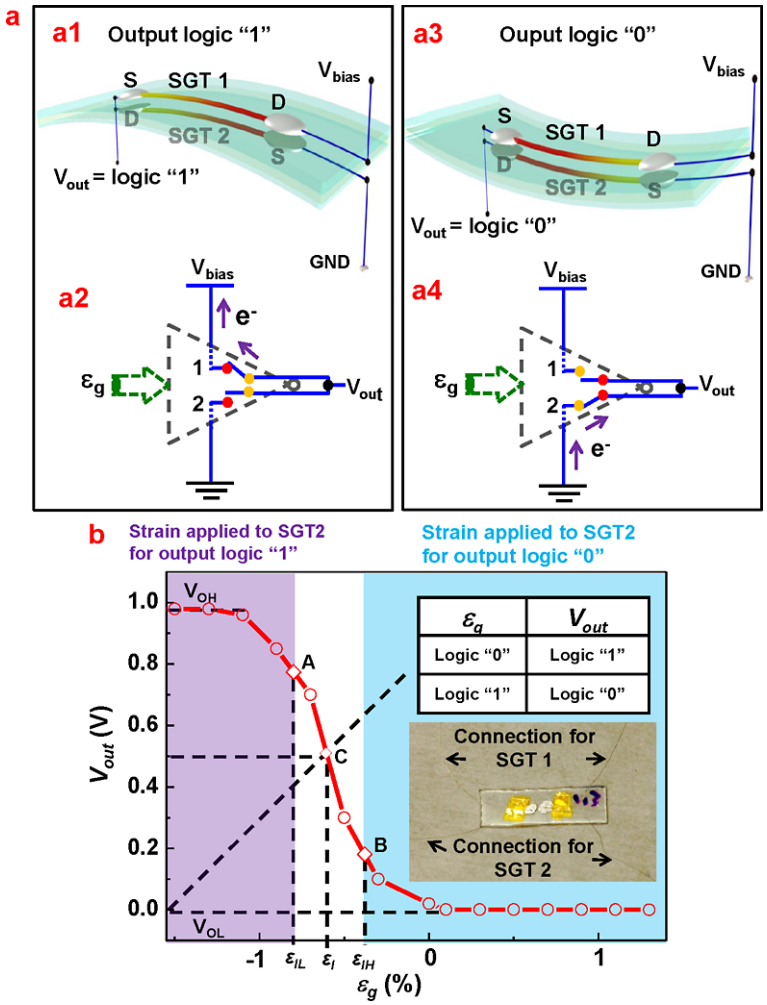


**Fig. 5.4** ZnO NW strain-gated inverter (SGI). (**a1**)–(**a4**) Schematics and corresponding symbols of a ZnO NW SGI performing logic operations in responding input strain. The strain input for the SGI is defined in reference to the strain acting to SGT 2. When the strain input for the SGI is logic "0", SGT 1 is on and SGT 2 is off. Therefore the electrical output is logic "1" for the SGI. GND is the grounded end. When the strain input for the SGI is logic "1", SGT 1 is off and SGT 2 is on. Therefore the electrical output is logic "0" for the ZnO SGI. The *c*-axis direction and the polarity of the piezopotential field for each SGT under strains are defined in Fig. 5.1. (**b**) The strain–voltage transfer characteristic (SVTC) and noise margins of the ZnO NW SGI with $V_{DS} = 1$ V. The slope of the dashed line connecting the point of the origin and point C is 1. The slopes of points A and B on the SVTC curve (*red line*) are both $-1$. *Inset*, optical picture of a ZnO NW SGI, with two SGTs and four connecting wires [23]

**Table 5.1** Two kinds of transition occur during the switching of a ZnO NW strain-gated NAND gate. One kind of transition changes the on/off status for all four SGTs, such as the case happening in the first two columns of the table (with purple color). The other kind of transition changes the on/off status for only two SGTs, like the cases happening in the last four columns of the table (with bluish color). The two numbers in the quotation marks represent the logic levels for strain input on the SGIs in a ZnO NW strain-gated NAND gate

| | "0 0" ⇄ "1 1" | | "0 1" → "1 1" | | "1 0" → "1 1" | |
|---|---|---|---|---|---|---|
| SGT 1 | On | Off | On | Off | Off | Off |
| SGT 2 | Off | On | Off | On | On | On |
| SGT 3 | Off | On | On | On | Off | On |
| SGT 4 | On | Off | Off | Off | On | Off |

**Table 5.2** Two kinds of transition occur during the switching of a ZnO NW strain-gated NOR gate. One kind of transition changes the on/off status for all four SGTs, such as the case happening in the first two columns of the table (with purple color). The other kind of transition changes the on/off status for only two SGTs, like the cases happening in the last four columns of the table (with blueish color). The two numbers in the quotation marks represent the logic levels for strain input on the SGIs in a ZnO NW strain-gated NOR gate

| | "0 0" ⇄ "1 1" | | "0 0" → "1 0" | | "0 0" → "0 1" | |
|---|---|---|---|---|---|---|
| SGT 5 | Off | On | Off | On | Off | Off |
| SGT 6 | On | Off | On | Off | On | On |
| SGT 7 | On | Off | On | On | On | Off |
| SGT 8 | Off | On | Off | Off | Off | On |

## 5.3 Piezotronic Logic Operations

### *5.3.1 NAND and NOR*

Logic operations of NW strain-gated NAND and NOR gates were realized by integrating two NW SGIs, which are gated individually by the applied strains, according to corresponding connection rules (Figs. 5.5A(a1) and (a2) for the NAND gate and Figs. 5.5A(b1) and (b2) for the NOR gate). The output voltages of NAND and NOR gates versus the input gate strains are shown in Fig. 5.5A(a3) for the NAND gate and Fig. 5.5A(b3) for the NOR gate. Two types of transition occur during the switching operation of both the ZnO NW strain-gated NAND and NOR gates, which have been tabulated (Tables 5.1 and 5.2). It can also be seen that NW strain-gated NAND

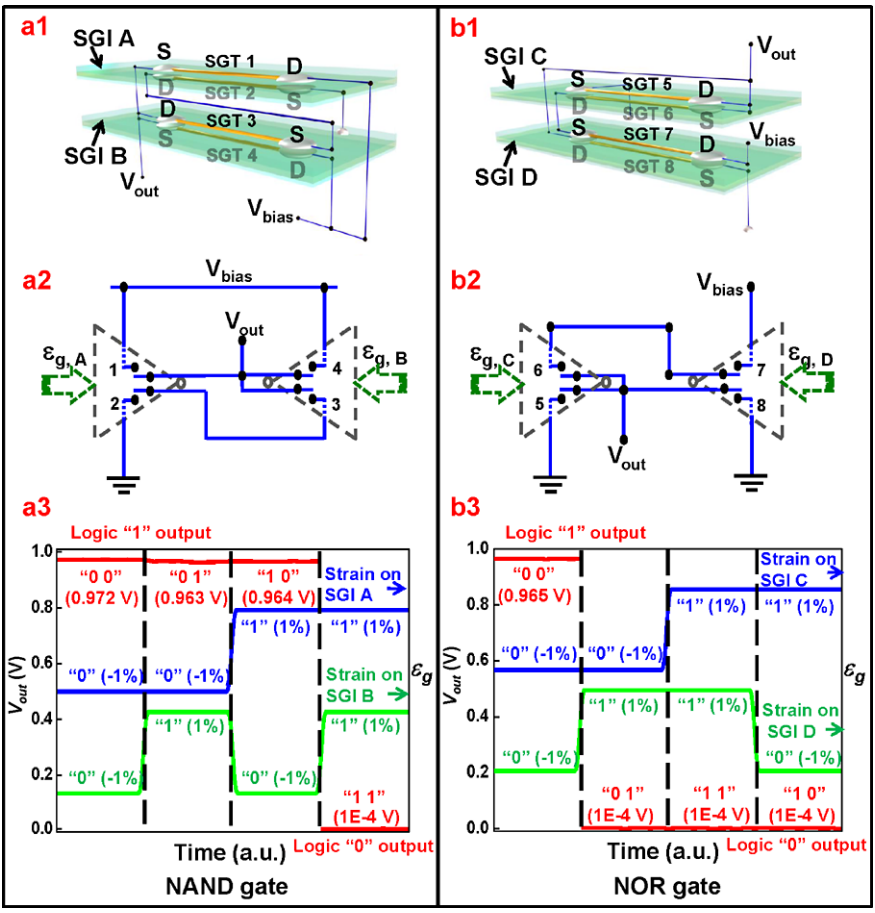


**Fig. 5.5A** (**a**), (**b**). ZnO NW strain-gated NAND and NOR logic gates. (**a1**)–(**a3**) ZnO NW strain–gated NAND gate. (**a1**) Schematic of the ZnO NW strain-gated NAND logic gate, which is composed of two SGIs, SGI A, and SGI B. The strain input A for SGI A is defined in reference to the strain applied to SGT 2 and the strain input B for SGI B is defined in reference to the strain applied to SGT 3. (**a2**) Layout for ZnO NW strain-gated NAND logic gate by connecting two ZnO NW SGIs. (**a3**) Logic operations and experimental truth table of the ZnO NW strain-gated NAND logic gate. The red line is the electrical output of the NAND gate. *Blue* and *green lines* represent the strain input applied on SGI A and SGI B, respectively. "1" and "0" in the quotation marks along the input curves represent the logic levels of the input. For the output, the first number in the quotation marks represents the logic level for strain input on SGI A and the second number represents the logic level for strain input on SGI B. The values in the parentheses are the corresponding physical values for the input and output. The same denominations apply for NOR and XOR logic gates. (**b1**)–(**b3**) ZnO NW strain-gated NOR gate. (**b1**) Schematic of the ZnO NW strain-gated NOR logic gate, which is composed of two SGIs, SGI C and SGI D. The strain input C for SGI C is defined in reference to the strain applied to SGT 5 and the strain input D for SGI D is defined in reference to the strain applied to SGT 8. (**b2**) Layout for ZnO NW strain-gated NOR logic gate connecting two ZnO NW SGIs. (**b3**) Logic operations and experimental truth table of the ZnO NW strain-gated NOR logic gate. The *red line* is the electrical output of the NOR gate. *Blue* and *green lines* represent the strain input applied on SGI C and SGI D, respectively. The abbreviation a.u. is for arbitrary units

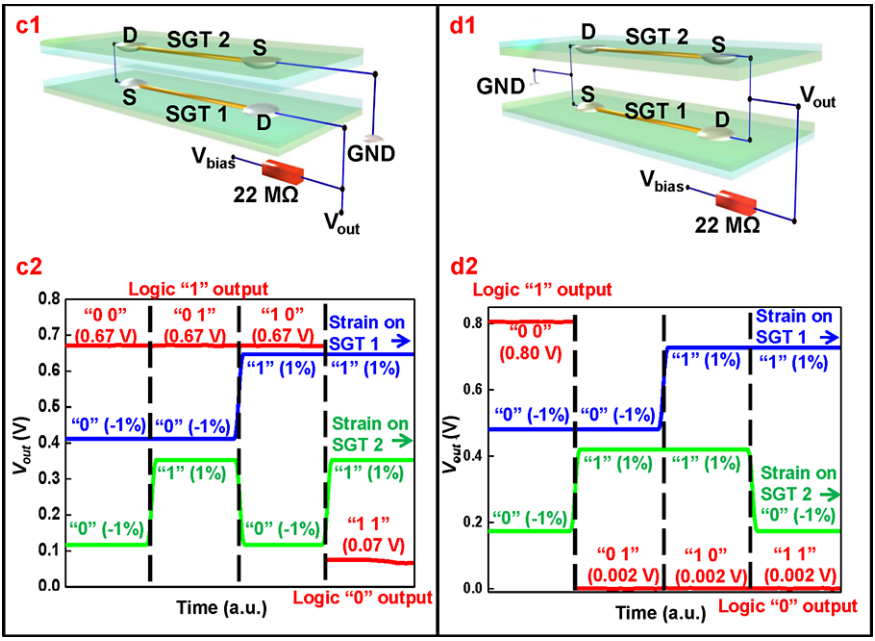


**Fig. 5.5B** (**c**), (**d**). (**c1**) Schematic of a resistive-load ZnO NW NAND gate constructed from serial connection of two ZnO NWs. A 22 M$\Omega$ resistor is used as the pull-up load. (**c2**) Logic operations and experimental truth table of the resistive-load ZnO NW NAND logic gate. *Blue curve* and *green curve* represent the strain input applied on SGT 1 and SGT 2, respectively. (**d1**) Schematic of a resistive-load ZnO NW NOR gate constructed from parallel connection of two ZnO NWs. A 22 M$\Omega$ resistor is used as the pull-up load. (**d2**) Logic operations and experimental truth table of the resistive-load ZnO NW NOR logic gate. *Blue curve* and *green curve* represent the strain input applied on SGT 1 and SGT 2, respectively [23]

and NOR gates with active loads (Figs. 5.5A(a3) and (b3)) exhibit better overall performance, such as larger logic swing, compared to passive-load NAND and NOR gates (Figs. 5.5B(c) and (d)).

### *5.3.2 XOR*

The strain-gated ZnO NW XOR logic was also realized by connecting two SGTs in parallel (Fig. 5.6(a)). The drain electrode of SGT 1 in Fig. 5.6(a) is connected to the electrical input $V_A$ while the drain electrode of SGT 2 is connected to $V_{\bar{A}}$, which is the logically complement electrical input to $V_A$. If the strain-gated input logic for SGT 2 is $B$, then the strain input logic for SGT 1 is $\bar{B}$. The change in the connections of the electrodes from those demonstrated in the NW SGI results in different logic functions. When the substrate is bent downward or upward, the electric output would be either $V_A$ or $V_{\bar{A}}$, with the overall output of the device

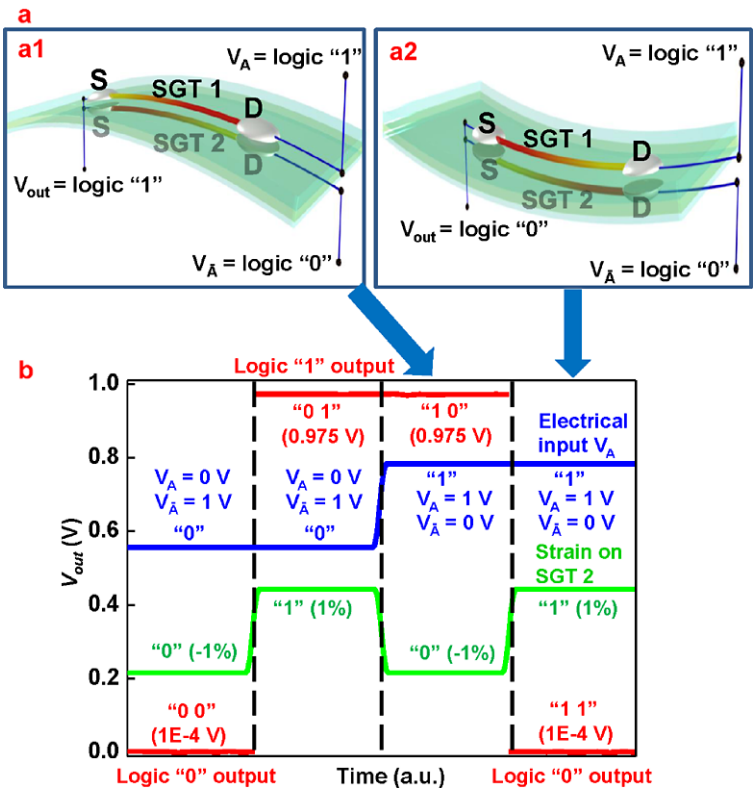


**Fig. 5.6** ZnO NW strain-gated XOR logic gate. (**a1**)–(**a2**) Schematics of a ZnO NW XOR logic gate performing logic operations on strain and electrical input. (**a1**) When the strain input applied on SGT 2 is logic "0" and the electrical input $V_A$ applied on SGT 1 is logic "1", SGT 1 is on and SGT 2 is off. Therefore the electrical output is logic "1" for the XOR gate. (**a2**) When the strain input applied on SGT 2 is logic "1" and the electrical input $V_{\bar{A}}$ applied on SGT 2 is logic "0", SGT 1 is off and SGT 2 is on. Therefore the electrical output is logic "0" for the XOR gate. (**b**) Logic operations and experimental truth table of the ZnO NW strain-gated XOR logic gate. The *red line* is the electrical output of the XOR gate. *Blue* and *green lines* represent the electrical and strain input applied on SGT 1 and SGT 2, respectively. We use the abbreviation a.u., arbitrary units [23]

logically expressed as $V_{\text{out}} = \bar{B}V_A + BV_{\bar{A}}$, which is the XOR logic. The output voltages of the XOR gate versus the input gate strains are shown in Fig. 5.6(b).

If drain electrodes of SGT 1 and SGT 2 in Fig. 5.6(a) are connected independently to arbitrary electrical input signals $D_1$ and $D_0$ rather than logically complements ($V_A$ and $V_{\bar{A}}$), the XOR gate demonstrated above is essentially a 2:1 multiplexer (MUX), with a control bit $B$ that is the input strain logic applied on SGT 2. Analogously, an n:1 MUX enables us to pick one of the n inputs and direct it to the output. When $B$ is logic "1", SGT 1 is off and the output is determined by the input connected to the drain electrode of SGT 2. Conversely, when $B$ is logic "0", SGT 2 is off and the output is determined by the input connected to the drain elec-

trode of SGT 1. Reversely, if the input $D_1$ and $D_0$ act as the output ports and the output for MUX as the input side, the device acts as a demultiplexer (DEMUX). The circuit can be expanded easily to create larger MUXs based on the above basic structures. The NW strain-gated MUXs and DEMUXs are critical logic components for processing mechanic-electrical signals.

## 5.4 Summary

By utilizing the gating effect produced by piezoelectric potential in a ZnO NW under externally applied deformation, SGTs have been fabricated, using which the universal logic operations such as NAND, NOR and XOR gates have been demonstrated for the first time for performing piezotronic logic operations [23]. In contrast to the conventional CMOS logic units, the SGT-based logic units are driven by mechanical agitation and relies only on $n$-type ZnO NWs without the presence of $p$-type semiconductor components. The mechanical–electronic logic units can be integrated with NEMS technology to achieve advanced and complex functionalities in nanorobotics, microfluidics and micro/nanosystems. Recently, the integration of the other two important components in a self-powered autonomous intelligent nanoscale system, the energy harvesting and the sensing/detecting parts, has been demonstrated [31] and ZnO piezotronic logic devices can be further integrated with the ultrasensitive ZnO NW sensors and ZnO NW-based nanogenerators to achieve a self-sustainable, all nanowire based, multifunctional self-powered autonomous intelligent nanoscale system.

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