Determining the Suitability of FPGAs for a Low-Cost, Low-Power Underwater Acoustic Modem

Ying Li[1,*], Lan Chen[1], Bridget Benson[2], and Ryan Kastner[2]

[1] 7th Research Group, Institute of Microelectronics of Chinese Academy of Sciences
Beijing 100029, P.R. China
[2] Department of Computer Science and Engineering, University of California, San Diego
La Jolla, CA92037, USA
liyjennifer@yahoo.com.cn, chenlan@ime.ac.cn,
{b1benson,kastner}@cs.ucsd.edu

Abstract. Few dense underwater wireless sensor networks exist because commercial acoustic modems are designed for sparse, long range, applications and are thus too expensive and power consuming for small, dense, sensor nets. In order to enable the proliferation of dense underwater sensor networks, a new low-cost, low-power acoustic modem must be designed. This paper investigates whether an FPGA is a suitable platform for such a modem design. We present the design and in-water test results of a complete FPGA implementation of a Frequency Shift Keying underwater digital transceiver and compare its cost and power consumption to other research underwater digital transceivers implemented on different hardware platforms.

Keywords: underwater acoustic modem, FPGA, FSK, sensor networks.

1 Introduction

Small, dense underwater sensor networks (containing 10s to 100s of nodes spaced 10s to 100s of meters apart) have the potential to greatly improve environmental (pollution, coral reef, seismic, ocean current, etc.) and structural (oil platform, pipeline, undersea tunnel, etc.) monitoring by providing high temporal and spatial resolution data of a given region of interest. This data can provide increased insight into episodic and periodic processes localized in a region of interest leading to greater understanding of our earth's bodies of water and the increased safety of mankind. Few dense networks currently exist because commercial off-the-shelf (COTS) modems' power consumption, ranges, and price points are all designed for sparse, long-range, expensive systems rather than small, dense, and cheap sensor-nets [1]. For example, Linkquest underwater modems all cost > $8000 [2] and require a minimum of 4W transmit power. Therefore, a new low-cost (to allow for the deployment of 10s

* Corresponding author.

W. Deng (Ed.): Future Control and Automation, LNEE 173, pp. 509–517.
springerlink.com

to 100s of nodes), low-power (to allow for long deployment) underwater acoustic modem must be designed.

We have designed a low-cost modem for small, dense underwater sensor networks by starting with the most critical component from a cost perspective – the transducer. The design substitutes a commercial underwater transducer with a home-made underwater transducer (<$50) and builds the rest of the modem's components (its analog and digital transceiver) around the properties of the transducer to extract as much performance as possible. This paper focuses on determining whether a field programmable gate array (FPGA) provides a suitable hardware platform for the digital transceiver of the low-cost, low-power modem.

Most existing research underwater modem designs [3-5] make use of digital signal processors for their digital transceivers. As many control and signal processing applications can often be implemented quickly on DSPs, designers often do not even consider implementing the design on an FPGA due to the specialized knowledge and increased design time of a hardware implementation. And, although studies have shown that FPGAs have evolved into highly valued DSP solutions platforms that reduce overall systems costs and power consumption for high throughput applications, there is still little evidence as to whether an FPGA provides power and cost benefits for simpler, lower-throughput applications [3].

Thus, design time aside, this paper investigates whether an FPGA provides a suitable digital hardware platform for the low-cost, low-power underwater modem design. The major contributions of this paper are:

- A fully implemented and tested FPGA implementation of an underwater FSK digital transceiver
- A hardware software (HW/SW) co-design test platform for real-time functional verification of the digital transceiver
- A power consumption comparison between different underwater digital transceiver implementations

Section 2 is a brief overview of our complete acoustic modem system. Section 3 describes the details of the FPGA digital transceiver design including the digital down converter, symbol synchronizer, and modulator/demodulator. Section 4 describes the HW/SW co-design used for accurate control and I/O. Section 5 presents in-water test results of the full modem design and compares the power consumption and cost of digital transceiver to existing research underwater digital transceiver designs. Section 6 is the conclusion.

2 Acoustic Modem Design

Underwater acoustic modems consist of three main components: 1. an underwater transducer, 2. an analog transceiver, and 3. a digital transceiver for control and signal processing. The most costly component is the underwater transducer as commercially available underwater omni-directional transducers (such as those as seen in existing research modem designs [4-6]) cost on the order of two to three thousand dollars. To

substantially reduce costs in our complete acoustic modem design, we substituted a commercial transducer with a lab-made transducer made from cheap piezoelectric ceramic material and potting compound. Our transducer has a center frequency of 40KHz, a narrow bandwidth, an input power capacity of about 50W, and costs <$50. To substantially reduce power consumption, our analog transceiver, under development, maximizes power efficiency in the transducer's frequency range, and contains a power management circuit to lower the output power of the transmitter when the actual distance between transmitter and receiver is small. The digital transceiver should be both low-cost and power efficient to compliment the full modem's design. The analog components' narrow operating frequency range governs the selection of the physical layer protocol for the digital transceiver implementation.

Frequency shift keying is a modulation scheme that has been widely used in underwater communications (especially in the shallow water, short distance environment we target) over the past two decades due to its resistance to time and frequency spreading of the underwater acoustic channel [4, 7]. Due to its relative simplicity and narrow bandwidth requirements, FSK is a suitable physical layer protocol for our low-cost, low-power underwater acoustic modem design as it can be implemented in a small, low power device and meet the frequency requirements of the modem's analog hardware. Table 1 shows the time and frequency parameters used in the FSK design.

Table 1. Modem parameters

Properties	**Assignment**
Modulation	FSK
Carrier frequency	40 KHz
Mark frequency	1 KHz
Space frequency	2 KHz
Symbol duration	5 ms
Sampling Frequency	192 KHz
Baseband Frequency	16 KHz

3 Design of UWSN FSK Digital Transceiver

3.1 Digital Down Convertor

The digital down converter is responsible for converting high resolution signals to lower resolution signals to simplify subsequent processing. It takes the incoming signal *adc_in* and multiplies it with a locally generated 40kHz signal. The mixed signal then passes through a low pass filter to filter out the high frequency components. Then the signal is downsampled from 192kHz to 16kHz to reduce processing power. The low-pass filter is a small 20-tap FIR filter designed using Spiral tool [8].

3.2 Modulator/Demodulator

The modulator/demodulator is responsible for translating a bit stream into a waveform and vice versa by shifting the frequency of a continuous carrier to the 'mark' or 'space' frequency each symbol period.

The modulator takes a binary input and selects to generate a sinusoidal wave using a cosine look up table. The phase angle offset is calculated using the formula:

$$\text{Offset} = \text{round}\ (\text{size} * F / Fs) \tag{1}$$

Where *size* is the number of elements in the look up table, *F* is the mark or space frequency and *Fs* is the sampling rate.

The demodulator uses the classic 'matched' filter structure, which is optimal for FSK detection with white Gaussian noise interference. It works by sending a symbol duration of the received signal through two add-and-shift band-pass filters. An energy detection block is applied to determine the relative amount of energy in each frequency band.

3.3 Symbol Synchronizer

Symbol synchronization, the ability of the receiver to synchronize to the first symbol of an incoming data stream, is the most critical and complex component in our digital transceiver design. When the modem receiver obtains an input stream, it must be able to find the start of the data sequence to set accurate sampling and decision timing for subsequent demodulation. Without accurate symbol synchronization, higher bit error rates incur thus reducing the reliability of the wireless network.

Our symbol synchronization approach relies on the transmission of a predefined sequence of symbols, often referred to as a training, or reference sequence. The transmitter sends a packet that begins with the reference sequence and the receiver correlates the received sequence and the known reference sequence in order to locate the start of the packet (and start of the first symbol). When the reference and receiving sequence exactly align with each other, the correlation result reaches a maximum value and the synchronization point can be located as the maximum point above a pre-determined threshold. We use a 15-bit Gold code as our reference sequence and perform a correlation with a 15-bit orthogonal Gold code to set a dynamic threshold. Due to space constraints, details of our symbol synchronization implementation and design considerations can be found in [9].

4 HW/SW Co-design

Xilinx Platform Studio 10.1 is applied to build a HW/SW co-design for accurate control and I/O of the digital transceiver. The co-design consists of the digital transceiver, a UART (Universal Asynchronous Receiver Transmitter) to connect to serial sensors or to a computer serial port for debugging, an interrupt controller to

process interrupts received by the UART or the transceiver, logic to configure the on board ADC, DAC, and clock generator, and MicroBlaze, an embedded microprocessor to control the system (Figure 1).

The MicroBlaze processor interfaces to the digital transceiver through two fast simplex links (FSLs), point-to-point, uni-directional asynchronous FIFOs that can perform fast communication between any two design elements on the FPGA that implement the FSL interface. The MicroBlaze interfaces to the interrupt controller and UART core over a peripheral local bus (PLB), based on the IBM standard 64-bit PLB architecture specification.

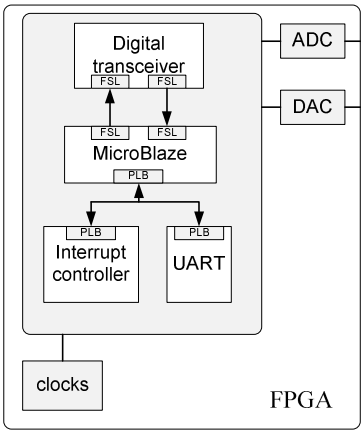

Fig. 1. HW/SW Co-Design for the digital transceiver

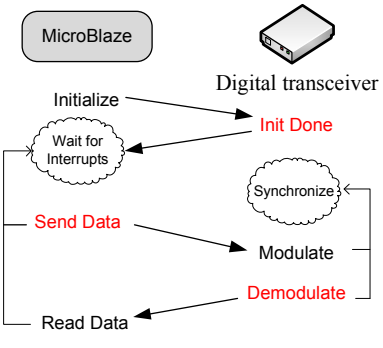

Fig. 2. Modem Control Flow. Interrupts are shown in red

Upon start-up, the MicroBlaze initializes communication with the digital transceiver through sending a command signal through the FSL bus signaling the transceiver to turn on. When the transceiver is ready to begin receiving signals, it sends an interrupt back to MicroBlaze to indicate initialization is complete. The transceiver then begins the down conversion and synchronization process, processing the signal received from the ADC and looking for a peak above the threshold to

indicate a packet has been received. If the transceiver finds a peak above the threshold, it finds the synchronization point, and demodulates the packet. The demodulated bits are stored in the FSL FIFO. When the full packet has been demodulated, the transceiver sends an interrupt indicating a packet has been received and the MicroBlaze may retrieve the packet from the FSL. The transceiver then returns to synchronization, searching for the next incoming packet.

After initialization, the MicroBlaze remains idle, waiting for interrupts either from the transceiver or UART. If it receives an interrupt from the transceiver indicating that a packet has been demodulated, the MicroBlaze reads the bits from the FSL FIFO and sends the bits over the UART to be printed on a computer's Hyperterminal for verification. If the MicroBlaze receives an interrupt from the UART, indicating that the user would like to send data, the MicroBlaze sends a command to the transceiver to send the bitstream the MicroBlaze places in the FSL. The transceiver then modulates the data from the FSL and sends the modulated waveform to the DAC for transmission. The MicroBlaze then returns to waiting for interrupts from the transceiver or the UART and the transceiver returns to synchronization, searching for the next incoming packet. This control flow is depicted in Figure 2.

5 Results

The digital transceiver design has been fully tested on a FPGA prototype platform, the DINI DMEG-AD/DA [10]. The test packet consisted of the 15 bit Gold Code ,011001010111101, followed by a 385 bit packet of randomized signals. Using our full modem design (the homemade transducer, analog transceiver, and digital transceiver), we sent packets in a 0.5m tank of water, a 50m swimming pool, and in Westlake, a freshwater lake in Westlake Village, CA. The results of bit error rate vs. SNR, are shown in Figure 3 [11]. All tank and lake tests achieved a bit error rate of less than 5% for distances up to 380 meters. The current modem design, without channel equalization, did not perform well in the pool's high multipath environment.

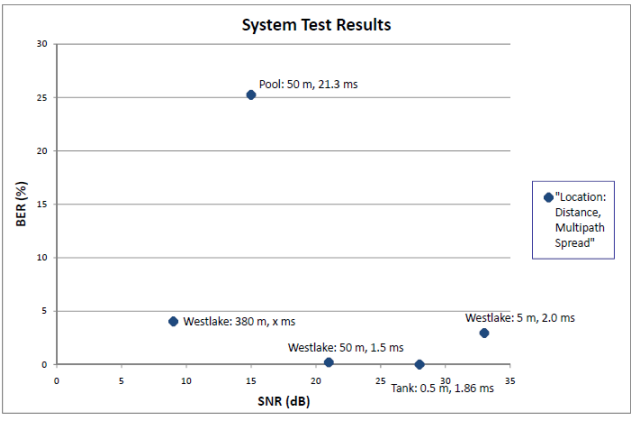

Fig. 3. Test results

We obtained a power estimate of the FSK digital transceiver design on various FPGA devices by entering the resource values of the HW/SW co-design into the Xilinx XPower Estimator 9.1.03 and the Altera Cyclone IV PowerPlay Early Power Estimator. The devices reported (except for the Virtex IV XC4VLX100 which is the device we used for prototyping) are in device families known for their low power consumption (the Xilinx Spartan 6 and the Altera Cyclone IV being some of the newest FPGA device families on the market). The particular devices reported are the smallest devices in their family that fit the total modem design. The letters 'Q', 'D', and 'T' in Table 3 stand for 'quiescent,' 'dynamic', and 'total' power respectively.

Table 2. FPGA power consumption

Device	Q Pwr (W)	D Pwr (W)	T Pwr (W)
XC4VLX100	0.775	0.2	0.975
XC3S4000	0.274	0.105	0.379
XC6SLX150T	0.212	0.021	0.233
EP4CE30	0.087	0.06	0.147

Table 3 compares the total digital processing power and cost of the digital transceiver design with existing underwater digital transceiver designs using various modulation schemes and platforms. From Table 3 we notice our FSK design on an FPGA provides comparable cost and power to other FSK designs.

Table 3. Modem design comparison

Mod	Device	Platform	T Pwr (W)	*Cost ($)
FSK[4]	Fixed DSP	TMS320C5416	0.180	45
FSK[12]	MCU	Blackfin 533	0.280	25
PSK[4]	FP DSP	TMS320C6713	2.0	25
DSSS[5]	FP DSP	TMS320C6713	1.6	25
Ours	FPGA	XC6SLX150T	0.233	14
	FPGA	EP4CE30	0.147	40

6 Conclusion

This paper investigates whether an FPGA provides a suitable digital hardware platform for the low-cost, low-power underwater modem design. We describe a

complete FPGA implementation of a FSK underwater acoustic digital transceiver and compare its cost and power consumption to other research underwater digital transceiver designs. Although an apples to apples comparison cannot be made, the cost and power estimates suggest that the FPGA provides comparable cost and power consumption to a fixed point DSP and offers the advantage of a relatively easy transition to ASIC once volume dictates.

Our anticipated cost and power estimates for the full underwater acoustic modem prototype (without housing or batteries) are shown in Table 4.

Table 4. Cost and power estimates for the underwater modem

	Cost ($)	**Power (W)**
Transducer	50	N/A
Analog Transceiver	150	TX:1.2-6.9 RX:0.275 Idle:0.240
Digital Transceiver	150	TX: 0.097 RX: 0.147 Idle: 0.087

Acknowledgment. This material is based upon work partially supported by the china scholarship council and partially supported under national science foundation grant #0816419 and a national science foundation graduate research fellowship.

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