Modular: The Super Computer

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Abstract. This article is deals with the history modular arithmetic, based on the rest classes calculus system «Restklassenarithmetik» (RCCS), or Modular Arithmetic, regarding its creation and development in the USSR. Characteristics of the USSR first modular super-computers: "T-340A", "K-340A", "Diamond (Алмаз)" and "5E53" and their development history are briefly considered. A brief analysis of the weakening of interest in the modular arithmetic in the USSR and its subsequent resumption of the Russian Federation is given. It also provides information on holding the 2006 special commemorative Scientific International Conference "50 Years of Modular Arithmetic" in the town of Zelenograd, Moscow.

Keywords: Modular Arithmetic, RCCS, K-340A, 5E53, Yuditski, Akushskiy.

1 Modular Arithmetic

In 1955 in Prague was published a collection of proceedings "Stroje Na Zpracovani Informaci", vol. 3, Nakl. CSAV that contains two articles: one by M. Valach and another by M. Valach and A. Svoboda. In these articles the idea to use operations on

$$M = p_1 p_2 \ldots p_n$$

residue ring, where $p_1, p_2, \ldots, p_n$ is in pairs mutual-simple numbers, instead of the $M = 2^n$ residue ring operations on computer numbers initially advanced. The known Chinese remainder theorem, which before was treated as the structural theorem of abstract algebra, guaranteed the specified parallelism in calculations above integers provided that the result of ring operations belongs to the range of integers defined by product of modules $p_1 p_2 \ldots p_n$. As a result, the new position-independent notation formed has received the name «residue number system» (RNS). There was a new scientific direction in modular arithmetic based on RNS.

Fig. 1. Feodor Viktorovich Lukin

Soon the idea became known in the USSR. Compared with the sketchy information from different sources, it is possible to reconstruct this history as follows. Approximately

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1957 regarding the "Almaz" (then "KB-1") the information on works in the USA on modular arithmetic arrived. The chief engineer of the Almaz, F.V. Lukin (Figure 1.), had personal experience in the design of computing devices and, especially, of their application in the largest systems. He appreciated perspectives of this direction. Feodor Viktorovich was the main organizer and the patron of works on the development of modular arithmetic. His diligence received a robust and successful development in the country. The beginning of its demise coincides with his departure from life.

Notwithstanding, the Almaz was not an engagement in the design of a computer and F.V. Lukin had sent the inquiry to the scientific research institute of electronic machines (in Russian - NII EM). In 1953, he was their chairman of the state commission on acceptance of computer "Strela", whose first appearance had been established in the Almaz. The inquiry had interested the mathematician Israel Akushsky and his chief leading the design of computer Davlet Juditsky, to become the founders of modular arithmetic in the USSR. One of leading theorists in the RNS method and active participants of its practical application (Dr.Sci.Tech.), professor and academician Academy of Sciences of Kazakhstan, Viljan Amerbaev recollects:

> "*Israel Akushsky told to me, that first information about RNS he has received from F.V. Lukin in the form of the inquiry on works in the USA. According to Israel Jakovlevich, Feodor Viktorovich considered RNS as very perspective direction of development of computer facilities*".

After this, the articles by A. Svoboda and M. Valach had arrived to I.J. Akushsky for preparation of its abstract. The initial information received (rather brief and superficial) has started the scientific research of I.J. Akushsky and D.I. Juditsky. The first attempt in the country to comprehend principles of construction modular computer was undertaken between 1957 and 1958 in NII EM by J.J. Bazilevsky, J.A. Shrejder, I.J. Akushsky, and D.I. Juditsky. However, it had not received uniform understanding and not all participants had taken a liking toward the essence of RNS.

2 Super-Computer "T-340A" and "K-340A"

In 1960, F.V. Lukin was recently nominated the director of the scientific research institute NII DAR (then the NII-37). He invited D.I. Juditsky and I.J. Akushsky to design the computer. D.I. Juditsky became the chief of the department and I.J. Akushsky became the chief of the laboratory in this department.

Fig. 2. Israel Jakovlevich Akushsky

Between 1960 and 1963 in this department, the first modular super-computer in the country (the T-340A) was designed as an experimental model of the complicated system. (Here, a super-computer is understood as a computer with record-breaking high characteristics at that time). The theory and practice of variant modular arithmetic principles of construction of the computer was designed on this basis by I.J. Akushsky, D.I. Juditsky, and E.S. Andrianov. This computer had really worked for many years in the experimental system. The received

results have been used in designing the K-340A computer, which has been mastered in a batch production and became the base for all systems designed in those years within NII DAR. In these computers, they released the principles of independent commands and data memory channels.

Operative memory was executed in the form of 16 blocks each with 1K-word capacity. Each block had two ports for input-output of information with subscribers (with an opportunity of a parallel exchange with any number of blocks) and with the processor. For speed increase, they realized program stratification of operative memory with alternation of the reference of the processor to blocks. In addition to the multiport, they applied buffer memory to two-operational commands. (Each command was carried out on two operations, each of which in other computers of that time was executed in the form of a separate command.) These features of memory system construction have provided high efficiency of the computer; delays were practically non-existent regarding the reference to memory of great volume (a scourge of the computer of those years). The speed of the T-340A and K-340A computers reached 1.2 million doubled, or 2.4 million single operations per second (OPS). Typical speed of the computer in those days was measured by tens or hundreds thousands OPS. By two factories it has been able to produce more than fifty K-340A computers, some of which in the structure of systems are still in operation until now - in 2006 it is forty years!!

Table 1. Specifications for the "T-340A" and "K-340A" Computers

The main designer:	T-340A - D.I. Juditsky, K-340A - D.I. Juditsky, after L.V. Vasiljev.
Development: NII DAR:	T-340A - 1960 … 1963 K-340A - 1963 … 1966
Manufacturers:	An experimental plant at NII DAR and the Sverdlovsk factory of radio equipment, per 1966-1973 it is let produce more than 50 complete sets.
Word length of data and commands:	45 bit
Notation:	Residue number system (RNS)
RNS - the bases and order of a word score by them:	
The bases:	2; 5; 23; 63; 17; 19; 29; 13; 31; 61.
Order of a word:	1; 2-4; 5-9; 10-15; 16-20; 21-25; 26-30; 31-34; 35-39; 40-45.
Performance:	1.2 million two-operational OPS (in the standard calculation, up to 2.4 million OPS)
Detection of an error in a word:	At performance of operations in the arithmetic device
Multiport buffer memory:	16 x 45 bit
RAM:	16K 45-digit words (720K bit)
ROM of commands:	16K 45-digit words (720K bit)
Element base:	Transistors, diodes, ferrite, etc.
Power consumption:	33 KW
The size of a rack cabinets:	600 x 700 x 1800 mm
Number of rack cabinets:	12

3 Super-Computer "Almaz"

In the beginning of 1963, F.V. Lukin was appointed director of the Center of microelectronics (CM), built in Zelenograd. One of its primary goals was:

> *"Design of construction principles of the radio-electronic equipment and the computer on the basis of microelectronics, the organization of their manufacture, transfer of this experience to the corresponding organizations of the country".*

To perform this task, Feodor Viktorovich invited his well-known collective of the T340A and K340A computer founders led by D.I. Juditsky and I.J. Akushsky. By this time the T-340A computer had been designed, constructed, and modified. The design of the project of serial computer K-340A, its manufacturing and debugging on an experimental plant of NII DAR have been completed after leaving the group of specialists in Zelenograd by remained collective of employees under direction of Leonid Viktorovich Vasiljev. In 1964, they had formed a department of perspective computers in the enterprise known nowadays as scientific research institute of physical problems (NII FP). D.I. Juditsky was nominated the chief engineer of NII FP.

Fig. 3. Davlet Islamovich Juditsky

By the end 1965, three organizations were given the competitive task to design outline sketches of the high-performance super-computer with a release date of 30 March 1967. The organizations were (i) the center of microelectronics (the ministry of electronic industry (MEP), designer F.V. Lukin), (ii) the institute of exact mechanics and computer facilities (the ministry of the radio industry (MRP), designer S.A. Lebedev), and (iii) the institute of electronic operating machines (the ministry of apparatus making, designer M.A. Kartsev)

The computer was to include the following characteristics: data word length of 45 bits, performance of 2.5 to 3.0 million algorithmic OPS, complex functions in one command (one algorithmic operation on tasks of the customer on the average corresponded to the four usual operations of the computer), work with words of variable length, and a memory size of 2^{17} 45-bit words (5.625M bits). That is, the usual understanding that required a computer with speed nearby 10 (9 to 12) one million OPS. Best known, by the end of 1966 computers possessed speed in 4 to 12 times smaller demanded the following.

Firm	Model	Speed of the computer, one million additions/second	Speed of elements, nanosecond
IBM	360/75	1,0	5
CDC	6600	2,5	10
Philco	2000/212	1,5	5
Burroughs	B 5500	0,3	20
Sparry Rand	1108	1,2	5

So in Zelenograd, the design of the outline sketch of super-computer “Almaz”, designer D.I. Juditsky had begun.

All forces of CM were involved in creating the “Almaz” computer, shown if Figure 4. NII FP executed development of architecture and the processor of the computer; NII TM did the base construction, the power supply system, and input/output system; NII TT designed the integrated circuit (IC). In this aspect the project Almaz had conclusive advantage in comparison with S.A. Lebedev’s and M.A. Kartsev’s projects, since the newest element base was created here, in Zelenograd, and on this process it had great influence.

Alongside with the application of modular arithmetic, they found one more architectural way to obtain substantial growth of the general productivity of the computer. This was the decision widely applied in later systems of processing of signals by the introduction of a system of the processor of preliminary processing a signal. Soon, it became a new word in a science and technique. Into structure of the “Almaz” computer, they used three types of computing processors.

Fig. 4. Super-computer “Almaz” engineering control console

Table 2. Specifications for the “Almaz” Super-Computer

The outline sketch:	March I968
Main designer:	D.I. Juditsky, Supervisor of studies I.J. Akushsky
The developer:	Center of microelectronics, Zelenograd
Word length of data and commands:	45 bits
Performance:	7.5 million algorithmic OPS (in the standard calculation, up to 30 million OPS)
Notation:	Residue number system (RNS) with the additional basis
RNS - the bases and order of a word score by them:	
The bases:	2; 5; 23; 63; 17; 19; 29; 13; 31; 61.
Order of a word:	1; 2-4; 5-9; 10-15; 16-20; 21-25; 26-30; 31-34; 35-39; 40-45
Detection of double and correction of single errors:	Performance of operations in the arithmetic device, hardware majorization (2 from 3) in all other devices
Calculation value of special functions:	Used as an elementary command
Memory size:	128K 45-digit words (5,898M bits)
Fast buffer memory:	32 55-digit words
Element base:	IC series “Tropa”
Power consumption:	5 KW
The size of a rack cabinets:	550x800x1750 mm
Volume of the equipment:	11 rack cabinets, an engineering control console, external devices
The occupied area:	80,100 м^2

- A narrowly specialized non-programmable processor for preliminary processing the information acting in real time, named in the Almaz the Converter of the information (CI);
- A programmable modular processor which is carrying out the basic data processing;
- A programmable binary processor that carries out non-modular operations used for computer control procedures.

The information from a source comes to CI, passes preliminary processing in real rate of receipt that excludes necessity of its intermediate storage. The results of this processing (their volume repeatedly less initial) act on the modular processor. Calculations have shown, that offered CI has the productivity equivalent about 4.0 million algorithmic OPS and allows to save about 3 megabits of memory. The modular processor of the "Almaz" computer has a productivity of 3.5 million algorithmic OPS. As a result, effective productivity of Almaz makes 3.5 + 4.0 = 7.5 million algorithmic OPS; that is, up to two to three times above requirements. See Table 2. These settlement data were confirmed by results of modeling on a universal computer and experimentally on the sample of the "Almaz" computer.

4 Super-Computer "5E53"

The outline sketch has been designed and on March, 30th, 1967 is presented to the customer. Competition has won computer "Almaz". In May, 1967 CM has received the order for design of the high-performance super-computer "5E53" and a 5-machine complex on its basis with the organization of a batch production in Zagorsk city an electromechanical factory (ZEMZ) MRP. The main designer 5E53 had been nominated D.I.Juditsky. In October, 1969 the collective of designers of the computer has been allocated in the independent organization - Specialized computer center (SVC), director D.I.Juditsky, the deputy science on I.J.Akushsky.

While Almaz was designed, the customer has specified characteristics: the 40-bit computer with performance on tasks of the customer up to 10 million algorithmic ops (nearby 40 million usual ops), the RAM 7,0M bit, PROM 2,9M bit, external memory 3G bit, the equipment of data transmission on hundreds kilometers was required.

The architecture 5E53 had many progressive decisions:

- Division of commands on administrative and arithmetic. Arithmetic commands (including preliminary and basic processing of the information) were carried out on modular processors, administrative - on binary.
- 8-levels the conveyor organization.
- Hardware block realization of arithmetic's: the block of addition/subtraction, the block of multiplication, the block of management of addresses, etc.),
- Division of data RAM and commands PROM,
- Division of trunks of commands bus and data bus,
- Hardware stratification of memory on 8 blocks with an alternating addressing on blocks.

Special RAM based on the integrated carrier (cylindrical magnetic film) was designed for the 5E53. By the speed, dimensions, weight, power, and cost it was much more attractive than an adaptability to manufacture applied RAM on ferrite cores. See Figure 5.

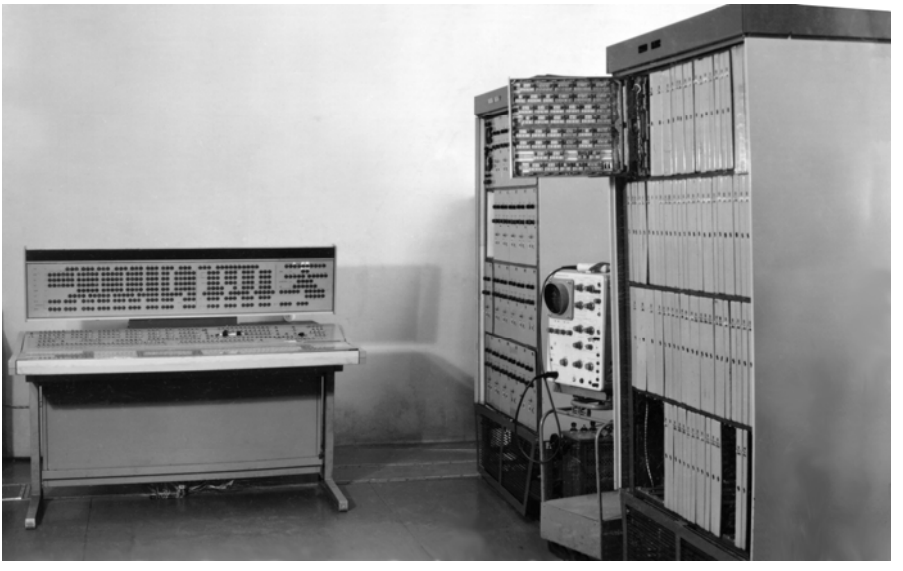

Fig. 5. Fragment of the pilot sample super-computer's 5E53

One more of the main problems was construction of PROM for storage of programs and constants which on tasks of the customer vary not often. Simple enough and fast constant memory, but supposing change of the information therefore was required. For 5E53 it is developed PROM with replaceable induction cards.

The storage on an optical type was designed as external memory of a large capacity. It had much in common with the cores at that time external memory on magnetic 35 mm tapes (a similar design, a drive, electronics), but differed in a data carrier and methods of record/reading of the information; it used photo/light-emitting diodes through an optical fiber on a film. As a result, the capacity of external memory increased by two orders of magnitude and attained 3G bits. The model of the storage was produced and it worked in the structure of the pilot model of the 5E53.

Attained reliability of the 5E53 was provided with self-corrected properties RNS in the arithmetic device, full majorization (2 of 3) all other systems of the computer's technology of installation intercell and interblock connections by a method turning and other means.

In the beginning of 1971, the design of the documentation was completed. All necessary tests of cells and subassembly have been finished and the pilot model of the 5E53 was fabricated and tested. On 27 February of 1971, eight complete sets of the design documentation was produced. Preparation of manufacture had begun. However, in the beginning of 1972 when preparation of manufacture 5E53 already came to the end and there has been begun manufacturing of separate devices of the computer, work on creation of system for which it intended stopped. Simultaneously,

Table 3. Specifications for the "5E53" Super-Computer

The contract design:	February 1971
Main designer:	D.I. Juditsky
Leading developers:	V.M. Amerbaev, I.J. Akushsky V.M. Radunsky, L.G. Rykov, M.N. Belova, P.F. Silantev, J.N. Cherkasov, V.S. Butuzov, V.A. Merkulov, P.V. Nesterov, V.N. Shugin
The developer:	Specialized computer center, MEP, Zelenograd
The manufacturer of the pilot sample:	Specialized computer center (SVC)
Word length:	Data - 20 bits and 40 bits Commands - 72 bits
Notation:	Residue number system (RNS) with the additional basis
The bases:	17; 19; 26; 31; 23; 25; 27; 29
Order of a word:	1-5; 6-10; 11-15; 16-20; 21-25; 26-30; 31-35; 36-40
Clock frequency:	6.0 MHz
Performance:	10 million algorithmic operations a second on tasks of the customer (40 million OPS) 6.6 million OPS on one the modular processor
Format of algorithmic operation:	Average is four usual
Time of performance modular operations:	1 step is 166 nanoseconds
Number of processors:	8 (4 modular and 4 binary)
PROM command:	Capacity: general is 2.8M bits A case is 573K bits The block is 72K bits Time of a cycle 332 nanoseconds, Rate of sample - 166 nanoseconds, Number of blocks - 40, Number of rack cabinets - 5.
The RAM of data:	Capacity: general{common} 7.0M bits A case is 1.0M bits The block is 4096 x 64 = 256K bits Time of a cycle is 700 nanoseconds Rate of sample is 166 nanoseconds Number of blocks is 28 Number of rack cabinets is 7
Volume of the equipment of the computer:	Types of rack cabinets is 7 and the engineering control console Number of rack cabinets is 24
The size of a rack cabinets:	1800 x 800 x 600 mm
Element base:	IC series "Tropa", "Posol", "Krug".
Power consumption:	60 KW.
Average time of non-failure operation:	600 hours
The occupied area (with the bench and repair equipment):	120м^2

work on the 5E53 stopped. There was no other consumer or other manufacturer in MRP. Although there was no demand for the 5E53, it appeared that in MEP the tasks for it continued. Low integration ICs could be designed with manual design; the time for large ICs and powerful systems of the automated designing has not yet arrived.

5 Destiny of Modular Arithmetic

In the 1960s and 1970s with respect to the designers of super-computer A-340A, K-340A, Almaz, and 5E53 in NII DAR, SVC and in the enterprises cooperating with them, serious scientific researches in the field of modular arithmetic were made. There were many publications on this theme in the open press, including and in the form of monographs. They had aroused serious interest at domestic and foreign specialists.

The true reasons for stopping the 5E53 project practically nobody knew. In fact, having received wide publicity in circles of experts and appreciated by them as a failure of the project, there began an independent life. There was an almost insuperable barrier on the further ways of introducing RNS in domestic computer facilities. Further use of modular arithmetic in the USSR energized enthusiasts, basically, in the theoretical plan and they were engaged only in the arithmetic. Foreign specialists of such shock have not gone though and there modular arithmetic has received more consecutive development. Figure 6 shows designers of the popular modular super-computers.

Fig. 6. V.S. Kokotin, M.D. Kornev, M.N. Belova, L.G. Rikov, V.S. Khajkov. Designers of the modular super-computers T340A, K-340A, Almaz, and 5E53. (22 September 2004 in Zelenograd, for D.I. Juditsky's 75-year birthday).

Currently, activity is characterized by two moments. First, there appeared to be a sharp increase in demand for the decision of tasks with prevalence of modular operations such as in processing of signals, images, cryptography, and toponymy, in addition to a demand for high reliability and productivity. On these tasks, modular arithmetic is also effective. Secondly, change the principles of creation of integrated circuits; decomposition of this process on "front-end" stages (circuitry designing) and "back-end" (layout designing), development of technology of the IP-blocks, programmed logic integrated circuit (PLIC) and a line of other innovations in the microelectronics, new devices facilitating integrated construction. As a result, interest in modular arithmetic again increases. The volume of publications has considerably increased for this theme and many enterprises have begun researches in the field of modular arithmetic.

The year 2005 marks the fiftieth anniversary of RNS based on modular arithmetic. It is a good occasion for summarizing its development, an estimation of a modern condition and prospects of development. Therefore, a number of the enterprises from five countries (Russia, Kazakhstan, Ukraine, Belarus, and the USA) have made a decision on carrying out of anniversary special scientific international conference "50 years of modular arithmetic". The materials of the conference appear on the site of the Moscow Institute of Electronic Technology (Technical University) (MIET)[1] and the Virtual computer museum[2] also are published in the form of the collection of proceedings of "50 Years of Modular Arithmetic". The anniversary international scientific and technical conference took place within the program of the International scientific and technical conference "Electronics and computer science - 2005". The collection of proceedings appear in Open Society "Angstrem", MIET, 2006, page 775 with ISBN 5-7256-0409-8.

The proceedings presented on conference testify that for fifty years, modular arithmetic has developed within independent scientific schools with various directions and real applications.

[1] http://www.mocnit.miee.ru/oroks22W

[2] http://www.computer-museum.ru/ and <http://www.computer-museum.ru/histussr/sokconf0.htm>