Chapter 6
Electronic Surface Properties of Semiconductor Surfaces and Interfaces

R. Shikler

Abstract In a world where the physical size of semiconductor devices is in the nano-region it is very important to understand the electronic properties of semiconductor surfaces and interfaces. These properties can be inferred indirectly from the measurement of work function variations across the surface. Kelvin probe force microscopy (KPFM) is a powerful tool that measures variations of work function and electrostatic potential distribution with nanometer resolution. In this chapter we review several important works that address the relation between KPFM measurements and the electronic or opto-electronic properties of the surfaces measured. We will start by explaining the dependence of the work function on the surface and specifically on surface states. This will be followed by a review on the work done on semiconductor surfaces and interfaces using KPFM. The focus is on correlating surface and interface properties with electro-optic device performance. This chapter is mostly focused on the works done on inorganic semiconductors with only a few examples on organic semiconductors.

6.1 Introduction

The ever decreasing dimensions of semiconductor devices increase the influence of the processes at their surfaces and interfaces compared to the bulk contribution. Therefore, understanding the electronic properties of semiconductor surfaces/interfaces is crucial for further development in this field. In general, an interface is defined as a boundary between media with different physical properties. For example, the interface between a semiconductor and vacuum or gas is referred

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S. Sadewasser and T. Glatzel (eds.), *Kelvin Probe Force Microscopy*, Springer Series in Surface Sciences 48, DOI 10.1007/978-3-642-22566-6_6,

to as a "free surface." or just a "surface." The interface between a semiconductor and another solid is usually referred to as an "interface." However, we shall sometimes use the term "surface" to denote any boundary. One of the basic properties of semiconductor surfaces is their work function. In this chapter we will try to understand the relation between the work function and the electronic properties of semiconductor surfaces.

One of the definitions for the work function of a metal, often used by experimentalists, is the difference between the barrier height on the metal–vacuum interface and the Fermi energy. This definition, however, does not specify the kinds of energies which contribute to the barrier height. In 1935 and 1936 Wigner and Bardeen have theoretically shown that the work function consists of two contributions: (1) an internal contribution from the bulk and (2) a contribution from a surface dipole barrier [1, 2]. Work done by Hölzl et al. [3] and Kiejna et al. [4] have demonstrated that for Tungsten for example, the work function can vary from 4.23 eV for the (1 1 3) surface to 5.7 eV for the (0 1 1) surface. These variations can affect various properties of the surface like atom absorption, see for example [4].

A similar picture holds for the case of semiconductors. The work function of a semiconductor is a property of its surface; it is largely affected by the electrical properties of the semiconductor surface. A comprehensive description of this subject can be found in many text books, for example by Many et al. [5], Mönch [6], Lüth [7] and Sze [8].

The termination of the periodic structure of a semiconductor at its free surface may form surface localized electronic states within the semiconductor bandgap and/or a double layer of charge, known as a surface dipole. The appearance of surface-localized states induces charge transfer between bulk and surface in order to establish thermodynamic equilibrium between the two. The charge transfer results in a non-neutral region (with a non-zero electric field) in the semiconductor bulk, usually referred to as the surface space charge region (SCR). This region may extend quite deeply into the bulk. Similar considerations are applied to a semiconductor interface.

The fixed charge trapped in surface states originates from bulk free carriers in the bands. We therefore expect the carrier density in the vicinity of the surface to deviate from its equilibrium value and result in a surface SCR. The surface may be found in three different regimes:

(a) Accumulation, where the majority carrier concentration at the surface is larger than its bulk value.
(b) Depletion, where the majority carrier concentration at the surface is smaller than its equilibrium value, but larger than the minority carrier concentration at the surface.
(c) Inversion, where the majority carrier concentration at the surface is smaller than the minority carrier concentration at the surface.

For example, case (b) is depicted in Figure 6.1 for the case of a p-type semiconductor. It is clearly shown that due to downward bending at the surface the distance between the Fermi level (E_F) and the conduction band minimum (E_c) is smaller

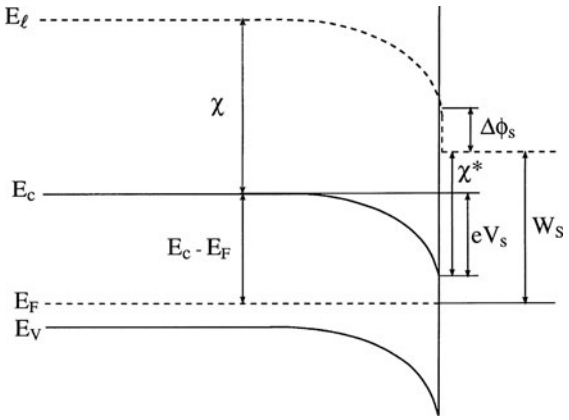

Fig. 6.1 Schematic diagram of the electronic band structure at a semiconductor surface [9]

at the surface with respect to the bulk. This implies that at the surface the density of electrons is larger than its bulk value. Additional quantities that are shown are the surface dipole ($\Delta\phi_s$) that causes the work function to change at the surface, the electron affinity (χ^*) and the work function (W_s). The SCR is also clearly visible in Figure 6.1 as the area where the bands are bent, i.e., where an electric field is present.

The SCR is obtained by solving the Poisson equation. The presence of a non-zero charge density implies a non-zero electric field and potential [8]. Therefore, even under equilibrium conditions the surface potential, denoted as V_s, is different from the electrostatic potential far away in the bulk. This explains the fact that the bands are bent in the vicinity of the surface (this variation manifests itself in a change of the work function because the value of $(E_c - E_F|_s)$, i.e., the distance between the conduction band minimum and the Fermi energy at the semiconductor surface is different from its bulk value). By definition, the energy band is lower the higher the electrical potential is, so that a positive V_s corresponds to downward-bent bands as seen in Figure 6.1. Because we are measuring the variation in the work function we are interested primarily in V_s and not in the exact "shape" of the surface SCR, i.e., the dependence of the electric potential on the distance from the surface. For a given set of semiconductor bulk and surface properties, the value of V_s is dictated by charge neutrality:

$$Q_{ss} = -Q_{sc}, \tag{6.1}$$

where Q_{ss} is the net surface charge and Q_{sc} is the net charge in the SCR (both per unit area). This is because the underlying crystal is the sole supplier of the surface charge. For the calculation of V_s we must know the functional dependence of Q_{ss} and Q_{sc} on V_s (see, for example, Kronik et al. [9]). This explains why by measuring the variation in the work function we can deduce the charge at the surface and the relating electronic properties.

The density and population of surface states may vary across the sample surface, and also the underlying doping concentration may vary (for example in pn structures see below). This means that Q_{ss} and also the surface potential V_s are not constant across the surface. In other words, variation of various sample parameters like doping concentration, surface states density, energy position of surface states, etc. can lead to spatial variations of the work function and therefore, of the contact potential difference (CPD). Another possibility is the presence of surface or interface dipoles. These dipoles can be created by partial charge transfer at the semiconductor/air interface in the presence of adsorbants (e.g., due to "tails" of interface state wave functions) [10–13].

One issue that influences the interpretation of results of Kelvin probe force microscopy (KPFM) measurements is the physical limitation of their lateral resolution. This is very important as the physical size of electronic devices become smaller and smaller. It is accepted that the finite tip size in scanning probe microscopies (SPMs) can have a profound effect on the obtained topographic image. Deconvolution of the tip shape from the image can be determined by several approaches [14–16]. The tip shape can then be used to restore the true surface topography from the measured image. In electrostatic force-based microscopes, the effect of the measuring tip is much larger because the measured forces have an infinite range. Tip effects in electrostatic force and KPFM were discussed and analyzed by several authors [17]. One of the simplest models was suggested by Hochwitz et al. [18], who modeled the tip by a series of (staircase) parallel plate capacitors. Hudlet et al. [19] have presented an analytical evaluation of the electrostatic force between a conductive tip and a metallic surface, while Belaidi et al. [20] have calculated the forces and estimated the resolution in a similar system. Jacobs et al. [21, 22] have extended the calculations for the case of a semiconductor sample, by replacing its surface by a set of ideal conductors with mutual capacitances between them. Another approach using integral equation-based boundary element method combined with modeling the semiconductor by an equivalent dipole-layer and image-charge model was reported by Strassburg et al. [23]. The key conclusion of these works is that the lateral resolution of the KPFM technique can be estimated to be below 20 nm thus giving it a certification as a high spatial resolution microscopy technique. A concise treatment of these issues can be found in Chap. 4 of this book. These theoretical works were complemented in recent years with many experimental works that demonstrated the KPFM ability to measure variations in $V_s(\vec{r})$ on a nanometric scale [24–38].

In the remainder of this chapter we will review these results and explain how a qualitative relation between the measured work function variations and the electrical properties of the surface is obtained. This relation can then be used to explain the influence of the surface on the performance of opto-electronic devices ranging from LED through solar cells to organic TFT. We specifically state that this is a qualitative relation as without exact knowledge of the bulk properties and the method used to fabricate the surface it is impossible to calculate a quantitative one.

6.2 KPFM Measurements of *pn* Junctions

Following the first measurements using KPFM of metal work functions [39–41] one of the basic and important structures that gained a lot of attention is a cleaved *pn*-junction. Devices whose structure is that based on a *pn*-structure like sample having a basic *pn* LED [24, 26, 28] and a laser diode [27] were cleaved and scanned on the cleaved surface as shown in Fig. 6.2.

The predicted built-in bias across the cleaved sample can be calculated using the doping concentrations [8]:

$$V_{\mathrm{bi}} = \frac{k_{\mathrm{B}}T}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right), \tag{6.2}$$

where k_{B} is the Boltzman constant, T the temperature, e the electron charge, N_A and N_D the doping concentrations on the p and n side, respectively and n_i the semiconductor intrinsic density. For example, the sample reported by Shikler et al. [24] that was grown using liquid phase epitaxy,[1] the expected value is $V_{\mathrm{bi}}^{b} = 2\,\mathrm{V}$, however, the measured difference is only $V_{\mathrm{bi}}^{s} = 1.33\,\mathrm{V}$ (the b and s superscripts stand for bulk and surface values) as it can be seen in Figure 6.3 [24].

The lower $V_{\mathrm{bi}}^{\mathrm{s}}$ (compared to $V_{\mathrm{bi}}^{\mathrm{b}}$) is most probably due to two main reasons: band bending due to semiconductor surface states, and/or external charge on the sample surface. Surface states (due to imperfect cleavage and/or oxides on the air exposed sample) can trap holes (electrons) on the cleaved surfaces of the p (n) sides of the junction, creating depletion type band bending opposite in sign on each side of the junction. Thus the bands will bend up in the n-doped region and down in the p-doped region, with the net result being a reduction of $V_{\mathrm{bi}}^{\mathrm{s}}$. The reduction of the built-in voltage on the surface may be used to derive the surface band bending and/or the surface charge on the cleaved crystal. However, the surface states distribution on

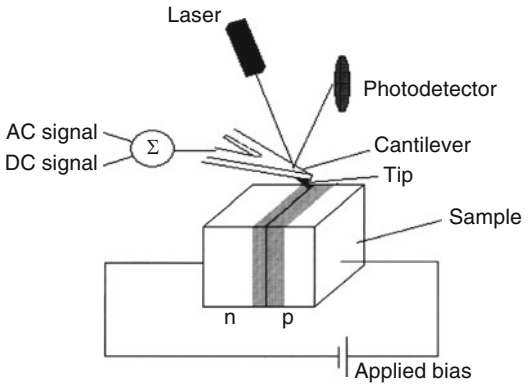

Fig. 6.2 Schematic of the cleaved GaP sample measurement setup under applied forward bias. Equilibrium measurements were conducted with $V_a = 0\,\mathrm{V}$

[1] Elma inc. 103460, Moscow, Zelenograd, Russia.

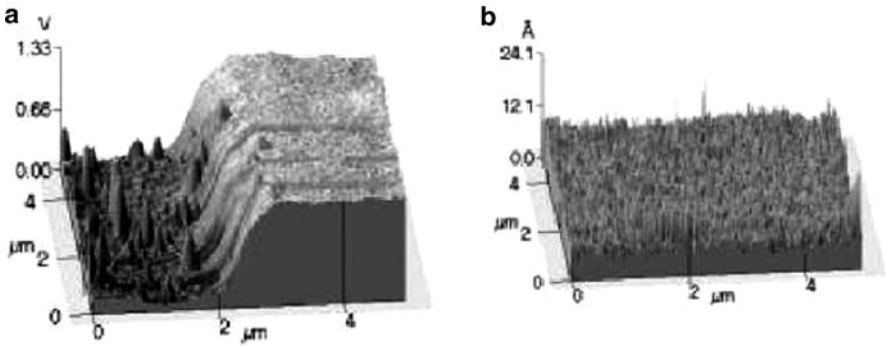

Fig. 6.3 (**a**) Contact potential difference measurements and (**b**) topography of a cleaved GaP *pn*-junction in equilibrium [24]

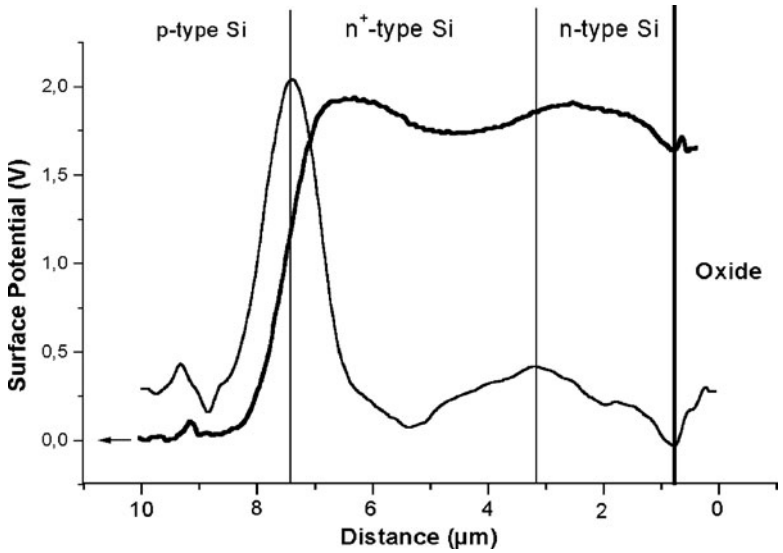

Fig. 6.4 Surface contact potential variations (*bold line*) and surface electric field (*thin solid line*) for reverse diode polarization as function of spatial location on the $pn^{+}n$ junction [29]

the cleaved junction surface is not known and therefore, the band bending can only be estimated by solving the Poisson equation assuming a constant distribution of surface charge [26]. The same phenomenon of reduction in the built-in voltage was also reported by Lévêque et al. [27]. When a forward bias is applied to the junction the built-in potential decreases, however the decrease is not the same as the applied bias. Similar results were reported for reverse bias by Doukkali et al. [29]. In their study they applied a reverse bias of 2 V to a $pn^{+}n$ junction with expected built-in bias at equilibrium of 0.88 V and measured instead of 2.8 V difference just under 2 V as can be seen in Figure 6.4.

The ability to detect the presence of surface states (surface charge) is very important especially for electro-optic devices like LED's and laser diodes. In these devices, part of the light is emitted through the cleaved plane. The emitted light can then be absorbed by the surface states which can lead to reduction in the emitted light intensity. We will shortly elaborate on this issue.

An important fact that can be observed in Figure 6.3 is the inhomogeneous distribution of the potential in the junction plane. Figure 6.3a shows small peaks on the left side of the junction that do not correspond to any topographic feature in Figure 6.3b. Moreover, on the right side of the junction there is a small protrusion at the middle of the right edge. When the junction was forward biased at V_a = 1.54 and 1.62 V the following was observed: some of the peaks at the left side disappear while others decrease in height compared to the average value at the left part of the junction. On the right side the small protrusion becomes larger when compared to the average value of the CPD on the right side as can be seen in Figure 6.5. These results show that the response of the surface is inhomogeneous which can lead in the case of LED to inhomogeneous emission of light.

The above studies lead naturally to the idea of measuring the interaction of light and surface states using KPFM. The basic of solar cells is the photovoltaic effect, where an electron hole pair created by light absorption separates and diffuses to the contacts. A specific variant of the photovoltaic effect is called surface photovoltaic effect. The surface photovoltage (SPV) is defined as the illumination-induced change in the surface potential. This effect, observed at Si and Ge surfaces, was first reported in a short note by Brattain in 1947 [42], followed by a detailed account some years later [43]. Combining the KPFM setup with optical pumping for SPV measurements with high spatial resolution was proposed by Weaver et al. [40]. Since then there were several studies in this area. Shikler et al. [25, 26] showed that light absorption by surface states can be responsible for the inversion of a *pn*-junction at the surface of a GaP LED. This effect, that is not possible in the bulk, is clearly shown in Figure 6.6.

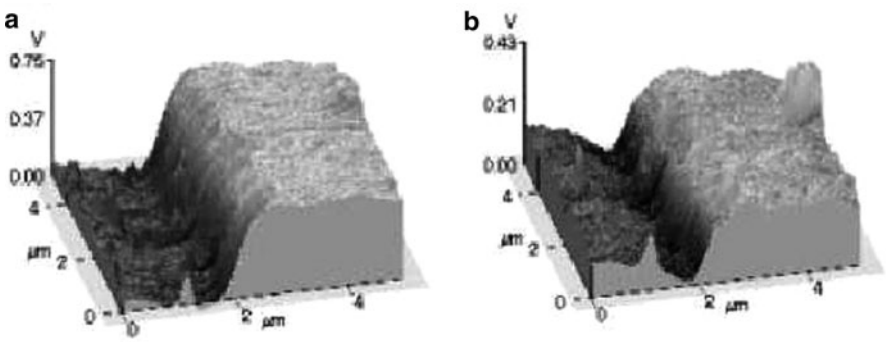

Fig. 6.5 CPD measurements of the GaP *pn*-junction under (**a**) 1.54 V and (**b**) 1.62 V forward bias [26]

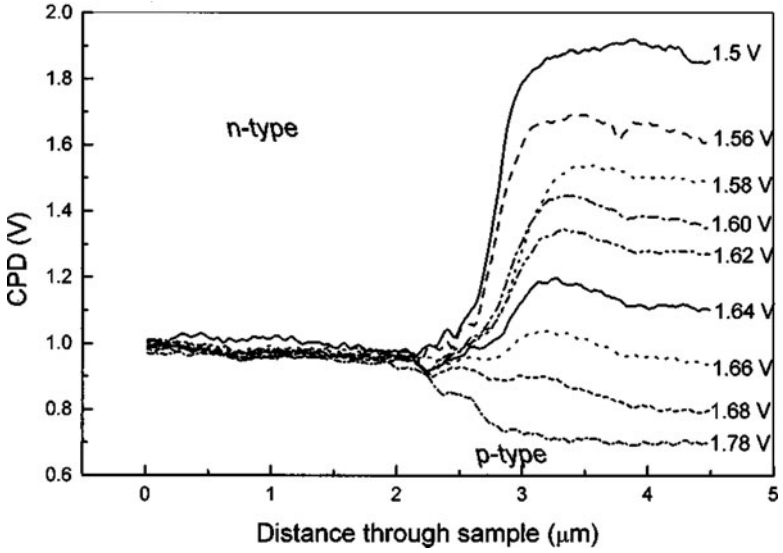

Fig. 6.6 Potential distribution across an GaP LED pn-junction under nine different applied forward bias [26]

The magnitude of $V_{\mathrm{bi}}^{\mathrm{s}}$ changes by about 1.1 V in the bias range between 1.5 and 1.78 V. This large change is unexpected based on the theory of pn-junctions [8]; this theory shows that V_{bi} in the bulk should decrease linearly with a proportionality factor of 1 with increasing forward bias. In principle, a change in $V_{\mathrm{bi}}^{\mathrm{s}}$ which is much larger than the external applied bias can be due to two reasons:

- Reabsorption of light emitted inside the device
- Charging or discharging of surface states

It was found that there is indeed a state whose energy is 2.16 eV below the conduction band minimum that has a transition that can increase the band bending at the p side of the junction as seen in Figure 6.6. Re-absorption of the LED internal emission increases the band bending at the cleaved surface. This may lead to several effects:

1. *High surface reverse currents.* As a result of the inverted junction on the surface, when the LED is biased in the forward direction, the junction on the surface will be under reverse bias. This will increase the device saturation current.
2. *Higher surface recombination rate.* Larger surface depletion fields increase the effective recombination velocity [44]. This will decrease the device efficiency.
3. *Change of the refractive index at the surface.* Large surface electric fields will change the refractive index at the surface due to the linear electro-optic effect. Changes of the surface refractive index will affect the LED radiation pattern.

An additional result, reported in this work, is the direct measurement of minority carrier diffusion length at the surface under illumination. This value is important for devices that are very thin in which it has the dominant length.

6.3 KPFM Measurements of Thin Film Solar Cells, the Role of Grain Boundaries

Recently, Streicher et al. [45] reported on locally resolved SPV on Zn-doped $CuInS_2$ thin films that are used for solar cells. In this work the authors report on a comparative study of pure $CuInS_2$ (CIS) and Zn-doped $CuInS_2$ (CIS:Zn) thin films using surface photovoltage spectroscopy (SPS) in combination with a KPFM setup.

In Figure 6.7 we see a series of normalized SPV spectra taken at different positions along the samples. The ability to take these spectra at nanoscale resolution is due to the combination of KPFM and optical pumping. Using this setup, the authors have shown that polycrystalline $CuInS_2$ and Zn-doped $CuInS_2$ thin films show homogeneous SPV across the sample surface. This indicates that the Zn doping does likely not result in local variations of the band gap. This is a very important result, since variation in the band gap can affect the efficiency of cells . The presence of the Zinc doping manifest itself in the presence of sub bandgap states that it can be described by an Urbach tail with $E_U \approx 74$ meV [46].

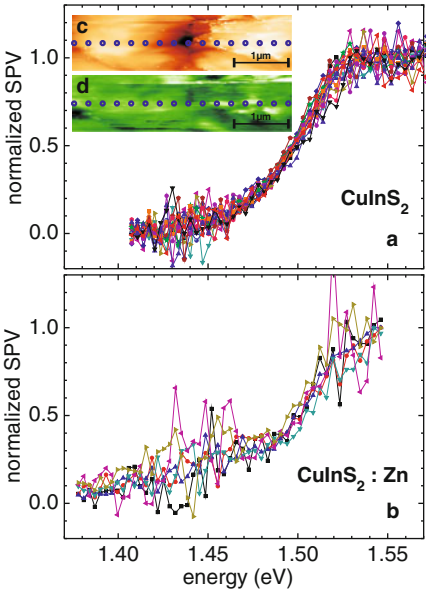

Fig. 6.7 Series of SPV spectra normalized to the maximum SPV of each spectrum for (**a**) pure $CuInS_2$ and (**b**) $CuInS_2$:Zn. The inset shows the position where the spectra on the $CuInS_2$ sample were taken in (**c**) topography and (**d**) work function [45]

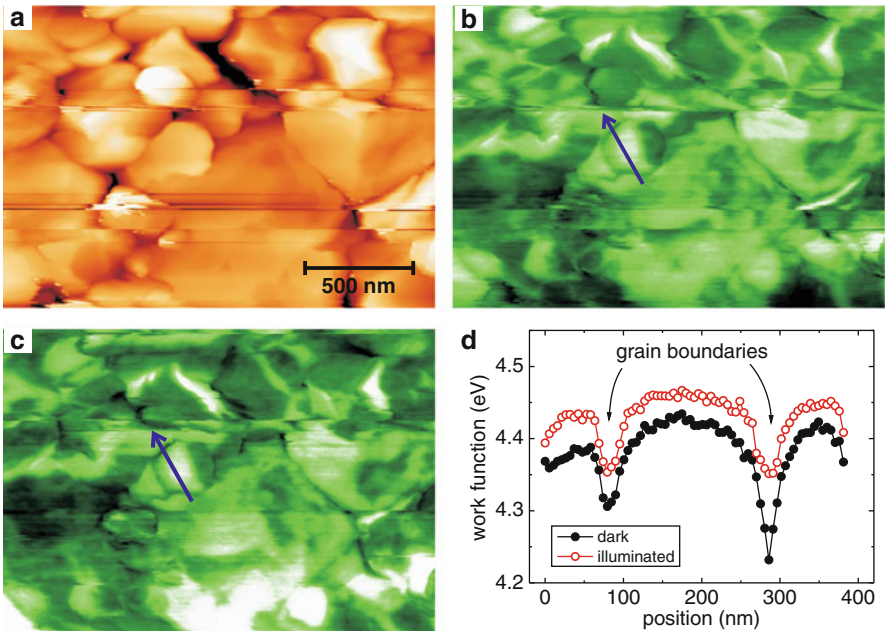

Fig. 6.8 KPFM measurement of a PVD grown $CuGaSe_2$ film. (**a**) Topography ($\Delta z = 360$ nm), (**b**) work function in the dark ($\Phi = 4.23$–4.50 eV) and (**c**) under illumination ($\Phi = 4.20$–4.50 eV). (**d**) Line profile along the *arrow* in (**b**) and (**c**), showing a drop in the work function at the grain boundaries [33]

Many thin films used as absorber in photovoltaic devices are polycrystalline materials. It is of interest to study the role played by the grain boundaries of these films. Sadewasser [33, 47] had reported on microscopic measurements of the individual grain boundaries in Cu–III–VI_2 chalcopyrite. Figure 6.8 shows AFM and KPFM images of a $CuGaSe_2$ film taken in the dark and under illumination. From the images we can infer that there is a dip in the work function at the grain boundaries. We also see the overall SPV response is positive and that it is larger at the grain boundaries than in the grain bulk. This indicates that the boundaries are probably charged. Such charged grain boundaries could increase current collection in the device, thereby compensating for the negative effects of recombination at the grain boundaries defects.

Similar results were reported for CdS/CdTe polycrystalline solar cells by Visoly-Fisher et al. [48, 49]. In their work they have observed the presence of a barrier for hole transport across grain boundaries in solar-cell quality CdTe, a conclusion supported by KPFM data. The barrier height varies between different grain boundaries. This barrier is expected to affect intergrain hole transport of the photocurrent. The demonstrated superiority of polycrystalline over single crystalline CdTe/CdS cells therefore implies that other mechanisms of current collection are operative in these cells (see Fig. 6.9).

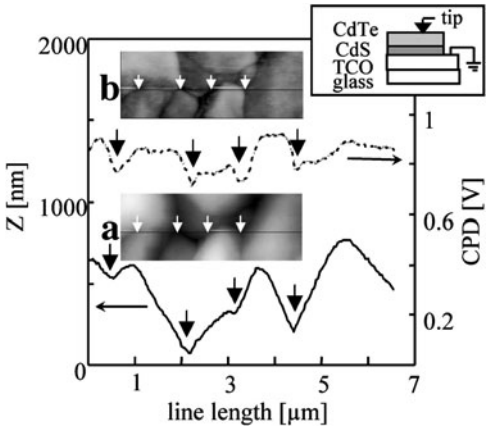

Fig. 6.9 (**a**) AFM topography image and line scan, and (**b**) KPFM image and line scan of a CdTe surface, taken simultaneously. The *lines* in the images indicate the locations of the line scans. The *arrows* indicate the locations of grain boundaries. Scan size was 2.4 µm × 6.7 µm, using a TiO_{2-x}-coated Si tip (Micromasch). The tip-sample separation was 30 nm, and the ac voltage amplitude was ∼6 V. The inset (*top right corner*) shows the schematic arrangement of the measurement. *TCO*: Transparent conducting oxide (here SnO_2:F)

Further measurements on the role of thin CdS films on Cu(In,Ga)Se_2 (CIGSe) solar cells showed that the deposition of a few nm thick CdS on a CIGSe solar cell can improve the quantum efficiency [50]. The authors found that the growth of a thin semiconductor film on top of a polycrystalline substrate can lead to nanoscale material modification around the substrate grain boundaries. When a thin layer of CdS was deposited on the top of CIGSe cells the resulting SPV is smaller and indicates a reduction of recombination as it can be seen in Figure 6.10. This effect is more pronounced at the grain boundaries.

6.4 KPFM Measurements on Organic Materials

To complete this review it will be beneficial to describe some of the work done with KPFM on organic materials. We will start by extending the topic of grain boundaries to the case of polycrystalline organics that are frequently used for thin film transistors (TFTs) [51–53].

Tello et al. [52] investigated charge trapping at the intergrain region (IGR) of pentacene made TFT. Organic field-effect transistors have experienced an impressive development in the last decade which has allowed the appearance of high performance devices with mobilities comparable to those of amorphous silicon [54]. One of the materials that has attracted major attention is pentacene. Mobilities as high as 3–5 $cm^2\,Vs^{-1}$ have been demonstrated in pentacene TFTs [55] and much attention has been devoted to the study of the correlation between the morphology and the

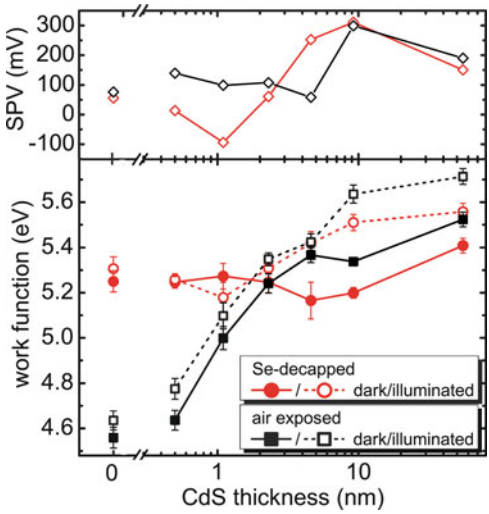

Fig. 6.10 Work function values (*lower graph*) of thin CdS films on a polycrystalline CIGSe film, determined in the dark and under illumination. The *error bars* indicate the full width at half maximum (FWHM) of a Gaussian distribution of the work function values and the *upper part* shows the values of the surface photovoltage [50]

charge transport properties [56]. In their work, they presented a KPFM study performed on transistors with different film thicknesses of the pentacene active layer in order to understand the effect of the film microstructure on the trapping of charges.

An example of an AFM and KPFM measurement in equilibrium and under bias of a TFT made from pentacene is shown in Figure 6.11. It is clear that the surface potential for V_{gs} = 0 V in this unbiased device is equal to 0V both in the pentacene grains and within the IGRs. When a negative bias is applied to the gate electrode, the surface potential in the pentacene grains does not vary, while a negative gate voltage dependent surface potential is measured in the IGRs. As the gate voltage becomes more negative, the potential in the IGRs reaches a minimum value (for $V_{gs} = -25$ V) and then increases again, although it does not go back to 0 V even at the highest bias.

These results provide clear evidence that in very thin pentacene films with island morphology bias stress-induced charge trapping occurs primarily in the thin IGRs between the pentacene islands. In these regions, only an incomplete charge accumulation can be formed and high gate voltages are required to charge portions of the film that are electrically unconnected to the rest of the film at lower gate bias. Once created, the trapped charges cannot be de-trapped in a short time scale. This result answers an important technological question about the operational stability of these devices which is limited by undesirable threshold voltage shifts during prolonged application of bias. The undesirable shift can be correlated with the charge trapping in the polycrystalline pentacene film. The correlation between the trapped charge and the topography indicates that the growth process plays an important role in determining the stability of the device.

The correlation of charge trapping and topographic structure was further observed in pBTTT TFT's [53]. In this work different mesophases exhibit different morphologies resulting in different surface potential distributions and different charge trapping in operating TFT.

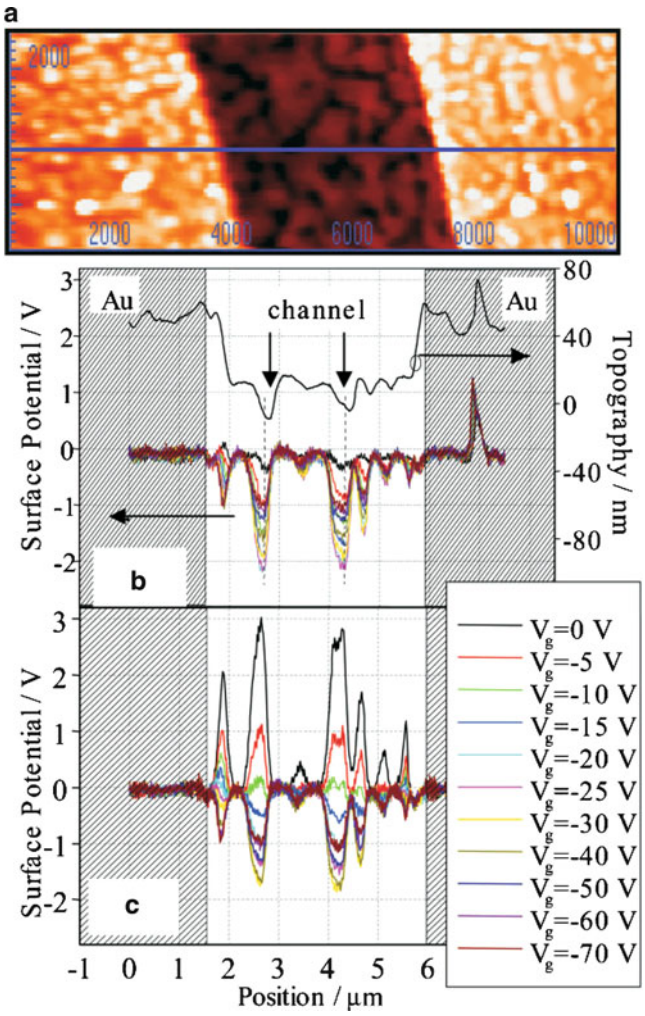

Fig. 6.11 (**a**) Topographic view of an unbiased pentacene TFT sample. The line scans were performed along the *blue line*. The scan area is approximately 2 µm × 10 µm. (**b**) Surface potential profile across the *blue line* at various gate voltages in a previously unbiased sample. The corresponding topographic profile is also shown. The *black arrows* point at the places where the IGRs are. (**c**) Surface potential across the same line, measured immediately after (**b**) [52]

6.5 Concluding Remarks

In this chapter we have reviewed some of the work done on inferring electronic properties of surfaces from KPFM measurements. The works presented show how KPFM measurements can be translated into valuable information regarding electronic and opto-electronic properties that take place in semiconductor devices.

Due to the high spatial resolution of the technique, nanoscale features can be studied and the physics of the processes that govern device performance can be deduced on nanometer scale.

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