From Sizing over Design Centering and Pareto Optimization to Tolerance Pareto Optimization of Electronic Circuits

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Abstract This paper presents an overview of sizing tasks in electronic circuit design and their corresponding formulations as optimization problems. We will start with the general multi-objective sizing problem. Then, the inclusion of statistically distributed parameters and of range-valued parameters into the scalar problems of yield optimization and design centering will be described. Finally, a problem formulation for considering these parameter tolerances by multi-objective Pareto optimization will be presented.

1 Parameters, Performances, Simulation

This paper deals with optimization of electronic circuits which are modeled with continuous signals in time and value, and which are usually nonlinear. Circuits of this type are usually described with nonlinear differential algebraic equations and often called analog circuits. Analog circuits are analyzed based on numerical integration with one of the many successors of the SPICE simulator [4]. Modern simulators are capable of handling mixed-signal circuits with digital parts, and of handling circuits which are described not only with transistor netlists, but with hardware description languages like VHDL-AMS or Verilog-AMS. It is worth noticing that not only analog and mixed-signal circuits and systems, but digital components as well may be described in this way. Hence, simulation-based design not only refers to analog design but to a general analog design view on any type of system. It is also worth noticing that numerical simulation provides the most significant way to abstract the analog design view from the physical level to the

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formal level of a performance function that maps the modeled circuit parameters $\mathbf{x} \in \mathbb{R}^{n_x}$ (simulator input) on the modeled circuit performance features $\mathbf{f} \in \mathbb{R}^{n_f}$ (simulator output, e.g., Gain bandwidth, delay):

$$\mathbf{x} \mapsto \mathbf{f} \tag{1}$$

Simulation of electronic circuits may take CPU times from seconds to minutes or hours. The cost for simulation is therefore by far dominating all other computational steps of an optimization process. This requires specific customized optimization approaches for electronic design.

We distinguish the following three types of parameters:

- Design parameters (e.g., transistor widths) $\mathbf{x}_d \in \mathbb{R}^{n_{xd}}$
- Statistical parameters (e.g., threshold voltage, oxide thickness) $\mathbf{x}_s \in \mathbb{R}^{n_{xs}}$
- Range parameters (e.g., supply voltage, temperature) $\mathbf{x}_r \in \mathbb{R}^{n_{xr}}$

2 Parameter Tolerances, Performance Specifications

Statistical parameters reflect the manufacturing variations which are transformed into a Gaussian distribution.

Range parameters reflect the circuit operating conditions. They are interval-bounded by upper bounds:

$$x_{r,i} \leq x_{r,U,i}\,,\ i = 1, \ldots, 2n_{xr} \tag{2}$$

Lower bounds are transformed into upper bounds, $x \geq x_L \rightarrow -x \leq -x_L$, no bound refers to $x_{r,U} \rightarrow \infty$.

The explicit performance specifications are given as bounds in the same way:

$$f_i \leq f_{U,i}\,,\ i = 1, \ldots, 2n_f \tag{3}$$

On the other hand, there are implicit specifications, which refer to conditions on the transistor channel geometries and transistor operating voltages. These implicit specifications define the constraint region of design parameters X:

$$X = \{\mathbf{x}_d \,|\mathbf{c}(\mathbf{x}_d) \geq \mathbf{0}\} \tag{4}$$

They can be computed for each circuit, e.g., by [2].

3 Sizing Tasks

Figure 1 shows the basic sizing tasks. While nominal design aims at finding design parameter values for optimum performance without considering parameter tolerances, tolerance design does include the tolerance ranges of operational parameters and the distribution of statistical parameters [1].

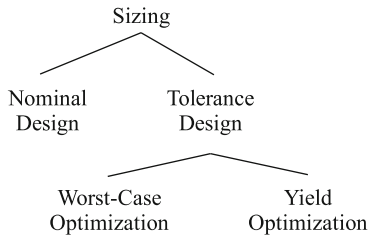

Fig. 1 Sizing tasks

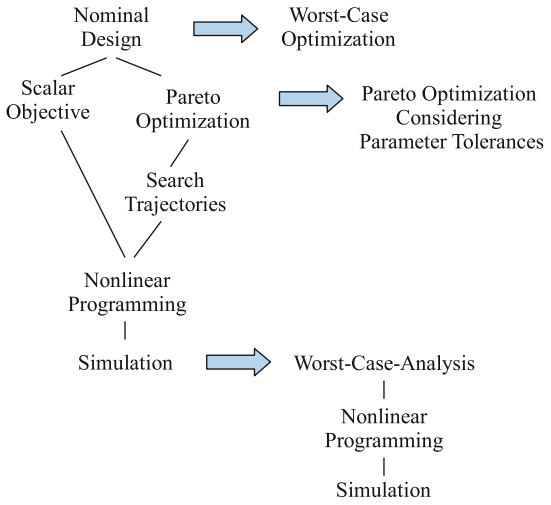

Fig. 2 Nominal design and worst-case optimization

4 Nominal Design

Circuit design inherently is a multiobjective optimization problem:

$$\min_{\mathbf{x}_d \in X} \begin{bmatrix} \vdots \\ f_i(\mathbf{x}_d) \\ \vdots \end{bmatrix} \rightarrow \mathbf{x}_d^*\,,\ f_i^* = f_i(\mathbf{x}_d^*)\,,\ i = 1, \ldots, n_f \tag{5}$$

An optimal design will always represent a certain trade-off between the competing design objectives. Nominal design therefore is either approached by a scalar objective function or by Pareto optimization, as shown in Fig. 2. If Pareto optimization is solved using deterministic methods, then the basic task consists in defining a set of search trajectories for scalar optimization problems, which in turn are solved with nonlinear programming methods like Sequential Quadratic Programming. At the bottom of this task chain, simulation is called frequently, which makes optimization cost between minutes, hours or even days.

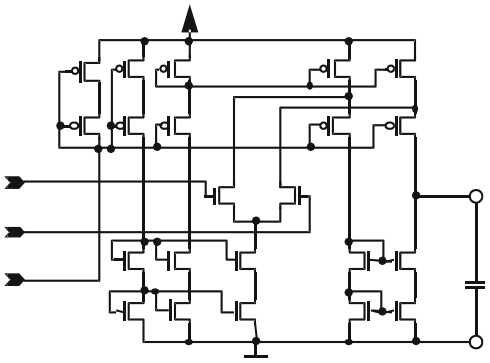

Fig. 3 Example circuit: operational amplifier

Table 1 Nominal design of operational amplifier

Performance	Specification	Initial	Design 1	Design 2
Gain	$\geq$80 dB	67 dB	100 dB	100 dB
Transit frequ.	$\geq$10 MHz	5 MHz	20 MHz	18 MHz
Phase margin	$\geq 60°$	75°	68°	72°
Slew rate	$\geq 10\,\mathrm{V}/\mu\mathrm{s}$	$4.1\,\mathrm{V}/\mu\mathrm{s}$	$12\,\mathrm{V}/\mu\mathrm{s}$	$12\,\mathrm{V}/\mu\mathrm{s}$
DC power	$\leq 50\,\mu W$	$122\,\mu W$	$38\,\mu W$	$39\,\mu W$

4.1 Example

For a simple operational amplifier depicted in Fig. 3, Table 1 shows typical results of a nominal design, in this case obtained with a commercial tool [3]. The circuit has 14 design parameters and five performances given in the first column of Table 1. The CPU time for one simulation is in the range of seconds, the CPU time for the optimization is in the range of minutes.

Column two gives the considered performance features and specifications, column three typical initial values of nominal design. The last two columns give the results of two different optimization runs with different weights among the performance features. We can see that in both cases the specs are fulfilled. While design 1 has a larger safety margin with respect to the transit frequency, design 2 has a larger safety margin with respect to the phase margin. The final decision on the design depends on the application and other aspects like manufacturing variability.

References

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