Substrate Modeling Based on Hierarchical Sparse Circuits

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Abstract In this paper, a new modeling approach appropriate for the substrate modeling is proposed. More generally, this technique can be applied for any homogeneous layer for which an exponential decay of the field variation can be assumed. The main idea is to perform a hierarchical modeling based on an exponential partitioning scheme conducing to a circuit model of linear complexity which is extracted with a low computational effort. The model obtained is further coupled with the models of the other parts in which the integrated circuit is decomposed or its sparse matrix is used as a boundary condition for field in SiO2 domain.

1 Introduction

With the continuous downscaling of CMOS devices analog, RF and digital circuitry are integrated on a single chip. However, due to the conducting nature of the common substrate, noise generated by the digital circuitry can be easily injected into and propagate through the silicon substrate. Accurate and efficient modeling of the electromagnetic effects in the semiconductor substrate is an important still open problem for the EDA community [1, 2].

The IC substrate is a semiconductor body represented by computational domains of rectangular shapes. It is usually structured in homogeneous layers, with constant material parameters. The traces of the circuit devices on the top surface of the substrate are called *connectors* or *contacts*. The bottom surface of the substrate is the *backplane contact*, usually a grounded or a floating metallic layer [3]. The top surface of the computational domain and its lateral surfaces have a virtual character, being conventional cuts in the real semiconductor substrate body. The contacts are

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also conventional surfaces [1, 3]. The number, shapes and sizes of the contacts are very much dependent on the actual circuit layer as well as on the modeling approach. Inhomogeneous, high-conductivity layers and structures such as the epi-layer, wells, diffusion gradients, and buried layers are usually included in the substrate models, but a simpler solution we will consider in our approach is the one in which the modeled substrate contains only the homogeneous Silicon bulk. The top contacts are placed on an orthogonal, regularly structured grid. They can be clustered to match the actual circuit layers.

The substrate models are based on electromagnetic (EM) field modeling. The choice of the most appropriate EM field regime for a particular model of the substrate depends on the values of the material constants and the required operating frequency range. At low frequencies, the substrate behavior is well described by static regimes, the most appropriate model being obtained by using, in conjunction, electrostatics (ES), electric conduction (EC) and magnetostatics (MS), aiming to model capacitive, conductive losses and inductive effects of the integrated circuit.

Numerical studies in [4] show that the electroquasistatic (EQS) assumptions are valid for high-resistivity substrates at frequencies below 20 GHz. In the case of low-resistivity substrates EQS can be used at least for frequencies up to 100 GHz.

Even in the simplest static regimes, the complexity of the extracted model with n connectors is $O(n^2)$, since the number of lumped circuit elements linking the connectors is given by $n(n-1)/2$. For instance, two millions of R, L or C elements are required to model 2,000 connectors in EC, MS or ES regimes. RC "equivalent" circuits are extracted from the EQS field solution. Fortunately, not all these elements have a similar importance in the model, as many of them describe weak interactions. Typical examples are links between far connectors or connectors screened by other connectors. That is why, a hierarchical modeling approach for the substrate is necessary. Several hierarchical approaches are described in [1, 5].

2 Hierarchical Approach

2.1 Main Idea

The substrate modeling approach we propose is valid at frequencies where the EQS regime may be considered valid. In order to also model the magnetic/inductive field effects in the substrate, we consider the EQS field in conjunction with the MS one. Thus, two independent models are extracted, to be connected in the global model of the IC. For this, we use the domain partitioning (DP) technique as described in [6]. The IC devices and the substrate interact by means of EM *hooks* [6]. The hierarchical sparsification we propose is based on an exponential partitioning scheme of the substrate (Fig. 1). Virtual contacts (hooks) are buried in the substrate at different depths (according to their levels), thus realizing a domain-partitioning of the substrate in horizontal layers structured in rectangular

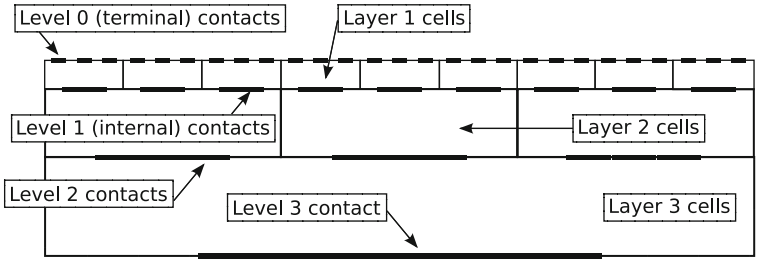


Fig. 1 Partitioning of the substrates in macro-cells

super-elements (macro-cells). The cell-walls thus generate an adapted *discretization macro-grid*, progressively refined from bottom to top. Unlike the literature, in our approach, the equivalent contacts have a physical meaning, being the terminals of the macro-cells in which the domain is partitioned. Thus, sparse hierarchical circuit-models with a reduced number of lumped elements are generated.

2.2 Theoretical Basis

The main reason which makes our hierarchical modeling approach valid is the exponential decay of the field variation on deeper horizontal planes. For instance, in EC, ES and MS field regimes, the scalar potential satisfies in homogeneous media the Laplace equation $\Delta V = 0$.

For the sake of simplicity, let's consider a 2D domain $\mathscr{D} = [0, a] \times [0, b]$, which represents the homogeneous substrate we want to model, with $V(x, 0) = 0$ for $x \in [0, a]$, $\partial V/\partial x(0, y) = 0$ and $\partial V/\partial x(a, y) = 0$ for $y \in [0, b]$. The top segment, corresponding to $y = b$ and $x \in [0, a]$ ensures the link with the upper part, so that a certain non-zero Dirichlet boundary condition has to be imposed for it: $V(x, b) = f(x)$ for $x \in [0, a]$. This problem can be solved analytically, the solution obtained after imposing three out of the four boundary conditions being:

$$V(x, y) = C_0 y + \sum_{i=1}^{\infty} C_i \cos(\lambda_i x) \sinh(\lambda_i y), \tag{1}$$

where $\lambda_i = \pi i/a$.

The constants C_i in (1) can be obtained by imposing the Dirichlet condition on the top horizontal segment $y = b$.

$$C_0 b = F_0/2 = \frac{1}{a} \int_0^a f(x)\, \mathrm{d}x,$$

$$C_i \sinh(\lambda_i b) = F_i = \frac{2}{a} \int_0^a f(x) \cos(\lambda_i x)\, \mathrm{d}x. \tag{2}$$

The values of the potential on the top segment depend on the device placed on the substrate. However, any possible variation can be approximated accurately as a piecewise linear function, which tends to the real variation when the fineness of the discretization tends to infinity. Such a function can be expressed as a linear combination of "hat functions". If N is the number of contacts (terminals) equidistantly placed on the top side and m is the index of the contact that is excited with a $V_0 = 1$ V potential, then the Fourier coefficients given by (2) are

$$F_0 = 2V_0/(N-1),$$
$$F_i = \frac{2V_0(N-1)}{\pi^2 i^2}\left[2\cos\frac{\pi i(m-1)}{N-1} - \cos\frac{\pi i(m-2)}{N-1} - \cos\frac{\pi i m}{N-1}\right]. \quad (3)$$

Finally, the coefficients in (1) are $C_0 = V_0/b(N-1)$ and $C_i = F_i/\sinh(\lambda_i b)$ where F_i is given by (3).

The Fourier series can be truncated, but, according to [7], in order to keep a minimal accuracy on the top segment (given by $y = b$ and also called "level 0"), the number of retained terms (spatial harmonics along the Ox direction) should be at least twice the total number of contacts in that direction: $n_0 = 2N$. The error due to the truncation of the series (1) at the M-th term is

$$\begin{aligned}
|V_M(x,y) - V(x,y| &\le \sum_{i=M+1}^{\infty} |C_i| \sinh(\lambda_i y) \\
&\le \frac{8V_0(N-1)}{\pi^2} \sum_{i=M+1}^{\infty} \frac{\sinh(\lambda_i y)}{i^2 \sinh(\lambda_i b)} \le A\int_M^{\infty} \frac{\sinh(\pi x y/a)}{x^2 \sinh(\pi x b/a)}\,\mathrm{d}x \\
&\approx A\int_M^{\infty} \frac{\exp(\pi(y-b)x/a)}{x^2}\,\mathrm{d}x \\
&= A\left(\frac{\exp(\pi(y-b)M/a)}{M} + \frac{\pi(y-b)}{a}E_1(M)\right) \\
&\le A\left(\frac{\exp(\pi(y-b)M/a)}{M} + \frac{\pi(y-b)}{a}e^{-M}\log(1+\frac{1}{M})\right), \quad (4)
\end{aligned}$$

where $A = 8V_0(N-1)/\pi^2$ and $E_1(M) = \int_M^{\infty} \exp(-t)/t\,\mathrm{d}t$ is the exponential integral and its margins are well known [8].

It is obvious from Fig. 2 that on deeper levels $y_k < b$, for the same accuracy, only a lower number of terms need to be retained from the Fourier series given by (1). For instance, if we would like that level 1 be accurately described by $N_1 = N/3$ contacts, the number of terms that have to be summed is $n_1 = 2N/3$. By imposing

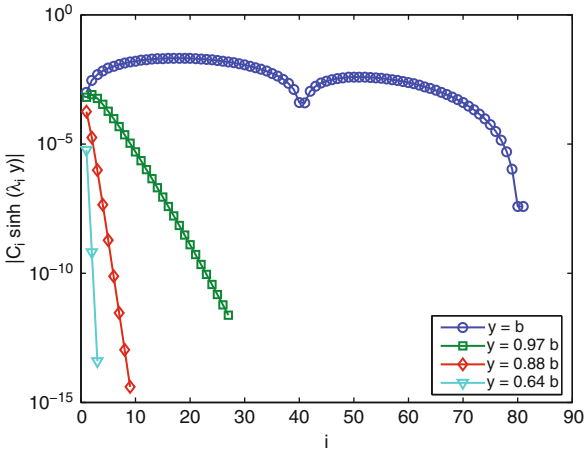


Fig. 2 Fourier coefficients for several depths

the condition that the first neglected term at level 1 be equal to the first neglected term at level 0, it follows that level 1 has to be placed as given by

$$y_1 \leq b - \frac{a}{\pi(2N/3+1)} \log \frac{|F_{2N/3+1}|}{|F_{2N+1}|}. \tag{5}$$

For the example above, it follows that $y_1 \leq 0.97b$. This kind of restriction gives a guidance about how deep a reduced number of contacts can be buried while keeping the modeling accuracy. By applying this procedure recursively, the substrate is partitioned in layers having an exponentially decreasing number of contacts. To simplify the presentation, we will assume that N is a power of 3, $N = 3^L$. Thus, in order to decrease the number of degrees of freedom (dofs) by 3 for each level, we will need $L + 1$ levels, a level j having $N_j = 3^{L-j}$ contacts. A layer j is placed between level j and level $j - 1$ (for $j = 1, \ldots, L$) and it will have a certain thickness Δy_j. We will place the layers according to a geometric progression of ratio $r > 1$: $\Delta y_2 = r\Delta y_1$, $\Delta y_3 = r^2\Delta y_1, \ldots, \Delta y_L = r^{L-1}\Delta y_1$. It follows that $\Delta y_1(r^L - 1)/(r - 1) = b$. If we chose $r = N_0/N_1 = 3$, the first level has a thickness of $\Delta y_1 = 2b/(3^L - 1)$ and its corresponding position $y_1 = b - \Delta y_1$ satisfies relation (5) only if the number of layers L is less than 4. In this case the cells that are used to discretize the substrate will have the same input-output behavior. Thus, only one cell, called *reference cell* has to be solved in order to find its input-output relationship and thus an equivalent circuit for it (Fig. 3).

Going down in the substrate, the number of dofs necessary to describe the solution decreases exponentially (level j has 3^{L-j} dofs). A lower number of dofs means a lower number of hooks (contacts) on deeper layers. Hence, the grid necessary to describe the field may be coarser, deeper in substrate. This is the main conclusion of the above study. Going down, the field distribution is smother and requires a lower number of spatial harmonics (samples) to be represented accurately.

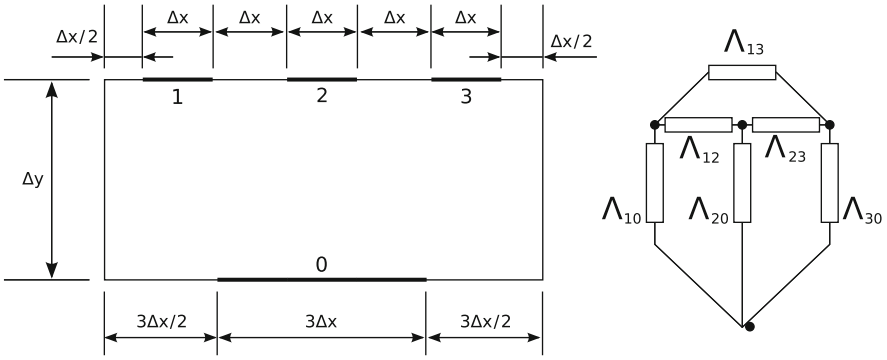


Fig. 3 Layout of a standard cell and its equivalent circuit

Even if the above explanations were given for the 2D case, they can be generalized without difficulty for the 3D case.

It is easy to show that the complexity of the equivalent circuit increases linearly. In 2D, a standard cell will have four terminals, three on the top segment and one on the bottom. The number of layers is $L = \ln(N)/\ln(3)$, the total number of cells is $(3^L - 1)/2$, and the number of branches of the equivalent circuit is $O(3(N-1)) = O(N)$. A model with 13 layers can handle about 1.6 million top-connectors, using almost 4.8 million lumped elements. In 3D, a standard cell will have ten terminals, nine on the top face and one on bottom, the number of layers is $L = \ln(N)/\ln(9)$, the total number of cells is $(9^L - 1)/8$, and the complexity of the equivalent circuit is $O(45(N-1)/8) = O(N)$. A model with seven layers can handle about 4.8 million top-connectors, about 600,000 cells and, consequently, using about twenty seven millions lumped elements, each cell having 45 lumped elements. The linear order of the extracted model is another great advantage of this approach.

2.3 Algorithm

The algorithm we propose has the following steps:

Step 1: Chose appropriate EMCE formulation for the upper part and simulate it. This implies the setting of the appropriate shape and position of terminals on the boundary part that will be connected to the substrate. This setting depends on the actual configuration of the device.

Step 2: Compute the number N of equidistant terminals necessary for the level 0 of the substrate. This depends on the minimum discretization step used at step 1.

Step 3: Compute the number of necessary layers in the substrate L and their heights.

Step 4: Simulate the reference cell (2D case shown in Fig. 3 left), and compute the geometric permeances (Fig. 3 right).

In this step, by solving the reference cell (e.g. with a BEM or FIT solver), the nodal permeances matrix is obtained. In 2D this matrix has 3×3 entries, but due to reciprocity and geometric symmetry, only four values are different:

$$\Lambda^{(n)}_{\text{ref.cell}} = \begin{bmatrix} \Lambda^{(n)}_{11} & \Lambda^{(n)}_{12} & \Lambda^{(n)}_{13} \\ \Lambda^{(n)}_{12} & \Lambda^{(n)}_{22} & \Lambda^{(n)}_{12} \\ \Lambda^{(n)}_{13} & \Lambda^{(n)}_{12} & \Lambda^{(n)}_{11} \end{bmatrix}. \tag{6}$$

These values are dimensionless and depend solely on the cell and contact sizes. The values of the permeances of the lumped elements are:

$$\begin{aligned} \Lambda_{12} &= -\Lambda^{(n)}_{12}, \quad \Lambda_{10} = \Lambda^{(n)}_{11} + \Lambda^{(n)}_{12} + \Lambda^{(n)}_{13}, \\ \Lambda_{13} &= -\Lambda^{(n)}_{13}, \quad \Lambda_{20} = \Lambda^{(n)}_{22} + 2\Lambda^{(n)}_{12}. \end{aligned} \tag{7}$$

Step 5: Assemble the nodal permeances matrix for the hierarchical sparsified circuit that models the substrate.

In this step, the nodal permeance matrix $\Lambda^{(n)}_{HSS}$ for the whole hierarchical circuit (Fig. 4) is derived. This is a sparse, symmetric matrix, having four non-zero elements on each row (Fig. 5). Its pattern depends on the node numbering. For instance, if the numbering is carried out from left to right and from bottom to top, the last N lines and columns correspond to the terminals. It is useful to partition the nodal permeance matrix of the HSS circuit according to this numbering as:

$$\Lambda^{n}_{HSS} = \begin{bmatrix} \Lambda^{n}_{HSS,11} & \Lambda^{n}_{HSS,12} \\ \Lambda^{n}_{HSS,21} & \Lambda^{n}_{HSS,22} \end{bmatrix} \tag{8}$$

Step 6: Compute the terminal admittance matrix of the top level with (9).

By eliminating the internal nodes of the model, the terminal permeance matrix Λ_T of the sparsified model can be obtained:

$$\Lambda_T = \Lambda^{n}_{HSS,11} - \Lambda^{n}_{HSS,12} \left(\Lambda^{n}_{HSS,22}\right)^{-1} \Lambda^{n}_{HSS,21}. \tag{9}$$

Algebraically, this means the computation of the Schur complement of the lower right block. The terminal admittance matrix is $\mathbf{Y}_{HSS} = (\sigma + j\omega\varepsilon)\Lambda_T$, where σ and ε are the conductivity and the permeability of the substrate. The same geometric permeances are used to compute the magnetic reluctances and, based on them, the fundamental loop inductances of the circuit placed above the substrate can be extracted.

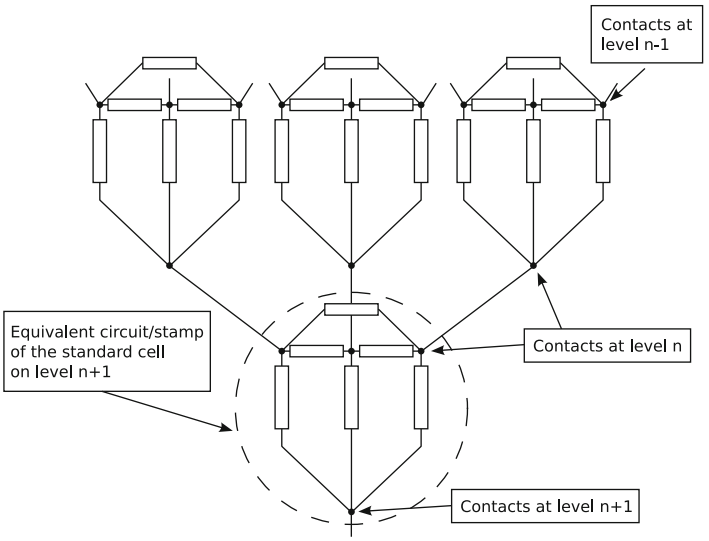
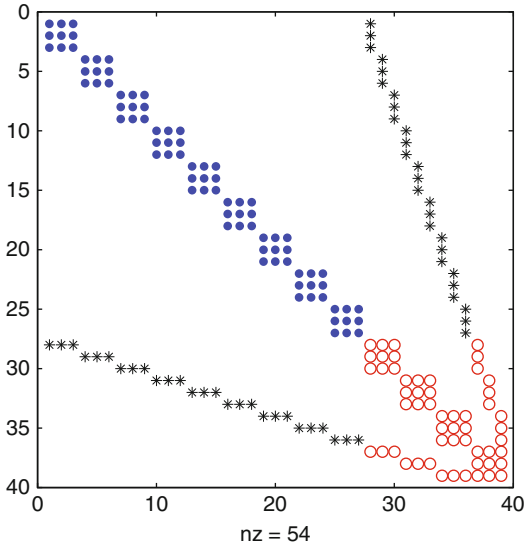


Fig. 4 Hierarchical sparse circuit of the substrate

Fig. 5 Structure of the nodal matrix Λ_{HSS}^{n}



Step 7: Clusterise the terminals of the substrate according to the terminals of the upper part.

Step 8: Couple the models with relation (10).

In the last step, the models are coupled by means of their contacts. Assuming that the top model has the terminals numbered so that the hooks that are connected

to the substrate are numbered at the end, its transfer matrix is partitioned as $\mathbf{Y}_{\text{top}} = [\mathbf{Y}_{11}\mathbf{Y}_{12}; \mathbf{Y}_{21}\mathbf{Y}_{22}]$ then, by imposing the coupling conditions, the admittance matrix of the whole model is

$$\mathbf{Y} = \mathbf{Y}_{11} - \mathbf{Y}_{12} \left(\mathbf{Y}_{HSS} + \mathbf{Y}_{22}\right)^{-1} \mathbf{Y}_{21}. \tag{10}$$

3 Results and Conclusions

In order to verify the proposed approach, a simple study case of a micro-strip dual conductor line in SiO2 over a lossy Si substrate was considered. The line admittance was computed by FIT, using DP with conform grids (Fig. 6) and with the hierarchical modeling for the substrate. The result shown in Fig. 7 validates the latter approach. The substrate was decomposed into five layers having progressive increasing thicknesses with a constant rate. The CPU time needed to extract the admittance matrix by hierarchical sparsification was 0.093 s, whereas the same time when using DP with conform grids was 20 s. This illustrates the important reduction of the extraction time. The proposed approach allows a fast extraction of parasitic GLC parameters in complex integrated circuits with over a million of components, modeling the EM coupling and noise propagation.

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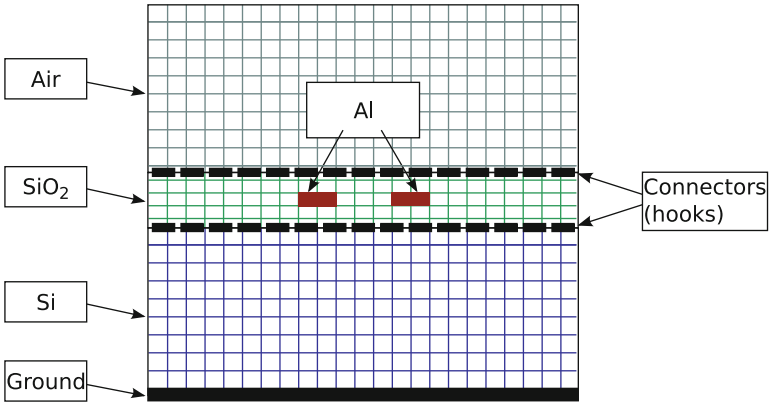

Fig. 6 Computational domain partitioned in three parts. Conform grids are shown

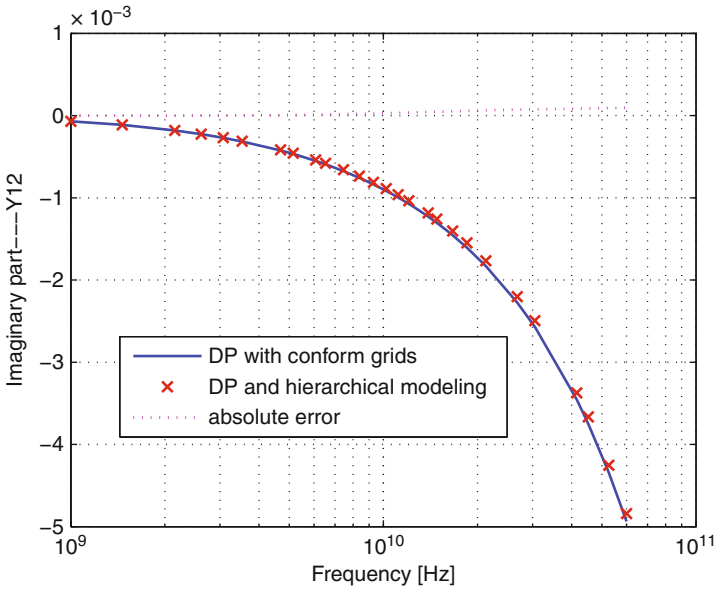

Fig. 7 Hierarchical approach is as accurate as DP with conform grids

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