Two Novel Long-Tail Pair Based Second Generation Current Conveyors (CCII)

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Abstract. Two novel long tail pair based CCII are proposed in this paper. The first OTA CCII offer 1.98GHZ current transfer bandwidth and 10MHZ voltage transfer bandwidth. The second proposed design of CCII is independent against bias current variation. The second proposed design offer voltage transfer bandwidth of 10MHZ and current transfer bandwidth of 1.2GHZ with a very accurate voltage and current copy at corresponding x and Z nodes. The none idealities of first CCII are also measured using Spice simulation with TSMC 180nm model parameters.

Keywords: OTA CCII, Voltage transfer bandwidth, Current transfer bandwidth.

1 Introduction

The current-mode approach considers the information flowing on time-varying currents. Current-mode techniques are characterized by signals as typically processed in the current domain. The current-mode approach is also powerful if we consider that all the analog IC functions, which are traditionally designed in the voltage-mode, can also be implemented in current-mode. In voltage mode circuits, the main building block used to add subtract, amplify, attenuate, and filter voltage signals is the operational amplifier. A current-mode approach is not just restricted to current processing, but also offers certain important advantages when interfaced to voltage-mode circuits. Since the introduction of conveyors in early 70's, lot of research has been carried out to prove usefulness of this CCII. The CCII is a functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block. Internal architecture of CCII is voltage follower cascaded with current follower as shown in figure:1.

2 OTA CCII

The simple current Mirror based CCII can be improved by replacing Simple diode connected level shifter in a flipped voltage follower based simple current mirror CCII

V.V. Das, G. Thomas, and F. Lumban Gaol (Eds.): AIM 2011, CCIS 147, pp. 95–99, 2011.

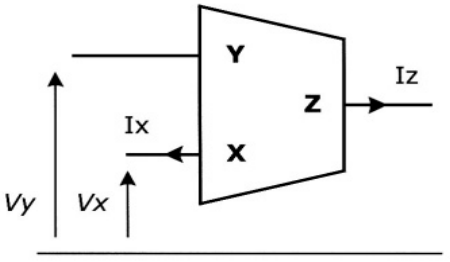

Fig. 1. CCII Block Representation

proposed by A.J.Lopez martin etal by OTA level shifter. The resulting circuit is depicted in figure:2. The proposed circuit is a combination of a OTA and FVF cell.In the proposed circuit(fig:2), transistors M1 to M4 form differential pair. Transistor M7 and M8 forms Flipped voltage follower. The X terminal voltage is connected to the gate of M2 transistor which is controlled by source voltage of M7.So,transistor M1-M4 and from terminal a through M7 forms a level shifter, the voltages at X and Y terminals follow each other. The drain voltage of M7 is also used to control M8 and M11 transistors. So, the current flowing at X terminal is conveyed to Z terminal via M8.Here M7 and M8 ensure low resistance at X node. While Y input is at gate of M1 which gives very high input impedance at Y input. The circuits of proposed CCII in figure 2 was simulated using 0.18 µm CMOS technology with NMOS and PMOS threshold voltages of approximately 0.4 V and -0.39v. The Transistor aspect ratios are shown in Table 1. Bias voltage was +/-1 V, and bias current IB was 70 µA**.** First, its time response was evaluated by configuring the the circuit as unity-gain voltage amplifiers. In order to do so, ports X and *Z* were loaded with 15 kΩ resistances. The input voltage, a 100KHZ**,** 100 mVpp, sinusoid. was applied to the Y port Figure2 and the result is tabulated in Table:2 The AC small-signal frequency response for the circuit is subsequently obtained, using the same load resistors. The simple structure of Figure 2 has a unity bandwidth of 100 MHz,as expected. Table 2 also compares simulation results of the proposed circuit with low-voltage current conveyor reported in the literature[6]. The advantages in terms of power dissipation ,offset and compactness at reduced circuit complexity can be clearly evidenced.

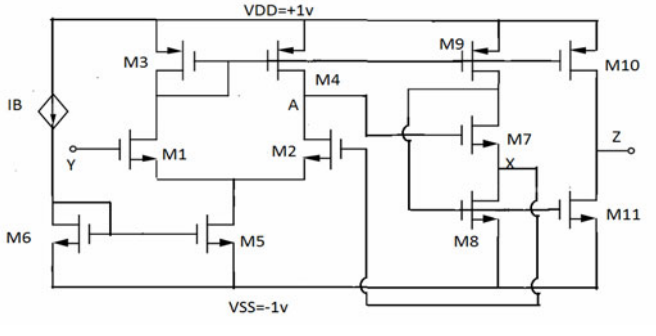

Fig. 2. OTA CCII based on differential pair

Table 1. Aspect Ratio for Fig:2

Transistor	W/L
M1,M2,M7	30u/.9u
M3,M4,M9,M10	15u/.9u
M5,M6,M8,M10	13.5u/2.7u

The small signal terminal impedances at X,Y and Z node is as follows.

$$Zx = ro8 \| \left[\left(\frac{ro7}{1+gm7ro7} \right) + ro9 \right], Zy = \gamma * W * L * cox, Rz = ro10 \| ro11,$$

The small signal ratios Vx/Vy and Iz/Ix is given as follows. The non-idealities of CCII shown in figure is measured using TSMC 180nm model parameters using spice simulation. The non ideal matrix is shown below.

$$\frac{Vx}{Vy} = \frac{r07\,gm7(ro/2)gm1}{1+ro7\,gm7(1+(ro/2)gm2)}, \frac{Iz}{Ix} = \frac{(gm11*ro11*r08)}{(ro11+ro10)(1+gm8ro8)}$$

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0.33\text{x}10^{-7} & 0 & 0.195\text{x}10^{-3} \\ 1 & 1.8\text{k} & 0.310 \\ 0.09 & \pm 1 & 0.005\text{x}10^{-3} \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix}$$

3 Cascode OTA and FVF Based CCII

The problem with the above CCII is the output offset is a function of I_b, technology parameters and input voltage. The mathematically it is given by,

Table 2. Simulation Results For OTA CCII

Characteristic Parameters	Proposed FV mirror based Arch-1	A.J.L.Martin etal
Voltage Supply	+/1V	1.5V
Power Cons.	0.58mwatt	0.75mwatt
Iz/Ix transfer BW	1.98Ghz	20Mhz
Vx/Vy transfer Bw	10Mhz	100Mhz
IBIAS	90uA	100uA
Offset	-23.72mv	300mv
Iz / Ix	1	1.1
Vx / Vy	1	1
Y Para. Imp.	6GΩ	80k
X Para. imp	1.4kΩ	10KΩ
Z Para. imp.	300kΩ	11KΩ
THD	1.21% @ 100Mhz	1%

$V_{offset} = \sqrt{\frac{2I_b}{\beta}}\left[V_{DS1} - V_{DS2}\right]$ The variation with I_b is plotted infigure:3 shows that the offset varies with biasing current Ib. From figure it is clear that as biasing current increases from 10mA to 170mA the output offset varies from -400mv to 0v.The circuit can be made independent from biasing current by adding one more pair of pMOS current mirror load on the top of the pMOS current mirror load in OTA based CCII in figure:2.The resulting CCII is shown figure:4 .

Table 3. Simulation Results For Cascoded OTA CCII

Characteristic Parameters	Proposed FV mirror based Arch-1	Cascoded OTA CCII	A.J.L.Martin etal
Voltage Supply	+/1V	+/-1.25V	1.5V
Power Cons.	0.354mwatt	0.9mV	0.75mwatt
current transfer bandwidth	2Ghz	1.2Ghz	100Mhz
IBIAS	70uA	60uA	100uA
offset	Function of Ibias	Independent of Ibias	300mv
Iz / Ix	1	1	1.1
Vx / Vy	1	1	1

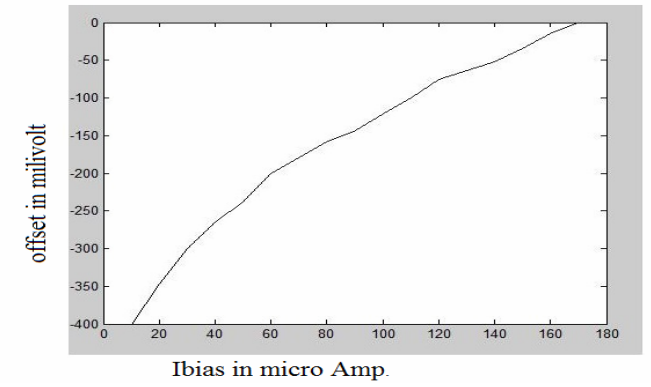

Fig. 3. Plot of biasing current dependency on output offset of OTA CCII in figure:2

5 Conclusion

Two novel CCII topologies are proposed simulated and compared with the present state of art design. The topologies are very compact, low power and wideband. The

second topology is a high precision with zero offset and independent of biasing current. The results are tabulated in Table-2 and 3.

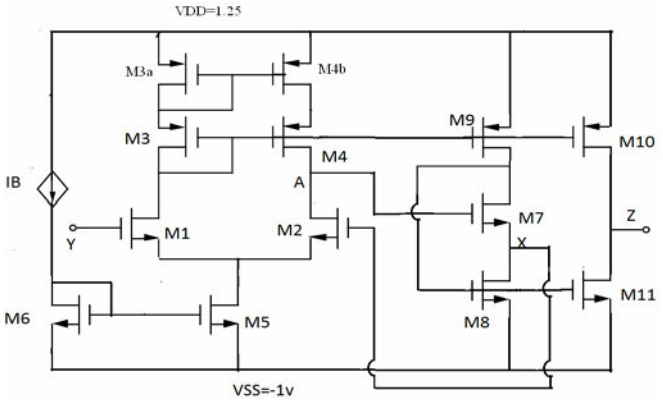

Fig. 4. OTA CCII based on differential pair

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