A Novel Design of Reconfigurable Architecture for Multistandard Communication System

T. Suresh[1] and K.L. Shunmuganathan[2]

[1] Research Scholar, R.M.K Engineering College,
Anna University, Chennai, India
fiosuresh@yahoo.co.in
[2] Professor & Head, Department of CSE, R.M.K Engineering College,
Anna University, Chennai, India
kls_nathan@yahoo.com

Abstract. The goal of future mobile communication systems will be to incorporate and integrate different wireless access technologies and mobile network architectures in a complementary manner so as to achieve a seamless wireless access infrastructure. To support this seamless user mobility across different wireless access technologies it is needed to design reconfigurable multistandard receiver architecture. This paper presents the system-level design of a wireless receiver's baseband architecture, which supports two wireless access technologies: Wideband Code Division Multiple Access (WCDMA) and Orthogonal Frequency Division Multiplexing (OFDM). In this paper, efficient method of Fast Fourier Transform (FFT) algorithm for OFDM standard and Rake Receiver design for WCDMA standard were implemented. This architecture efficiently shares the resources needed for these two standards while reconfiguring. The proposed architecture is simulated using ModelSimSE v6.5 and mapped onto a Spartan 3E FPGA device (3s5000epq208) using the tool Xilinx ISE 9.2. Simulation results show that the proposed architecture can be efficiently reconfigured in run-time and proved as area efficient.

Keywords: FPGA, WCDMA, OFDM, FFT/IFFT, Rake Receiver, Reconfigurable.

1 Introduction

The need to support several standards in the same handheld device, associated with the power consumption and area restrictions, created the necessity to develop a portable, power efficient, integrated solution [1]. Users carrying an integrated open terminal can use a wide range of applications provided by multiple wireless networks, and access to various air interface standards. The continuous evolution of wireless networks and the emerging variety of different heterogeneous, wireless network platforms with different properties require integration into a single platform [2]. This has lead to an increased interest in the design of reconfigurable architecture. The idea of the reconfigurable architecture is that it should be possible to alter the functionality of a mobile device at run-time by simply reusing the same hardware for different

V.V. Das, G. Thomas, and F. Lumban Gaol (Eds.): AIM 2011, CCIS 147, pp. 87–94, 2011.
© Springer-Verlag Berlin Heidelberg 2011

wireless technologies and ultimately for users to connect to any system that happens to be available at any given time and place.

2 Reconfigurable Architecture

Multistandard wireless communication applications demand high computing power [3], flexibility, and scalability. An Application-Specific Integrated Circuit (ASIC) solution would meet the high computing power requirement, but is inflexible [4] and the long design cycle of ASICs makes them unsuitable for prototyping. On the other hand, general purpose microprocessors or Digital Signal Processing (DSP) chips are flexible, but often fail to provide sufficient computing power. Field Programmable Gate Arrays (FPGAs) [5] signal processing platforms are now widely being accepted in base_station designs. However, low power and form factor requirements have prevented their use in handsets. Reconfigurable hardware for Digital Base-Band (DBB) [6] processing is rapidly gaining acceptance in multi-mode handheld devices that support multiple standards. In Reconfigurable Hardware tasks that are required initially can be configured in the beginning. When another task is required, the configuration to load it can then be triggered. In this paper we present the design methodology for reconfigurable baseband signal processor architecture that supports WCDMA and OFDM wireless LAN standards.

During recent years, a number of research efforts focused on the design of new reconfigurable architectures. In [7] the flexibility of the MONTIUM architecture was verified by implementing HiperLAN/2 receiver as well as a Bluetooth receiver on the same architecture. In [8], a broadband mobile transceiver and a hardware architecture which can be configured to any cyclic-prefix(CP) based system reconfigurable architecture for multicarrier based CDMA systems is proposed. Reconfigurable Modem (RM) Architecture targeting 3G multi-standard wireless communication system was proposed in [3]. This architecture targeted two 3G wireless standards WCDMA and CDMA 2000 and the design objectives are scalability, low power dissipation and low circuit complexity. It is seen that though different functions can be reconfigured on a reconfigurable hardware, the major challenge is to have an efficient system configuration and management function which will initiate and control the reconfiguration as per the different application requirements.

3 Reconfigurable Receiver Architecture

Figure 1 shows the Block Diagram of Reconfigurable Receiver System. This Receiver System is able to reconfigure itself to the WCDMA or OFDM Wireless LAN (WLAN) standard. The Proposed architecture comprises functional blocks, which is in the form of reusable, reconfigurable [9-12] functional blocks for use in implementing different algorithms necessary for OFDM and WCDMA standards. One or more reusable functional blocks as given in Fig. 1, can be configured to implement a process including multiplication, addition, subtraction and accumulation. By accommodating the above mentioned capabilities, the architecture should be configured to support WCDMA and WLAN OFDM Standards. For example Fast Fourier Transform (FFT) (basic butterfly function) for WLAN OFDM and Rake.

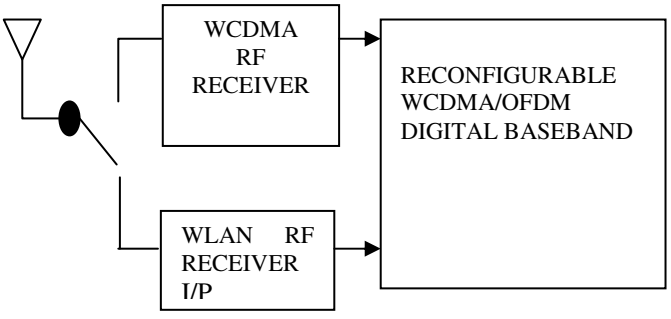

Fig. 1. Block Diagram of Reconfigurable Receiver System

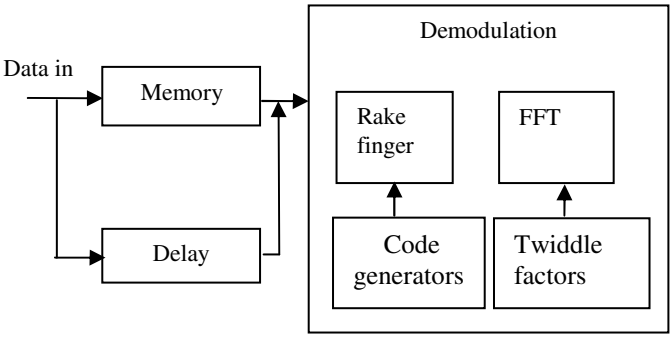

Fig. 2. Block Diagram of Reconfigurable Receiver Architecture

Receiver algorithms (multiply and accumulate select function) for WCDMA are implemented in the architecture as shown in Fig.2. This architecture allows for transformation of the chip from WCDMA chip to WLAN Wi-Fi chip on-demand wherein new algorithms can be accommodated on-chip in real time via different control sets.

3.1 Rake Finger Implementation

In WCDMA receivers, the demodulation is performed in the Rake fingers by correlating the received signal with a spreading code over a period corresponding to the spreading factor. The output of the i^{th} Rake finger can be expressed as

$$O_i(n) = \sum_{i=0}^{L_{sf}-1} C_s\left(i + nL_{sf}\right)R\left(i + nL_{sf}\right). \quad (1)$$

where C_s is the combined spreading and scrambling code and R is the received signal and both are complex numbers [3]. Since the scrambling and spreading codes are always of +/-1, the multiplication and addition of each correlation stage are simplified. So the equation(1) is simplified to

$$(R_r+jR_i)(C_{sr}-jC_{si}) = (R_rC_{sr}+ R_iC_{si})+j(R_iC_{sr}- R_rC_{si}) . \quad (2)$$

If the value +1 is represented as logic '0' and the value -1 is represented as logic '1', the equation (4) is simplified as follows

$$= \begin{cases} R_r+R_i+j(R_i-R_r), \text{ when } C_{sr}=0, C_{si}=0 \\ R_r-R_i+j(R_i+R_r), \text{ when } C_{sr}=0, C_{si}=1 \\ -(R_r-R_i)-j(R_i-R_r), \text{ when } C_{sr}=1, C_{si}=0 \\ -(R_r+R_i)-j(R_i-R_r), \text{ when } C_{sr}=1, C_{si}=1 \end{cases} \quad (3)$$

Since the code input is binary valued, the complex multiplication in the correlations is simplified to one real addition/subtraction and one imaginary addition/subtraction. Selection of addition or subtraction is done with the help of multiplexer. So the total resources required to implement Rake Receiver using (3) are two adders, two subtractors and one multiplexer.

3.2 FFT Implementation

In OFDM, the demodulation is performed by applying 64-point FFT. The twiddle factor is calculated and put in a table in order to make the computation easier and can run simultaneously. The Twiddle Factor table is depending on the number of points used. During the computation of FFT, this factor does not need to be recalculated since it can refer to the Twiddle factor table, and thus it saves time. Figure 3 shows the 2 point Butterfly structure [13] where multiplication is performed with the twiddle factor after subtraction.

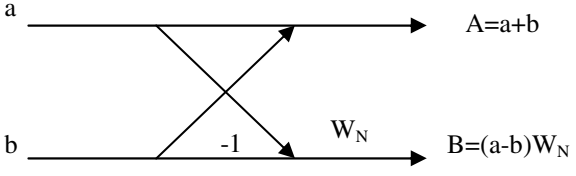

Fig. 3. 2 Point Butterfly Structure

Multiplication is certainly the most vital operation in Communication processing, and its implementation in an integrated circuit component requires large hardware resources and significantly affects the size, performance, and power consumption of a system [14]. So an efficient way of multiplier reduction in FFT processing is done as follows. Consider the problem of computing the product of two complex numbers R and W

$$X = RW = (R_r+jR_i)(W_r+jW_i)$$
$$= (R_rW_r-R_iW_i)+j(R_rW_i+R_iW_r) \quad (4)$$

From equation (4), the direct architectural implementation requires total of four multiplications and one real subtraction and one imaginary addition to compute the complex product. However, by applying the Strength Reduction Transformation we can reformulate equation (4) as:

$$X_r=(R_r-R_i)Wi+R_r(W_r-W_i) \quad (5a)$$

$$X_i=(R_r-R_i)W_i+R_i(W_r+W_i) \quad (5b)$$

As can be seen from Equations (5a) and (5b), by using the Strength Reduction Transformation the total number of real multiplications is reduced to only three. This however is at the expense of having two additional subtractors and one adder.

4 Processing Element

Figure 4 shows the Processing Element(PE) and its resources required for the implementation of FFT in WLAN OFDM and figure 5 shows the Processing Element(PE) and its resources required for the implementation of Rake finger in WCDMA. It is shown that the two adders and subtractors(red coloured) are shared by both the standards. So the proposed Reconfigurable Architecture consists of processing units ,their computational elements are shared by both the Rake Receiver operation of WCDMA and FFT operation of OFDM. The processing units perform the multiply-accumulate operation in the Rake mode as described in section 3.1 and butterfly operations in the FFT mode as described in section 3.2. The computational resources required by the proposed architecture are 5 adders, 4 subtractors, 3 multipliers and multiplexers.

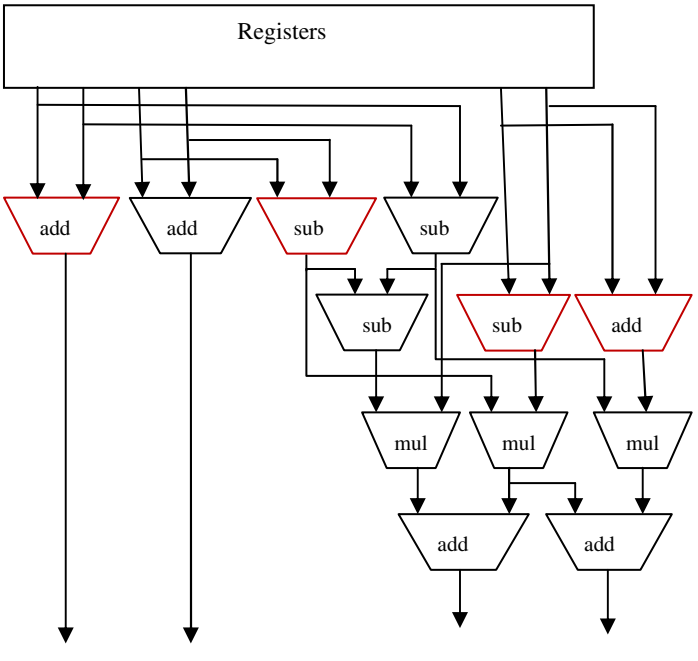

Fig. 4. PE and its Resources of WLAN OFDM

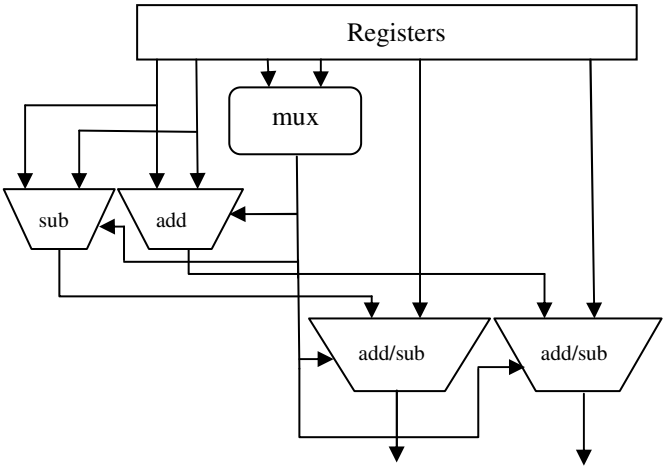

Fig. 5. PE and its Resources of WCDMA

5 Results and Discussion

The proposed reconfigurable architecture described in section 3 and 4 were simulated using ModelSimSE v6.5 and mapped onto a Spartan 3E FPGA device (3s5000epq208) with speed grade (-5) using the tool Xilinx ISE 9.2 and synthesized. The proposed Reconfigurable Architecture with Resource sharing is compared with Reconfigurable Architecture without Resource sharing. Table 1 and Figure 6 show the Resources utilized by the proposed Architecture(Reconfigurable Architecture with Resource sharing) and the Reconfigurable Architecture without Resource sharing. From the results presented above it seems that there is a significant reduction in large number of computational resources which forms the proposed architecture which is more efficient than the conventional Architecture in terms of area.

Table 1. Resource utilization of Reconfigurable Architecture without and with Resource sharing

Resources Utilized	Reconfigurable Architecture without Resource Sharing	Reconfigurable Architecture with Resource Sharing
Number of Slices	1172 out of 4656 (25%)	1070 out of 4656 (23%)
Number of 4 input LUTs	2195 out of 9312 (23%)	2048 out of 9312 (22%)
Number of IOBs	140 out of 158 (88%)	140 out of 158 (88%)

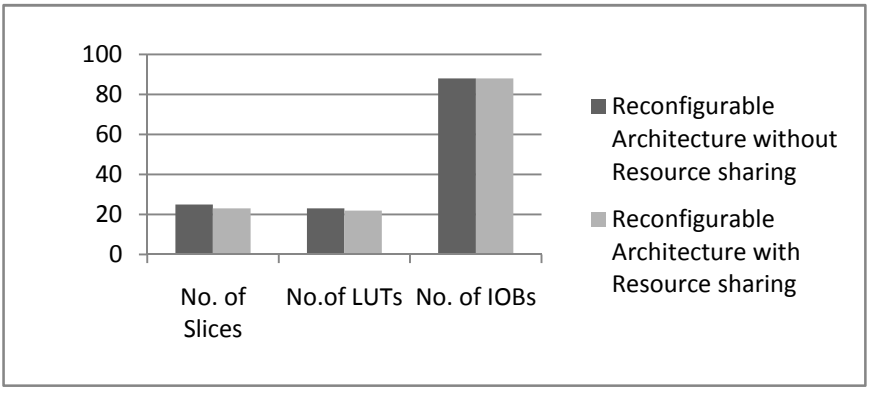

Fig. 6. Comparison of the percentage of resources utilized by Reconfigurable Architecture without Resource Sharing and with Resource Sharing

6 Conclusion

An architecture which can reconfigure itself to wireless LAN OFDM and WCDMA standards, was presented in this paper. While configuring these two standards, it was also presented to implement FFT operation for OFDM and Rake Receiver functioning for WCDMA efficiently. To lower the number of multipliers in FFT and eliminate the multipliers in Rake Receiver, we adopted Strength Reduction Transformation technique and multiplier-less technique. The proposed architecture was simulated using ModelSimSE v6.5 and mapped onto a Xilinx Spartan 3E FPGA device and synthesis report was generated. Simulation results demonstrated that the proposed architecture can reduce hardware overhead, enhance circuit efficiency and significantly reduce area. Moreover, the proposed architecture can be improved to reconfigure to various other advanced wireless standards.

References

1. Atallah, J.G., Ismail, M.: Future 4G front-ends enabling smooth vertical handover. IEEE Circuits and Devices Magazine XXII, 6–15 (2006)
2. Liljana Gavrilovska, M., Vladimir Atanasovski, M.: Interoperability in Future Wireless Communications systems: A Roadmap to 4G. Microwave Review, 19–28 (2007)
3. Lee, J.-S., Ha, D.S.: FleXilicon: a Reconfigurable Architecture for Multimedia and Wireless Communications. In: IEEE International Symposium on Circuits and Systems, pp. 4375–4378 (2006)
4. Kim, J., Ha, D.S.: A New Reconfigurable Modem Architecture for 3G Multi-Standard Wireless Communication Systems. In: IEEE International Symposium on Circuits and Systems, pp. 1051–1054 (2005)
5. David, R., Chillet, D., Pillement, S., Sentieys, O.: A compilation framework for a dynamically reconfigurable architecture. In: Glesner, M., Zipf, P., Renovell, M. (eds.) FPL 2002. LNCS, vol. 2438, pp. 153–194. Springer, Heidelberg (2002)

6. Harju, L., Nurmi, J.: A Programmable Baseband Receiver Platform for WCDMA/OFDM Mobile Terminals. In: IEEE Wireless Communications and Networking Conference, USA, pp. 33–38 (2005)
7. Rauwerda, G.K., Smit, G.J.M., van Hoesel, L.F.W., Heysters, P.M.: Mapping Wireless Communication Algorithms to a Reconfigurable Architecture. The Journal of Supercomputing 30, 263–282 (2004)
8. Liang, Y.-C., Naveen, S., Pilakkat, S.K., Marath, A.K.: Reconfigurable Signal Processing and Hardware Architecture for Broadband Wireless Communications. EURASIP Journal on Wireless Communications and Networking 3, 323–332 (2005)
9. Hauck, S., Fry, T.W., Hosler, M.M., Ko, J.P.: The Chimaera Reconfigurable Functional Unit. IEEE Transactions on Very Large Scale Integration(VLSI) Systems 12(2), 206–217 (2004)
10. Parizi, H., Niktash, A., Kamalizad, A., Bagherzadeh, N.: A Reconfigurable Architecture for Wireless Communication Systems. In: Third International Conference on Information Technology: New Generations, pp. 250–255 (2006)
11. Hartenstein, R.: Coarse Grain Reconfigurable Architectures. In: Conference on Asia South Pacific Design Automation, pp. 564–570 (2001)
12. Qu, Y., Tiensyrj, K., Soininen, J.-P., Nurmi, J.: Design Flow Instantiation for Run-Time Reconfigurable Systems: A Case Study. EURASIP Journal on Embedded Systems 11 (2008)
13. Heysters, P., Smit, G., Molenkamp, E.: A Flexible and Energy-Efficient Coarse- Grained Reconfigurable Architecture for Mobile Systems. The Journal of Supercomputing 26, 283–308 (2003)
14. Hinkelmann, H., Zipf, P., Li, J., Liu, G., Glesner, M.: On the design of reconfigurable multipliers for integer and Galois field multiplication. Microprocessors & Microsystems 33(1), 2–12 (2009)