

Reduction of Large Resistor Networks

Joost Rommes, Peter Lenaers, and Wil H.A. Schilders

Abstract Electro Static Discharge (ESD) analysis is of vital importance during the design of large-scale integrated circuits, since it gives insight in how well the interconnect can handle unintended peak charges. Due to the increasing amount of interconnect and metal layers, ESD analysis may become very time consuming or even unfeasible. We propose an algorithm for the reduction of large resistor networks, that typically arise during ESD, to much smaller equivalent networks. Experiments show reduction and speed-ups up to a factor 10.

1 Introduction

Electro Static Discharge (ESD) analysis is of vital importance during the design of large-scale integrated circuits and derived products. A human touch charged by walking across a carpet, for instance, can affect or destroy a device containing electric components. The costs involved may vary from a few cents to millions if, due to interconnect failures, a respin of the chip is needed. An example of a damaged piece of interconnect that was too small to conduct the amount of current is shown in Figure 1.

ESD analysis [1, 2] requires knowledge on how fast electrical charge on the pins of a package can be discharged. In many cases, the discharge is done through the power network, the interconnect and the substrate, which are resistive. Diodes are used to protect transistors on a chip against peak charges. The discharge paths, that

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consist of very large resistor networks connected through diodes, must be of low resistance to allow for sufficient discharge.

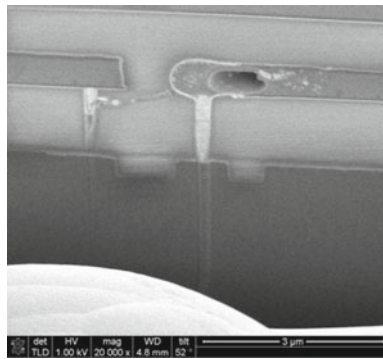


Fig. 1: Example of a piece of interconnect that was damaged because it was too small to conduct the amount of current caused by a peak charge

In practice, one is only interested in the path resistances from the output of one device to the input of another. But since one device can serve as driver to multiple other devices, the network that needs to be analyzed can be regarded as a tree with one root and many leaves. To complicate matters each branch (path from one internal node to another) can consist of multiple parallel paths, thus complicating the computation of the correct resistance.

The interconnect and resistance network are typically modeled by resistors, and diodes are used to connect different parts of the network. The resulting resistive network may contain up to millions of resistors, hundreds of thousands of internal nodes, and thousands of external nodes (nodes with connections to diodes). Simulation of such large networks within reasonable time is often not possible, and including such networks in full system simulations may be even unfeasible. Hence, there is need for much smaller networks that accurately or even exactly describe the resistive behavior of the original network, but allow for fast analysis.

In this paper we describe a new approach for the reduction of large resistor networks. We show how insights from graph theory, numerical linear algebra, and matrix reordering algorithms can be used to construct an equivalent network with the same number of external nodes, but much less internal nodes and resistors. This equivalent reduced network exactly describes the behavior of the original network, i.e., no approximation error is made. The approach is illustrated by numerical results.

The paper is organized as follows. In section 2 we describe the relevant properties of resistor networks and formulate the network reduction problem. An overview of existing approaches to deal with large resistor networks is given in section 3. In section 4 we describe a new approach to reduce resistor networks. Results of the new approach are shown in section 5. Section 6 concludes.

2 Properties of Resistor Networks

A resistor network consists of internal nodes, external nodes (or terminals), and resistors. Figure 2 shows a simple resistor network with external nodes $Z, A, B,$ and $C,$ and internal nodes X and Y (there are five resistors). Of interest are the path resistances from Z to $A, B,$ and $C.$ This small example is purely for illustrational

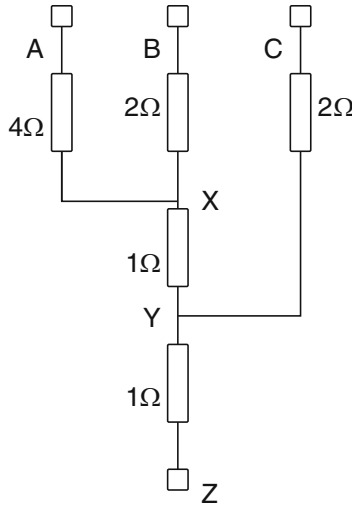


Fig. 2: Simple resistor network with external nodes $Z, A, B,$ and $C.$ Of interest are the path resistances between external nodes

purposes; in real-life applications the number of nodes and resistors is much larger: typical networks consist of millions of resistors and nodes, of which (tens of) thousands are external nodes. In the following it will be assumed that the network has $n > 0$ internal nodes, $m > 0$ external nodes, and $r > 0$ resistors.

2.1 Mathematical Formulation

Using Ohm’s Law for resistors and Kirchhoff’s Current Law [3], the electrical behavior of a resistance network can be described by

$$\mathbf{i} = Y \cdot \mathbf{v}, \tag{1}$$

where $\mathbf{i}, \mathbf{v} \in \mathbb{R}^N$ and $Y \in \mathbb{R}^{N \times N}$ (with $N = n + m$) contain the unknown inflowing currents, node voltages, and conductances, respectively.

We distinguish between internal and external nodes:

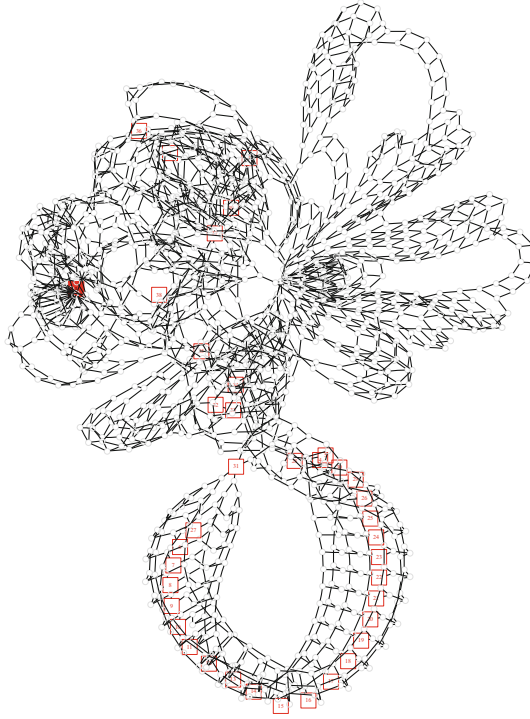


Fig. 3: Graph representation of a realistic resistor network. The *squares* are external nodes and need to be preserved in the reduced network. Of interest are the path resistances between external nodes

$$\begin{bmatrix} \mathbf{i}_e \\ \mathbf{i}_i \end{bmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ei}^T & Y_{ii} \end{bmatrix} \begin{bmatrix} \mathbf{v}_e \\ \mathbf{v}_i \end{bmatrix},$$

where $\mathbf{i}_e, \mathbf{v}_e \in \mathbb{R}^m$ and $\mathbf{i}_i, \mathbf{v}_i \in \mathbb{R}^n$ correspond to external and internal nodes, respectively, and Y is partitioned accordingly. Note that $\mathbf{i}_i = \mathbf{0}$ since it is assumed that currents can only be injected in external nodes.

One node is chosen as reference (ground) node: this makes the Y matrix non-singular. All diagonal elements of Y are strictly positive and all off-diagonal elements are negative or zero. The conductance matrix $Y = (y_{ij})$ is symmetric and (after grounding) positive-definite ($\mathbf{x}^T Y \mathbf{x} > 0$ for all $\mathbf{x} \in \mathbb{R}^n$). In most of the applications, the conductance matrix Y is very sparse, typically having $O(1)$ nonzeros per row. Figure 3 shows a realistic resistor network.

The impedance matrix Z can be obtained by inverting Y : $Z = Y^{-1}$. For large networks this is not possible due to memory and CPU limitations, and it is neither necessary since usually only specific elements are needed: the path resistance from the reference node (terminal) to another terminal b , for instance, is given by the diagonal element z_{bb} .

2.2 Problem Formulation

The problem is: given a very large resistor network described by (1), find an equivalent network with (a) the same external nodes, (b) exactly the same path resistances between external nodes, (c) $\hat{n} \ll n$ internal nodes, and (d) $\hat{r} \ll r$ resistors. Additionally, (e) the reduced network must be realizable as a netlist so that it can be (re)used in the design flow as subcircuit of large systems (see Figure 4 for an example use of a reduced netlist).

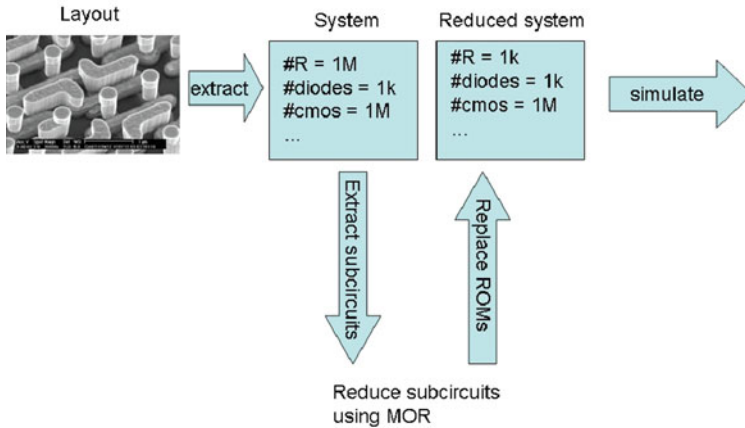


Fig. 4: Typical (re)use of reduced equivalent network in the design flow: the original network is reduced to a smaller network that replaces the original network in the complete system

Simply eliminating all internal nodes will lead to an equivalent network that satisfies conditions (a)–(c), but violates (d) and (e): for large numbers m of external nodes, the number of resistors $\hat{r} = (m^2 - m)/2$ in the dense reduced network is in general much larger than the number of resistors in the sparse original network (r of $O(n)$), leading to increased memory and CPU requirements.

3 Existing Approaches

There are several approaches to deal with large resistor networks. If the need for an equivalent reduced network can be circumvented in some way, this is usually the best to do. To see this, one has to take into account that due to sparsity of the original network, memory usage and computational complexity are *in principle* not an issue, even not for networks containing millions of resistors. Solving linear systems with the related conductance matrices is typically of complexity $O(n^\alpha)$, where $1 < \alpha \leq 2$, instead of the traditional $O(n^3)$ [4], and hence the path resistance problem can be solved directly. Of course, α depends on the sparsity and will rapidly increase as

sparsity decreases. This also explains why eliminating all internal nodes does not work in practice: the large reduction in unknowns is easily undone by the enormous increase in number of resistors, mutually connecting all external nodes.

However, if we want to (re)use the network in full system simulations, a reduced equivalent network is needed to limit simulation times or make simulation possible at all. There is software [5, 6] available for the reduction of parasitic reduction networks, but this software produces approximate reduced networks while in many cases an exact reduced network is needed. In [7] approaches based on large-scale graph partitioning packages such as (h)METIS [8] are described, but only applied to small networks. Structure preserving projection methods for model reduction [9, 10], finally, have the disadvantage that they lead to dense reduced-order models if the number of terminals is large.

4 Improved Approach

Knowing that eliminating all internal nodes is not an option and that projection methods lead to dense reduced-order models, we use concepts from matrix reordering algorithms such as AMD [11] and BBBB [12], usually used as preprocessing step for (parallel) LU- or Cholesky-factorization, to determine which nodes to eliminate. The fill-in reducing properties of these methods also guarantee sparsity of the reduced network. Similar ideas have also been used in [7, 13].

Our main motivation for this approach is that large resistor networks in ESD typically are extracted networks with a structure that is related to the underlying (interconnect) layout. Unfortunately, the extracted networks are usually produced by extraction software of which the algorithms are unknown, and hence the structure of the extracted network is difficult to recover. Standard tools from graph theory, however, can be used to recover at least part of the structure.

Note that in the context of this paper, with structure we refer to the topological structure of the network. This is in contrast with structure preserving model order reduction methods [9], where structure usually refers to the mathematical structure of the dynamical system. In our applications, the reduced network should have approximately the same sparsity and topology as the original network.

Our approach can be summarized as follows:

1. The first step is to bring the conductance matrix Y into Balanced Border Block Diagonal (BBBB) form using techniques of [11, 12, 14], see Figure 5. In this form, the matrix consists of two parts: the main body A_{11} and border blocks A_{12} , $A_{21} = A_{12}^T$ and A_{22} . The main body is partitioned into subblocks, where each block B_{ii} represents a cluster in the network. Block B_{ii} has a nonzero entry when two nodes in cluster i are connected. Internal nodes that connect different clusters are in the border. Borderblock A_{22} contains information on the connections between bordernodes, while borderblocks A_{12} and A_{21} contain information on the connections between bordernodes and the different clusters. The clusters contain both external and internal nodes, while all nodes in the border are internal.

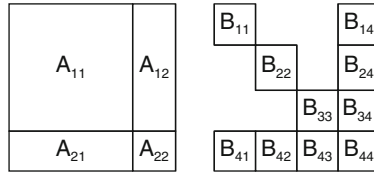


Fig. 5: Matrix in BBBD-form (*left*) with subblocks

2. The second step is to eliminate the internal nodes in block A_{11} . This is done using the Schur complement [15]. Since the ordering is chosen to minimize fill-in, the resulting reduced matrix is sparse. Note that all operations are exact, i.e., we do not make any approximations. As a result, the path resistances between external nodes remain equal to the path resistances in the original network.
3. Finally, the reduced conductance matrix can be realized as an reduced resistor network that is equivalent to the original network. Since the number of resistors (and number of nodes) is smaller than in the original network, also the resulting netlist is smaller in size.

An additional reduction could be obtained by removing relatively large resistors from the resulting reduced network. However, this will introduce an approximation error that might be hard to control a priori, since no sharp upper bounds on the error are available [16]. Another issue that is subject to further research is that the optimal ratio of number of (internal) nodes to resistors (sparsity) may also depend on the ratio of number of external to internal nodes, and on the type of simulation that will be done with the network.

5 Numerical Results

Table 1 shows results for three resistor networks of realistic interconnect layouts. The number of nodes is reduced by a factor > 10 and the number of resistors by a factor > 3 . As a result, the computing time for calculating path resistances in the original network (including nonlinear elements such as diodes) is 10 times smaller.

Table 1: Results of reduction algorithm

	Network I		Network II		Network III	
	Original	Reduced	Original	Reduced	Original	Reduced
#external nodes	274		3399		1978	
#internal nodes	5558	516	99112	6012	101571	1902
#resistors	8997	1505	161183	62685	164213	39011
CPU time	10 s	1 s	67 hrs	7 hrs	20 hrs	2 hrs
Speed up	10x		9.5x		10x	

6 Conclusions

Electro Static Discharge analysis is of crucial importance for present chip design. Because the resulting resistor networks may contain millions of nodes and resistors, full system simulation becomes too expensive or unfeasible, leading to delay in the design cycle. Hence, there is need for reduced networks that are much smaller but exactly reproduce the behavior of the original networks. We propose an algorithm based on concepts from graph and matrix reordering theory. The new method can reduce large resistor networks to small equivalent networks. Since the reduced network exactly matches the behavior of the original network, it can replace the original network in the design flow for Electro Static Discharge analysis. Speedups of up to a factor 10 are obtained for industrial circuits.

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