A New FGMOST Euclidean Distance Computational Circuit Based on Algebraic Mean of the Input Potentials

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Abstract. A new Euclidean distance circuit focused on high-speed operation will be presented in this paper. The computing accuracy will be improved compensating the error introduced by the second-order effects, which affect MOS transistor operation (short channel effect and mobility degradation) by a proper common-mode input voltage excitation of the squarer circuit. Because the elementary approach of designing an Euclidean distance circuit (exclusively based on classical MOS transistors in saturation) requires an additional threshold voltage extractor circuit, the new proposed idea is to use a FGMOST (Floating Gate MOS Transistor), having the advantage of a very large reducing of the circuit complexity.

Keywords: Computational circuits, FGMOST, VLSI design.

1 Introduction

Because of the square-law model of MOS transistor working in saturation, many analog signal-processing functions can be achieved using this square characteristic. Based on this principle, several basic building blocks, such as multipliers, active resistors and transconductors have been developed [1],[2],[3],[4],[5]. The Euclidean distance between $V_a = (V_{a1}, V_{a2}, \cdots, V_{an})$ and $V_b = (V_{b1}, V_{b2}, \cdots, V_{bn})$ (two n-dimensional vectors), defined as:

$$\|V_a - V_b\| = \sqrt{\sum_{k=1}^{n} (v_{ak} - v_{bk})^2}. \tag{1}$$

represents a direct measure of similarity between vectors V_a and V_b. The area of utilization of the Euclidean distance circuits includes instrumentation systems, communication circuits, neural networks, display systems [6] or several classification algorithms such as vector quantization or nearest neighbour classification. Several constraints (circuit area, power dissipation and modularity) limit the possibilities of implementing a high-speed Euclidian distance circuit. Choosing an analog VLSI implementation fulfills all the previous requirements, resulting the necessity of finding a simple and accurate circuit capable to compute the desired function, Euclidean distance.

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2 Principle of Operation

The n-th order Euclidian distance circuit consists in n voltage squarer circuits and a square-root circuit.

2.1 The CMOS Square Circuit

First-order analysis. The proposed CMOS squarer using algebraic mean of the input potentials is presented in Fig. 1. Because $I_{D1}+I_{D2} = I_{D2}+I_{D3} = I_{D3}+I_{D4}$, it results that $I_{D1} = I_{D3}$ and $I_{D2} = I_{D4}$. Considering that all transistors from Fig. 1 are working in saturation and are characterized (in a first-order analysis) by a square characteristic, it is possible to write that $V_{GS_1} = V_{GS_3}$ and $V_{GS_2} = V_{GS_4}$, resulting a V potential equal with the algebraic mean of the input potentials:

$$V = \frac{V_a + V_b}{2}. \tag{2}$$

In this case, the output current of the circuit from Fig. 1 will have the following expression:

$$I_O = I_1 + I_2 - I = \frac{K}{2}(V_a - V_T)^2 + \frac{K}{2}(V_b - V_T)^2 - K(\frac{V_a + V_b}{2} - V_T)^2. \tag{3}$$

equivalent with:

$$I_O = \frac{K}{4}(V_a - V_b)^2 \tag{4}$$

So, the circuit computes the square of the differential input voltage.

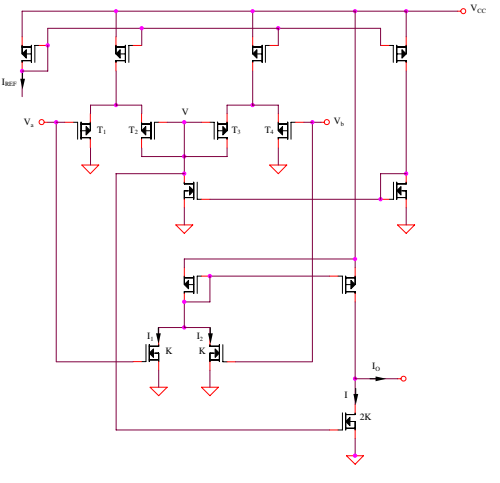

Fig. 1. CMOS squarer using algebraic mean of the input potentials

Second-order effects. Considering the second-order effects, which affect the MOS transistor operation, that is short-channel effect (5) and mobility degradation (6):

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{5}$$

$$K = \frac{K_0}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})} \tag{6}$$

and supposing that the design condition $\lambda = \theta_D$ is fulfilled, it results that the gate-source voltage of a transistor working in saturation will have the following expression:

$$V_{GS} \cong V_T + \sqrt{\frac{2I}{k}} + \theta_G \frac{I}{k} \tag{7}$$

In this case, because $I_{D1} = I_{D3}$ and $I_{D2} = I_{D4}$, the relations $V_{GS_1} = V_{GS_3}$ and $V_{GS_2} = V_{GS_4}$ still remain valuable, so, even in a second-order analysis, the potential V will have the same expression (2). It results:

$$I_O = \frac{K}{4}(V_a - V_b)^2 - \theta_G[(V_a - V_T)^3 + (V_a - V_T)^3 - 2(\frac{V_a + V_b}{2} - V_T)^3]. \tag{8}$$

After algebraic calculations, the output current will have the following expression:

$$I_O = \frac{K}{4}(V_a - V_b)^2 - \frac{3}{4}\theta_G(V_a - V_b)^2(V_a + V_b - 2V_T) \tag{9}$$

The last term of (9) represents the error introduced by the mobility degradation. It is obvious that if the common mode input voltage is a little bit smaller than the MOS threshold voltage, that is if $V_a = v_a + V_T$ and $V_b = v_b + V_T$, with $v_a, v_b \ll V_T$, this error could be strongly reduced, resulting:

$$\epsilon_r = 3\theta_G(v_a + v_b) \ll 6\theta_G V_T \tag{10}$$

2.2 The CMOS Square-Root Circuit

Because of the square characteristic of MOS transistor working in saturation, a square-root circuit is relatively easy to implement in CMOS technology. The simplest approach is referring to a gate-source connected NMOS transistor (Fig. 2).

The circuit output voltage is:

$$V_O = V_T + \sqrt{\frac{2I_O}{k}} \tag{11}$$

The main disadvantage of the proposed square-root circuit is the necessity of using a threshold voltage extractor circuit to compute V_T , in order to remove the first undesired term from relation (11). As a result, the extreme simplicity of the proposed circuit will be considerable increased by this block. Three possible implementations of threshold voltage extractor circuits, preferred for theirs relatively small silicon area consumption due to the removing of any resistor from theirs design are presented in Fig. 3, 4 and 5, respectively.

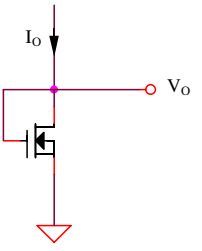

Fig. 2. The CMOS square-root circuit using a gate-source connected NMOS transistor

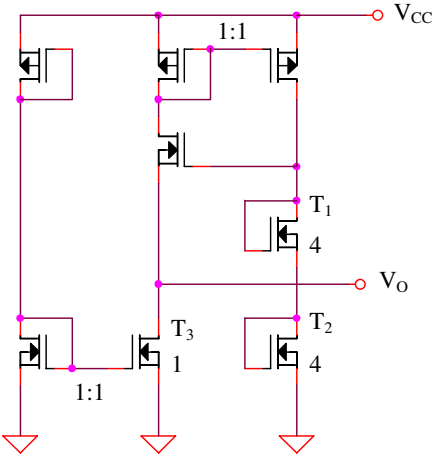

Fig. 3. Threshold voltage extractor - version I

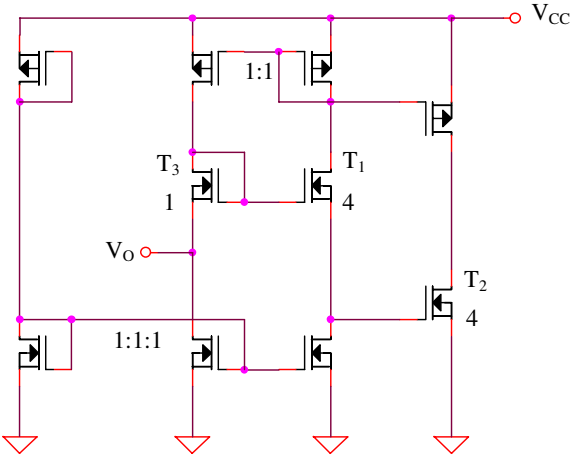

Fig. 4. Threshold voltage extractor - version II

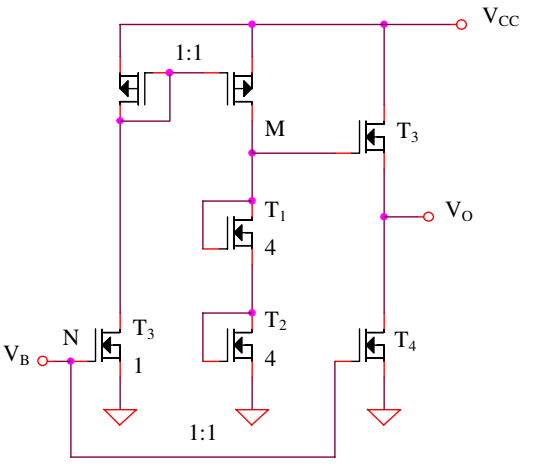

Fig. 5. Threshold voltage extractor - version III

The output voltage of the first two voltage extractor circuit could be written as:

$$V_O = V_{GS_1} + V_{GS_2} - V_{GS_3} \tag{12}$$

Considering that all the MOS transistors are working in saturation at the same drain current and supposing that the aspect ratio of T_1 and T_2 transistors are four time greater that the aspect ratio of T_3, the output voltage will be equal with the threshold voltage of the NMOS devices:

$$V_O = V_{T_n} \tag{13}$$

For the same reason, the differential voltage $V_M - V_N$ (for the third V_T extractor circuit) will be equal with the threshold voltage. A difference circuit $T_3 - T_4$ (working in saturation) is used in order to refer the output voltage of the circuit to the ground. The output voltage of the difference circuit (which is the same with the output voltage of the threshold voltage extractor circuit) will have the following expression:

$$V_O = V_M - V_N = V_{T_n} \tag{14}$$

2.3 The CMOS Square-Root Circuit Using a FGMOS (Floating Gate MOS Transistor)

The multiple-input floating-gate transistor is an ordinary MOS transistor whose gate is floating. The basic structure of a n-channel floating-gate MOS transistor is shown in Fig. 6a. The floating-gate is formed by the first silicon layer over the channel while the multiple input gates are formed by the second polysilicon layer, which is located over the floating-gate. This floating-gate is capacitive coupled to the multiple input gates. The symbolical representation of such devices is shown in Fig. 6b.

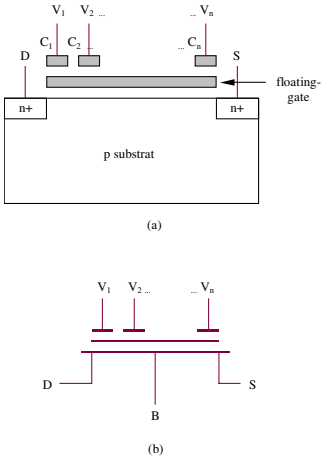

Fig. 6. (a) N-channel FGMOS transistor; (b) symbolic representation

The drain current of a FGMOS transistor with n-input gates in the saturation region is given by the following equation:

$$I_D = \frac{K}{2}[\sum_{i=1}^{n} k_i(V_i - V_S)^2 - V_T]. \tag{15}$$

where $K = \mu_n C_{ox}(W/L)$ is the transconductance parameter of the transistor, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W/L is the transistor aspect ratio, $k_i, i = 1, \cdots, n$ are the capacitive coupling ratios, V_i is the i-th input voltage, V_S is the source voltage and V_T is the threshold voltage of the transistor. The capacitive coupling ratio is defined as:

$$k_i = \frac{C_i}{\sum_{i=1}^{n} C_i + C_{GS}}. \tag{16}$$

where C_i are the input capacitances between the floating-gate and each of the i-th input and C_{ox} is the gate-source capacitance which is equal to $(2/3)C_{ox}$ for operation in the saturation region. All the overlap capacitances are assumed to be considerably smaller than capacitances summation $\sum_{i=1}^{n} C_i + C_{GS}$. Equation (15) shows that the FGMOS transistor drain current in saturation is proportional to the square of the weighted sum of the input signals, where the weight of each input signal is determined by the capacitive coupling ratio of the input. The proposed idea is to replace the classical NMOS transistor from Fig. 2 with a FGMOST for implementing the square-root circuit. The main goal of this replacement is the possibility of removing the first term from relation (11) by a proper polarization of the second gate of the FGMOST, that is without using any additional threshold extractor circuit and, in consequence, with an important reducing of the silicon area occupied by the Euclidean distance circuit. The FGMOS implementation of the square-root circuit is presented in Fig. 7.

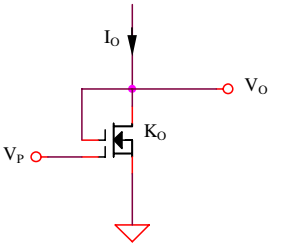

Fig. 7. The FGMOS square-root circuit

Applying relation (15) for the circuit presented in Fig. 7, it results that:

$$I_O = \frac{K_O}{2}(kV_O - kV_B - V_T)^2 \tag{17}$$

Considering a polarization voltage V_B that satisfies the condition $V_B = V_T/k$, the output voltage of the circuit from Fig. 7 will have the following expression:

$$V_O = \frac{1}{k}\sqrt{\frac{2I_O}{K_O}} \tag{18}$$

3 Euclidean Distance Circuit Using a FGMOST

The block diagram of the FGMOST Euclidean distance circuit is presented in Fig. 8. Considering n square circuits from Fig. 1 and the FGMOS square-root

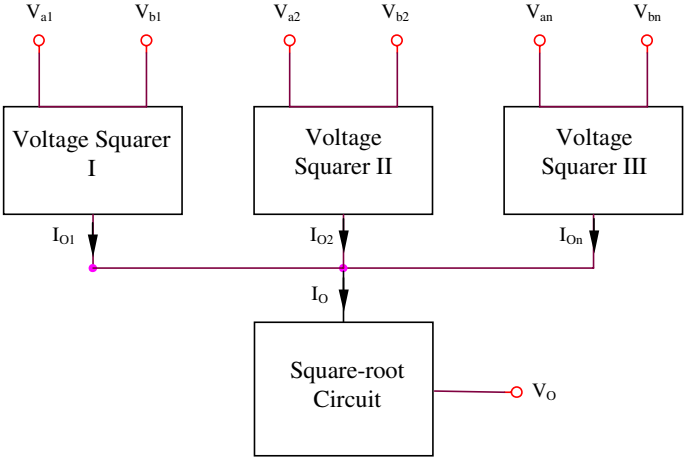

Fig. 8. The block diagram of the FGMOST Euclidean distance circuit

circuit from Fig. 7 and imposing that $K/2K_o = k^2$, the output voltage of the Euclidean distance circuit will have the following expression:

$$V_O = \sqrt{\sum_{k=1}^{n} (v_{ak} - v_{bk})^2}. \tag{19}$$

4 Conclusions

The proposed circuit implements three important functions in the area of computational circuits: the squaring and square-root functions and the Euclidian distance. In order to reduce the circuit complexity by removing the necessity of using a threshold voltage extractor block, a FGMOS transistor is used. An original technique for reducing the squarer errors introduced by the second-order effects that affect the MOS transistor operation have been presented.

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