A Non-subtraction Configuration of Self-similitude Architecture for Multiple-Resolution Edge-Filtering CMOS Image Sensor

Norihiro Takahashi and Tadashi Shibata

Department of (Frontier Informatics;
Electrical Engineering and Information Systems),
The University of Tokyo,
7-3-1 Hongo, Bunkyo-ku, Tokyo, Japan
ntaka@else.k.u-tokyo.ac.jp, shibata@ee.t.u-tokyo.ac.jp
http://www.if.t.u-tokyo.ac.jp/

Abstract. The *self-similitude* architecture developed in our previous work for multiple-resolution image perception [1] has been transformed into a non-subtraction configuration. In contrast to the previous work, the subtraction operations are entirely eliminated from the computation repertory of processing elements. As a result, the hardware organization of multiple-resolution edge-filtering image sensor has been greatly simplified. In addition, a fully pixel-parallel *self-similitude* processing has been established without any complexity in the interconnects. A proof-of-concept chip capable of performing four directional edge filtering at full, half and quarter resolutions was designed in a 0.18μm 5-metal CMOS technology and was sent to fabrication. The performance was verified by circuit simulation (Synosyps NanoSim), showing that the four directional edge filtering at multiple resolutions is carried out at more than 1000 frames/sec. with a clock rate of 500kHz.

Keywords: Edge Detection, Hardware Implementation, Image Perception, Multiple-Resolution, Self-Similitude.

1 Introduction

Edge detection is one of the most fundamental image pre-processing for human-like visual perception systems. It is grounded on the fact that human image recognition relies on edge information in various orientations extracted from input images [2]. In fact, many algorithms have been established using directional edge detection in the fields of feature extraction from images and image feature vector representation [3]-[4].

The multiple-resolution image processing scheme is exploited to handle various sizes of images. When the edge-based image representation [4] is combined with multiple-resolution processing, image recognition robust against scaling has

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been demonstrated [5]. However, because directional edge filtering in multiple-resolutions is computationally very expensive, hardware implementation is necessary for real-time recognition system. In this regard, the *self-similitude* architecture was proposed for the first time and implemented in an analog CMOS image sensor in our previous work [1].

The concept of the multiple-resolution image perception is illustrated in Fig. 1 [5], taking face detection as an example. There are three different-size facial images in the full size picture, in which only the smallest size face is enclosed in the detection window. However, by scaling the picture with 1/2, 1/4... resolutions, different size faces are all detected. It was shown in [5], where any size facial images can be correctly recognized by the combination of $(1/2)^n$-scaling of input images and the use of three different sizes for template images, viz. 100%, 80%, and 60%.

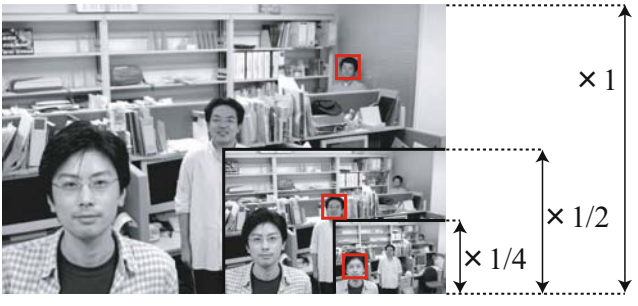

Fig. 1. Concept of multi-resolution image perception. Any size facial images can be detected by combination of $(1/2)^n$-scaling of input images and use of three template image sizes of 100%, 80%, and 60%.

Multiple-resolution image processing functions were utilized in various objectives and already implemented in several chips. A multiresolution image sensor [6] has the simple function of multiple-resolution image readout. There were also image sensors for programmable kernel filtering, where the kernel size is variable and any sort of convolution is practicable [7]-[9]. An edge detection image sensor was reported employing the multi-scale veto algorithm [10]. In a spatial-temporal multiresolution image sensor [11], the resolution is intentionally changed to realize low-power object tracking. Such a spatial-temporal multiple-resolution function was first implemented in [12].

In our previous work [1], a multiple-resolution edge-filtering CMOS image sensor was developed based on the *self-similitude* architecture. The proof-of-concept chip was designed using the voltage mode analog circuitry and fabricated to verify the concept. However, the subtraction operation included in the basic repertory of processing elements (PEs) made the PE control very complicated and reduced the fill factor of each pixel. In order to solve the problem, one row (and one column) of subtraction circuitries are placed at the peripheries of

the photodiode and PE array, and the subtraction operation was removed from the PE array. However, this has reduced the advantage of the *self-similitude* architecture which offers a fully pixel-parallel processing capability of a CMOS image sensor for multiple-resolution filtering.

In this work, a non-subtraction configuration of the *self-similitude* architecture was proposed in contrast to the subtraction-separated configuration in our previous work [1]. By assigning a plus or minus sign to the pixel value readout from each pixel, all computations have been archieved using only additions. As a result, the hardware organization and the PE control have been simplified in a great deal and the merit of the fully pixel-parallel computation has been enabled in this configuration. This allows us to develop the application of *self-similitude* architecture not only to edge-filtering, but also to different types of multiple-resolution image processing on CMOS image sensors.

2 Non-subtraction Configuration of Self-similitude Algorithm

The basic idea of the *self-similitude* algorithm for multiple-resolution edge filtering was already presented in our previous paper [1]. However, because the algorithm has been modified to remove subtraction operations, a brief explanation is given in the following. Fig. 2 (a) shows the MIMD (multiple instruction multiple data) organization of the multiple-resolution edge filter. Photodiodes (PDs) are located at four corners of each PE, allowing each PE to receive four pixel luminance data using only intra-PE interconnects [13]. Fig. 2 (b) shows the output signal from a PD cell which bears a plus or minus sign with respect to the bias value.

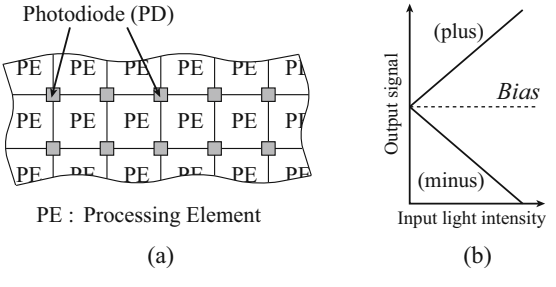

Fig. 2. MIMD organization of multi-resolution edge-filtering image sensor (a) and output signal from a PD cell (b)

Fig. 3 compares the fundamental operation repertory in the modified algorithm with that of the previous one. In the modified algorithm, only two types of operations, addition of the inputs from PDs at four corners and addition of

the inputs from four neighboring PEs, are defined. Because the number of operations is reduced from ten to two, the control signal management of PEs has been greatly simplified. Furthermore, because the operation necessary for edge filtering is only addition, the PEs for subtraction which were placed at the periphery of the PD and PE array in the previous work have been entirely eliminated. The sign patterns of convolution kernels are generated by assigning a proper plus/minus sign to each PD readout.

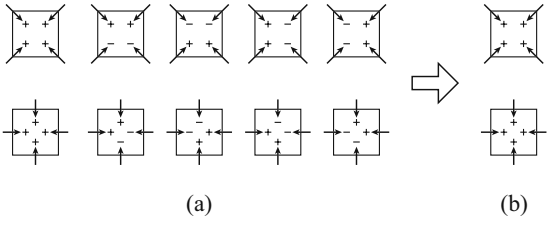

Fig. 3. Fundamental operation repertory in previous work (a) and in this modified algorithm (b)

The procedure of multiple-resolution directional edge filtering is explained in Fig. 4 using two typical examples. Full-resolution horizontal edge filtering proceeds in two steps. Before the processing, plus signs are assigned to upper PD cells, while minus signs are assigned to lower PD cells as shown in the left of Fig. 4 (a). In the first step, four PEs carry out the diagonal-input addition. In the second step, the center PE carries out orthogonal-input addition using the first step results (R). This results in a horizontal edge filtering of the 4x4 kernel. During the processing, the same operations are being carried out in other equivalent locations simultaneously. Then the roles (first step operations and second step operations) of respective PEs are interchanged and the same procedure is repeated to accomplish the filtering for the entire image.

The half-resolution +45-degree edge filtering requires three steps as illustrated in Fig. 4 (b). Before the processing, PD cells in the upper left triangle region are assigned with plus signs, PD cells in the lower right triangle region with minus signs, and PD cells on the central diagonal line with zero values. 16 PEs (+ marked) carry out the diagonal addition in the first step and four PEs (+ marked) carry out the orthogonal addition in the second step using the first-step operation results (R). In the third step, the center PE (also + marked) conducts the addition using the second-step operation results (R'). The resultant kernel is for an 8x8, +45-degree edge filtering. In order to expand the kernel region to one step a larger area, the orthogonal addition need be repeated one more time.

In the previous work, a filtering kernel pattern having plus and minus coefficients was produced by addition and subtraction operations of PEs. This increased the number of operations of a PE as shown in Fig. 3 (a). In the present work, however, plus and minus signs are assigned to output signals from PDs to

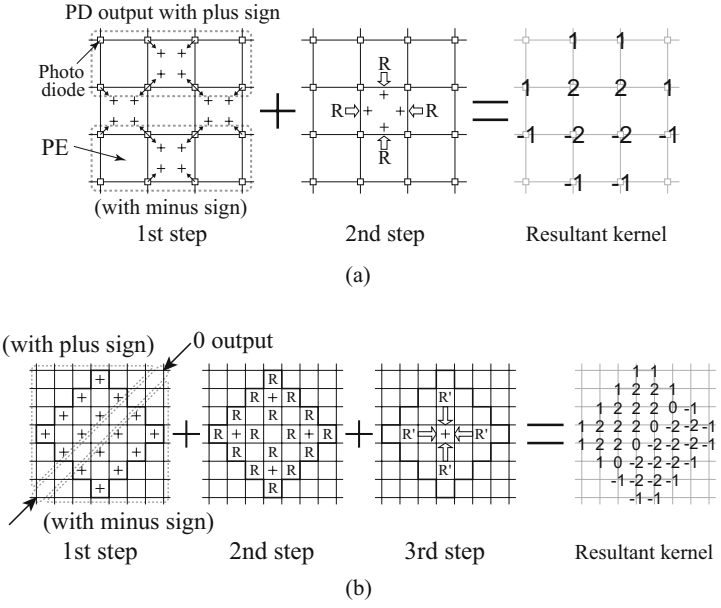

Fig. 4. Full-resolution horizontal (a) and half-resolution +45-degree (b) edge filtering operations

produce kernel patterns. Then, only addition operations are required for PEs. This has resulted in a great simplification of the hardware organization and a fully pixel-parallel implementation of the *self-similitude* architecture in the CMOS image sensor has been enabled for various kinds of filtering processing in the multiple-resolution regime.

3 Hardware Organization of Edge Filtering Image Sensor

The hardware organization in this work is shown in Fig. 5 in comparison with that of the previous work. The hardware consists of a 56x56-PD array and a 55x55-PE array. Interconnects are provided among all nearest neighbor PEs for full resolution processing, among every two and four rows/columns for half and quarter resolution processing, respectively. As compared to the previous work, the PEs for subtraction are removed in this work, which has greatly simplified the control signal management for PEs and also has reduced the chip area.

Each PD cell has the function of linearly transforming the light intensity into the analog electrical signal. The output of each PD is controlled by the external digital signals. That is, the output value (Out) is plus/minus signed value of input signal (In) with bias value ($Bias$), or just bias value itself.

$$Out = \pm In + Bias\ (Plus/Minus),\ Bias\ (Zero). \tag{1}$$

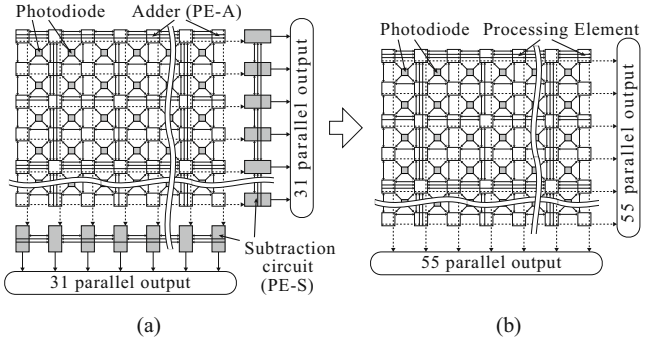

Fig. 5. Hardware organization of multi-resolution directional edge filtering image sensor in previous work (a) and in present work (b)

Fig. 6 represents the block diagram of PE cell. One of the four input data (from PD, nearest/second/fourth neighbor PEs) is selected by the selector at each side of the PE. Then, the addition of these selected inputs is carried out and the result is sent to neighbor PEs in all directions.

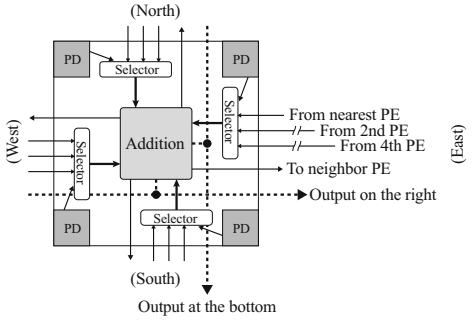

Fig. 6. Block diagram of PE cell

Examples of single row/column parallel processing are illustrated in Fig. 7. An example of full-resolution horizontal edge filtering is shown in Fig. 7 (a), where the second step of the processing is carried out in every two PEs (depicted in gray) in the same row. An example of full-resolution +45-degree edge filtering is represented in Fig. 7 (b), and the second step is operated in the PEs on the diagonal line. Fig. 8 shows the pixel-parallel processing using the same examples of the processing in Fig. 7. Control signals for assigning plus and minus signs are inputted from the outside of the PD array. If the control signals are made to propagate in four directions in the PD array, simple wiring scheme would be achieved even for pixel-parallel processing.

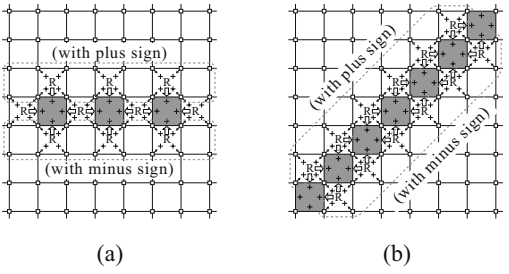

Fig. 7. Examples of row/column parallel processing: full-resolution horizontal edge filtering (a) and +45-degree edge filtering (b)

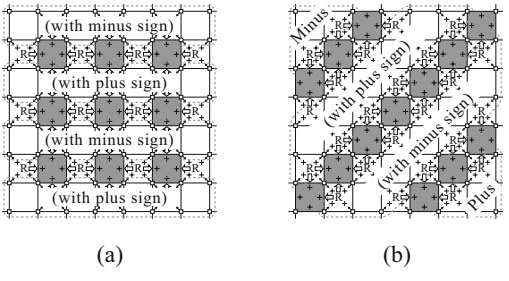

Fig. 8. Examples of pixel-parallel processing: full-resolution horizontal edge filtering (a) and +45-degree edge filtering (b)

4 Hardware Implementation and Discussions

The concept of the non-subtraction configuration of the *self-similitude* architecture was implemented in the hardware using current-mode analog computation. The layout and the specification of the proof-of-concept chip are shown in Fig. 9. In this chip, only the line parallel processing as illustrated in Fig. 7 was implemented for the purpose of verifying the concept. However, extension to the pixel-parallel processing shown in Fig. 8 can be easily accomplished by just changing the control circuitries outside the PD array so that they produce the signals necessary for pixel-parallel processing.

Simulation results are demonstrated in Fig. 10. The illumination data for the PDs were virtually given as external analog signals. A circular picture was used as an input. Circular silhouettes corresponding to respective edge directions are seen in the edge filtering results. In this simulation, the execution time for each row/column edge filtering was within 2μs, which implies every directional edge filtering at multiple-resolution for entire image is accomplished in less than 220μs. This result means the presented multiple-resolution edge filtering processor has the capability of performing more than 1000 frames/sec (limited by the PD integration and readout time). Since the power consumption is easily reduced by introducing the enable function, the chip is also embeddable in low power systems.

Process Technology	0.18μm CMOS, 1-Poly, 5-Metal
Die Size	5.0mm x 5.0mm
Voltage Supply	1.8 V
PE Size	73.68μm x 62.56μm
PD Size	13.84μm x 26.72μm
Fill Factor	8.0 %
Resolution	1/1, 1/2, 1/4-res.

Fig. 9. Layout and specification of proof-of-concept chip

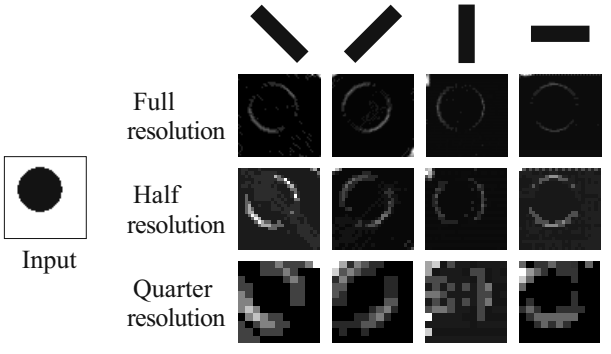

Fig. 10. Simulation results of multi-resolution directional edge filtering

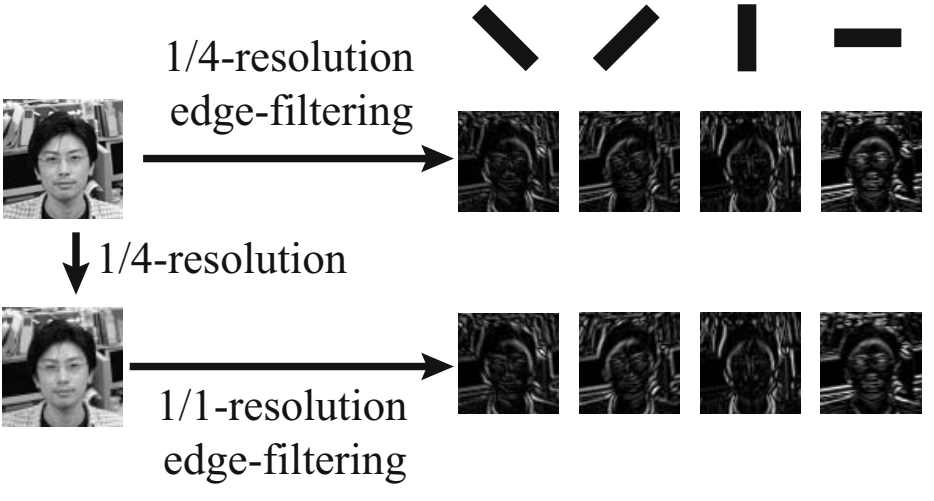

Fig. 11. Verification of *self-similitude* computation algorithm

Because the edge filtering kernels of lower resolutions are not the exact expansions of the full-resolution kernels, the *self-similitude* algorithm is verified by software simulation. Fig. 11 shows the simulation results of quarter-resolution directional edge filtering using *self-similitude* algorithm and full-resolution directional edge filtering after lowering the resolution from full to quarter. The simulation results indicate that these two different procedures of quarter-resolution edge filtering generate almost the same images. That is, the tiny kernel differences between different resolutions have no great influence upon the final edge pictures.

5 Conclusion

A multiple-resolution directional edge filtering processor has been developed based on the *self-similitude* architecture without using subtraction function. As a result, the hardware structure and the controlling method is greatly simplified. The proof-of-concept chip was designed and the concept has been verified by simulations.

Acknowledgments

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