11. Material Aspects of Micro- and Nanoelectromechanical Systems

Christian A. Zorman, Mehran Mehregany

One of the more significant technological achievements during the last 20 years has been the development of MEMS and its new offshoot, NEMS. These developments were made possible by significant advancements in the materials and processing technologies used in the fabrication of MEMS and NEMS devices. While initial developments capitalized on a mature Si infrastructure built for the integrated circuit (IC) industry, recent advances have come about using materials and processes not associated with IC fabrication, a trend that is likely to continue as new application areas emerge.

A well-rounded understanding of MEMS and NEMS technology requires a basic knowledge of the materials used to construct the devices, since material properties often govern device performance and dictate fabrication approaches. An understanding of the materials used in MEMS and NEMS involves an understanding of material systems, since such devices are rarely constructed of a single material but rather a collection of materials working in conjunction with each other to provide critical functions. It is from this perspective that the following chapter is constructed. A preview of the materials selected for inclusion in this chapter is presented in Table 11.1. It should be clear from this table that this chapter is not a summary of all materials used in MEMS and NEMS, as such a work would itself constitute a text of significant size. It does, however, present a selection of some of the more important material systems, and especially those that illustrate the importance of viewing MEMS and NEMS in terms of material systems.

11.1 Silicon

11.1.1 Single-Crystal Silicon

Use of silicon (Si) as a material for microfabricated sensors dates back to the middle of the 20th century when the piezoresistive effect in germanium (Ge) and Si was first identified [11.1]. It was discovered that the piezoresistive coefficients of Si were significantly higher than those associated with metals used in conventional strain

Table 11.1 Distinguishing characteristics and application examples of selected materials for MEMS and NEMS

Material	Distinguishing characteristics	Application examples
Single-crystal silicon (Si)	High-quality electronic material, selective anisotropic etching	Bulk micromachining, piezoresistive sensing
Polycrystalline Si (polysilicon)	Doped Si films on sacrificial layers	Surface micromachining, electrostatic actuation
Silicon dioxide (SiO_2)	Insulating, etched by HF, compatible with polysilicon	Sacrificial layer in polysilicon surface micromachining, passivation layer for devices
Silicon nitride (Si_3N_4, Si_xN_y)	Insulating, chemically resistant, mechanically durable	Isolation layer for electrostatic devices, membrane and bridge material
Polycrystalline germanium (polyGe), Polycrystalline silicon-germanium (poly SiGe)	Deposited at low temperatures	Integrated surface micromachined MEMS
Gold (Au), aluminum (Al)	Conductive thin films, flexible deposition techniques	Innerconnect layers, masking layers, electromechanical switches
Bulk Ti	High strength, corrosion resistant	Optical MEMS
Nickel-iron (NiFe)	Magnetic alloy	Magnetic actuation
Titanium-nickel (TiNi)	Shape-memory alloy	Thermal actuation
Silicon carbide (SiC) diamond	Electrically and mechanically stable at high temperatures, chemically inert, high Young's modulus to density ratio	Harsh-environment MEMS, high-frequency MEMS/NEMS
Gallium arsenide (GaAs), indium phosphide (InP), indium arsenide (InAs) and related materials	Wide bandgap, epitaxial growth on related ternary compounds	RF MEMS, optoelectronic devices, single-crystal bulk and surface micromachining
Lead zirconate titanate (PZT)	Piezoelectric material	Mechanical sensors and actuators
Polyimide	Chemically resistant, high-temperature polymer	Mechanically flexible MEMS, bioMEMS
SU-8	Thick, photodefinable resist	Micromolding, High-aspect-ratio structures
Parylene	Biocompatible polymer, deposited at room temperature by CVD	Protective coatings, molded polymer structures
Liquid crystal polymer	Chemically resistant, low moisture permeability, insulating	bioMEMS, RF MEMS

gauges; and this finding initiated the development of Si-based strain gauge devices, and along with Si bulk micromachining techniques, piezoresistive Si pressure sensors during the 1960s and 1970s. The subsequent development of Si surface micromachining techniques along with the recognition that micromachined Si structures could be integrated with Si IC devices marked the advent of MEMS with Si firmly positioned as the primary MEMS material.

For MEMS applications, single-crystal Si serves several key functions. Single-crystal Si is one of the most versatile materials for bulk micromachining due

to the availability of anisotropic etching processes in conjunction with good mechanical properties. Single-crystal Si has favorable mechanical properties (i. e., a Young's modulus of about 190 GPa), enabling its use as a material for membranes, resonant beams, and other such structures. For surface micromachining applications, single-crystal Si substrates are used primarily as mechanical platforms on which device structures are fabricated, although the advent of silicon-on-insulator (SOI) substrates enables the fabrication of single-crystal Si surface micromachined structures by using the buried oxide as a sacrificial layer. Use of high-quality single-crystal wafers enables the fabrication of integrated MEMS devices, at least for materials and processes that are compatible with Si ICs.

From the materials perspective, single-crystal Si is a relatively easy material to bulk micromachine due to the availability of anisotropic etchants such as potassium hydroxide (KOH) and tetramethyl-aluminum hydroxide (TMAH) that attack the (100) and (110) Si crystal planes significantly faster than the (111) crystal planes. For example, the etching rate ratio of (100) to (111) planes in Si is about 400:1 for a typical KOH/water etching solution. Silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and some metallic thin films (e.g., Cr, Au, etc.) provide good etch masks for most Si anisotropic etchants. Heavily boron-doped Si is an effective etch stop for some liquid reagents. Boron-doped etch stops are often less than 10 μm thick, since the boron concentration in Si must exceed 7×10^{19} cm^3 for the etch stop to be effective and the doping is done by thermal diffusion. Ion implantation can be used to create a subsurface etch stop layer; however, the practical limit is a few micrometer.

In contrast to anisotropic etching, isotropic etching exhibits no selectivity to the various crystal planes. Commonly used isotropic Si etchants consist of hydrofluoric (HF) and nitric (HNO_3) acid mixtures in water or acetic acid (CH_3COOH), with the etch rate dependent on the ratio of HF to HNO_3. From a processing perspective, isotropic etching of Si is commonly used for removal of work-damaged surfaces, creation of structures in single-crystal slices, and patterning of single-crystal or polycrystalline films.

Well-established dry etching processes are routinely used to pattern single-crystal Si. The process spectrum ranges from physical techniques such as sputtering and ion milling to chemical techniques such as plasma etching. Reactive ion etching (RIE) is the most commonly used dry etching technique for Si patterning. By combining both physical and chemical processes, RIE is a highly effective anisotropic Si etching technique that can be used to generate patterns that are independent of crystalline orientation. Fluorinated compounds such as CF_4, SF_6, and NF_3, or chlorinated compounds such as CCl_4 or Cl_2, sometimes mixed with He, O_2, or H_2, are commonly used in Si RIE. The RIE process is highly directional, which enables direct lateral pattern transfer from an overlying masking material to the etched Si surface. SiO_2 thin films are often used as masking and sacrificial layers owing to its chemical durability under these plasma conditions. Process limitations (i. e., etch rates) restrict the etch depths of conventional Si RIE to less than 10 μm; however, a process called deep reactive ion etching (DRIE) has extended the use of anisotropic dry etching to depths well beyond several hundred micrometer.

Using the aforementioned processes and techniques, a wide variety of microfabricated devices have been made from single-crystal Si, such as piezoresistive pressure sensors, accelerometers, and mechanical resonators, to name a few. Using nearly the same approaches but on a smaller scale, *top-down* nanomachining techniques have been used to fabricate nanoelectromechanical devices from single-crystal Si. Single-crystal Si is particularly well suited for nanofabrication because high crystal quality substrates with very smooth surfaces are readily available. By coupling electron-beam (e-beam) lithographic techniques with conventional Si etching, device structures with submicrometer dimensions have been fabricated. Submicrometer, single-crystal Si nanomechanical structures have been successfully micromachined from bulk Si wafers [11.2]

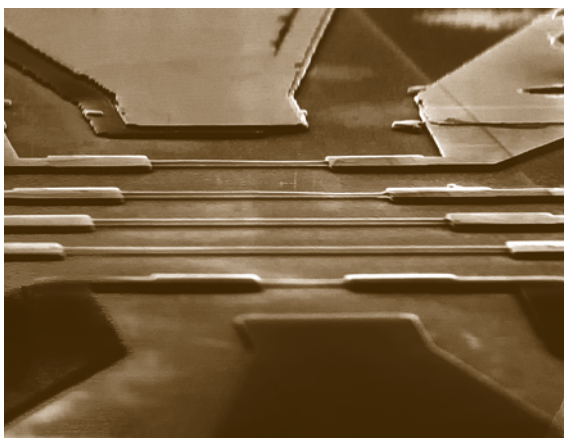

Fig. 11.1 A collection of Si nanoelectromechanical beam resonators fabricated from a single-crystal Si substrate (courtesy M. Roukes, Caltech)

and silicon-on-insulator (SOI) wafers [11.3]. In the former case, an isotropic Si etch was performed to release the device structures, whereas in the latter case, the 50–200 nm structures were released by dissolving the underlying oxide layer in HF. An example of nanoelectromechanical beam structures fabricated from a single-crystal Si substrate is shown in Fig. 11.1.

11.1.2 Polycrystalline and Amorphous Silicon

Surface micromachining is a process where a sequence of thin films, often of different materials, is deposited and selectively etched to form the desired micromechanical (or microelectromechanical) structure. In contrast to bulk micromachining, the substrate serves primarily as a device-supporting platform. For Si-based surface micromachined MEMS, polycrystalline Si (polysilicon) is most often used as the structural material, SiO_2 as the sacrificial material, silicon nitride (Si_3N_4) for electrical isolation of device structures, and single-crystal Si as the substrate. Like single-crystal Si, polysilicon can be doped during or after film deposition. SiO_2 can be thermally grown or deposited on polysilicon over a broad temperature range (e.g., 200–1150 °C) to meet various process and material requirements. SiO_2 is readily dissolvable in hydrofluoric acid (HF), which does not etch polysilicon and thus can be used to dissolve SiO_2 sacrificial layers. Si_3N_4 is an insulating film that is highly resistant to oxide etchants. The polysilicon micromotor shown in Fig. 11.2 was surface micromachined using a process that included these materials.

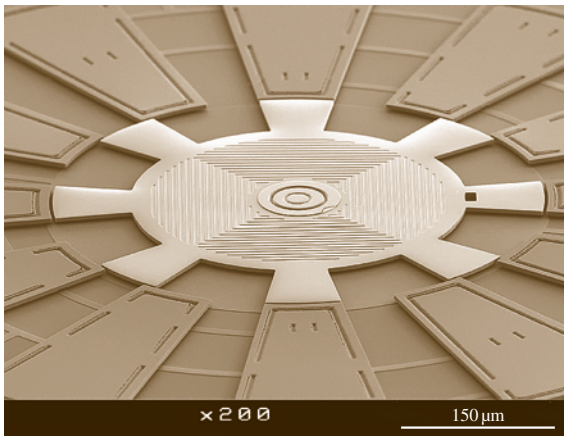

Fig. 11.2 SEM micrograph of a surface micromachined polysilicon micromotor fabricated using a SiO_2 sacrificial layer

For MEMS and IC applications, polysilicon films are commonly deposited using a process known as low-pressure chemical vapor deposition (LPCVD). The typical polysilicon LPCVD reactor is based on a hot-wall, resistance-heated furnace. Typical processes are performed at temperatures ranging from 580 to 650 °C and pressures from 100 to 400 mtorr. The most commonly used source gas is silane (SiH_4). The microstructure of polysilicon thin films consist of a collection of small grains whose microstructure and orientation is a function of the deposition conditions [11.4]. For typical LPCVD processes (e.g., 200 mtorr), the amorphous-to-polycrystalline transition temperature is about 570 °C, with polycrystalline films deposited above the transition temperature. At 600 °C, the grains are small and equiaxed, while at 625 °C, the grains are large and columnar [11.4]. The crystal orientation is predominantly (110) Si for temperatures between 600 and 650 °C, while the (100) orientation is dominant for temperatures between 650 and 700 °C.

The resistivity of polysilicon can be modified using the doping methods developed for single-crystal Si. Diffusion is an effective method for doping polysilicon films, especially for heavy doping of thick films. Phosphorus, which is the most commonly used dopant in polysilicon MEMS, diffuses significantly faster in polysilicon than in single-crystal Si due primarily to enhanced diffusion rates along grain boundaries. The diffusivity of phosphorus in polysilicon thin films with small equiaxed grains is about $1 \times 10^{12}\,\mathrm{cm}^2/\mathrm{s}$. Ion implantation is also used to dope polysilicon films. A high-temperature annealing step is usually required to electrically activate the implanted dopants as well as to repair implant-related damage in the polysilicon films. In general, the conductivity of implanted polysilicon films is not as high as films doped by diffusion.

In situ doping of polysilicon is performed by simply including a dopant gas, usually diborane (B_2H_6) or phosphine (PH_3), in the CVD process. The addition of dopants during the deposition process not only modifies the conductivity but also affects the deposition rate of the polysilicon films. As shown in Fig. 11.3, the inclusion of boron generally increases the deposition rate of polysilicon relative to undoped films [11.5], while phosphorus (not shown) reduces the rate. In situ doping can be used to produce conductive films with uniform doping profiles without requiring the high-temperature steps commonly associated with diffusion or ion implantation. Although commonly used to produce doped polysilicon for electrostatic devices, *Cao* et al. [11.6] have used in situ phosphorus-doped

polysilicon films in piezoresistive strain gauges, achieving gauge factors as high as 15 for a single strip sensor.

The thermal conductivity of polysilicon is a strong function of its microstructure, and therefore the conditions used during deposition [11.4]. For fine-grained films, the thermal conductivity is about 25% of the value of single-crystal Si. For thick films with large grains, the thermal conductivity ranges between 50% and 85% of the single-crystal value.

Like the electrical and thermal properties of polysilicon, the as-deposited residual stress in polysilicon films depends on microstructure. For films deposited under typical conditions (200 mtorr, 625 °C), the as-deposited polysilicon films have compressive residual stresses. The highest compressive stresses are found in amorphous Si films and polysilicon films with a strong, columnar (110) texture. For films with fine-grained microstructures, the stress tends to be tensile. Annealing can be used to reduce the compressive stress in as-deposited polysilicon films. For instance, compressive residual stresses on the order of 500 MPa can be reduced to less than 10 MPa by annealing the as-deposited films at 1000 °C in a N_2 ambient [11.7, 8]. Rapid thermal annealing (RTA) provides an effective method of stress reduction in polysilicon films on temperature-sensitive substrates. *Zhang* et al. [11.9] reported that a 10 s anneal at 1100 °C was sufficient to completely relieve the stress in films that originally had a compressive stress of about 340 MPa. RTA is particularly attractive in situations where the process parameters require a low thermal budget.

As an alternative to high-temperature annealing, *Yang* et al. [11.10] have developed an approach that actually utilizes the residual stress characteristics of polysilicon deposited under various conditions to construct polysilicon multilayers that have the desired thickness and stress values. The multilayers are comprised of alternating tensile and compressive polysilicon layers that are deposited in a sequential manner. The tensile layers consist of fine-grained polysilicon grown at a temperature of 570 °C, while the compressive layers are made up of columnar polysilicon deposited at 615 °C. The overall stress in the composite film depends on the number of alternating layers and the thickness of each layer. With the proper set of parameters, a composite polysilicon multilayer can be deposited with near zero residual stress and no stress gradient. The process achieves stress reduction without high-temperature annealing, a considerable advantage for integrated MEMS processes.

Many device designs require polysilicon thicknesses that are not readily achievable using conventional LPCVD polysilicon due to the low deposition rates associated with such systems. For these applications, epitaxial Si reactors can be used to grow polysilicon films. Unlike conventional LPCVD processes with deposition rates of less than 100 Å/min, epitaxial processes have deposition rates on the order of 1 μm/min [11.11]. The high deposition rates result from the much higher substrate temperatures (> 1000 °C) and deposition pressures (> 50 torr) used in these processes. The polysilicon films are usually deposited on SiO_2 sacrificial layers to enable surface micromachining. An LPCVD polysilicon seed layer is sometimes used in order to control nucleation, grain size, and surface roughness. As with conventional polysilicon, the microstructure and residual stress of the epi-poly films, as they are known, are related to deposition conditions. Compressive films generally have a mixture of [110] and [311] grains [11.12, 13], while tensile films have a random mix of [110], [100], [111], and [311] grains [11.12]. The Young's modulus of epi-poly measured from micromachined test structures is comparable with LPCVD polysilicon [11.13]. Mechanical properties test structures [11.11–13], thermal actuators [11.11], electrostatically actuated accelerometers [11.11], and gryoscopes [11.14] have been fabricated from these films.

As a low-temperature alternative to LPCVD polysilicon, physical vapor deposition (PVD) techniques have been developed to produce Si thin films on temperature-sensitive substrates. *Abe* et al. [11.15] and *Honer* et al. [11.16] have developed sputtering pro-

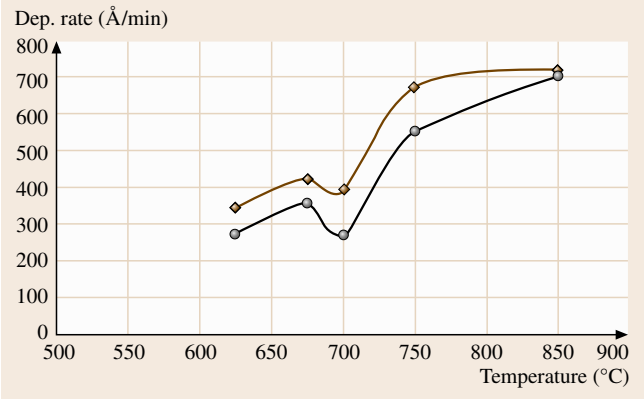

Fig. 11.3 Deposition rate versus substrate temperature for in situ boron-doped (◆) and undoped (○) polysilicon films grown by atmospheric pressure chemical vapor deposition (after [11.5])

cesses for polysilicon. Early work [11.15] emphasized the ability to deposit very smooth (2.5 nm) polysilicon films on thermally oxidized wafers at reasonable deposition rates (19.1 nm/min) and with low residual compressive stresses. The process involved DC magnitron sputtering from a Si target using an Ar sputtering gas, a chamber pressure of 5 mtorr, and a power of 100 W. The authors reported that a post-deposition anneal at 700 °C in N_2 for 2 h was needed to crystallize the deposited film and perhaps lower the stress. *Honer* et al. [11.16] sought to develop a polymer-friendly, Si-based surface micromachining process based on polysilicon sputtered onto polyimide and PSG sacrificial layers. To improve the conductivity of the micromachined Si structures, the sputtered Si films were sandwiched between two TiW cladding layers. The device structures on polyimide were released using oxygen plasma etching. The processing step with the highest temperature was, in fact, the polyimide cure at 350 °C. To test the robustness of the process, sputter-deposited Si microstructures were fabricated on substrates containing CMOS devices. As expected from thermal budget considerations, the authors reported no measurable degradation of device performance.

PECVD has emerged as an alternative to LPCVD for the production of Si-based surface micromachined structures on temperature-sensitive substrates. *Gaspar* et al. [11.17] recently reported on the development of surface micromachined microresonators fabricated from hydrogenated amorphous Si (a-Si:H) thin films deposited by PECVD. The vertically actuated resonators consisted of doubly-clamped microbridges suspended over fixed Al electrodes. The a-Si:H films were deposited using SiH_4 and H_2 precursors and PH_3 as a doping gas. The substrate temperature was held to around 100 °C, which enabled the use of photoresist as a sacrificial layer. The microbridges consisted of a large paddle suspended by two thin paddle supports, with the paddle providing a large reflective surface for optical detection of resonant frequency. The megahertz-frequency resonators exhibited quality factors in the 1×10^5 range when tested in vacuum.

11.1.3 Porous Silicon

Porous Si is produced by room temperature electrochemical etching of Si in HF. If configured as an electrode in an HF-based electrochemical circuit, positive charge carriers (holes) at the Si surface facilitate the exchange of F atoms with H atoms terminating the Si surface. The exchange continues in the subsurface region, leading to the eventual removal of the fluorinated Si. The quality of the etched surface is related to the density of holes at the surface, which is controlled by the applied current density. For high current densities, the density of holes is high and the etched surface is smooth. For low current densities, the hole density is low and clustered in highly localized regions associated with surface defects. Surface defects become enlarged by etching, which leads to the formation of pores. Pore size and density are related to the type of Si used and the conditions of the electrochemical cell. Both single-crystal and polycrystalline Si can be converted to porous Si.

The large surface-to-volume ratios make porous Si attractive for gaseous and liquid applications, including filter membranes and absorbing layers for chemical and mass sensing [11.18]. When single-crystal substrates are used, the unetched porous layer remains single crystalline and is suitable for epitaxial Si growth. It has been shown that CVD coatings do not generally penetrate the porous regions, but rather overcoat the pores at the surface of the substrate [11.19]. The formation of localized Si-on-insulator structures is therefore possible by simply combining pore formation with epitaxial growth, followed by dry etching to create access holes to the porous region and thermal oxidation of the underlying porous region. A third application uses porous Si as a sacrificial layer for polysilicon and single-crystalline Si surface micromachining. As shown by *Lang* et al. [11.19], the process involves the electrical isolation of the solid structural Si layer by either pn-junction formation through selective doping or use of electrically insulating thin films since the formation of pores only occurs on electrically charged surfaces. A weak Si etchant will aggressively attack the porous regions with little damage to the structural Si layers and can be used to release the devices.

Porous polysilicon is currently being developed as a structural material for chip-level vacuum packaging [11.20]. In this example, a 1.5 μm thick polysilicon is deposited onto a supporting PSG sacrificial layer, electrochemically etched in an HF solution to render it porous, and then annealed by RTA to reduce stress in the porous layer. When fabricated locally over a prefabricated device structure (prior to release), the porous Si forms a localized shell that will serve as a mechanical support for the main packaging structure. The porous structure enables an HF etch to remove the supporting PSG layer as well as any sacrificial oxide layers associated with the prefabricated MEMS device. After the sacrificial etch, the packaging sequence is completed by

depositing a polysilicon film by LPCVD at 179 mtorr on the porous shell, thus fully encapsulating the device under vacuum conditions. This technique was used to package a microfabricated Pirani vacuum gauge, which enabled an in situ measurement of pressure versus time. The authors found no detectable change in pressure over a 3-month period.

11.1.4 Silicon Dioxide

Silicon dioxide (SiO_2) is one of the most widely used materials in the fabrication of MEMS. In polysilicon surface micromachining, SiO_2 is used as a sacrificial material since it can be easily dissolved using etchants that do not attack polysilicon. SiO_2 is widely used as an etch mask for dry etching of thick polysilicon films since it is chemically resistant to dry etching processes for polysilicon. SiO_2 films are also used as passivation layers on the surfaces of environmentally sensitive devices.

The most common processes used to produce SiO_2 films for polysilicon surface micromachining are thermal oxidation and LPCVD. Thermal oxidation of Si is performed at temperatures of 900–1200 °C in the presence of oxygen or steam. Since thermal oxidation is a self-limiting process, the maximum practical film thickness that can be obtained is about 2 μm, which is sufficient for many sacrificial applications. As noted by its name, thermal oxidation of Si can only be performed on Si surfaces.

SiO_2 films can be deposited on a wide variety of substrate materials by LPCVD. In general, LPCVD provides a means for depositing thick (> 2 μm) SiO_2 films at temperatures much lower than thermal oxidation. Known as low-temperature oxides, or LTO for short, these films have a higher etch rate in HF than thermal oxides, which translates to significantly faster release times when LTO films are used as sacrificial layers. Phosphosilicate glass (PSG) can be formed using nearly the same deposition process as LTO by adding a phosphorus-containing gas to the precursor flows. PSG films are useful as sacrificial layers since they generally have higher etching rates in HF than LTO films.

PSG and LTO films are deposited in hot-wall, low-pressure, fused-silica furnaces in systems similar to those described previously for polysilicon. Precursor gases include SiH_4 as a Si source, O_2 as an oxygen source, and, in the case of PSG, PH_3 as a source of phosphorus. LTO and PSG films are typically deposited at temperatures of 425–450 °C and pressures ranging from 200 to 400 mtorr. The low deposition temperatures result in LTO and PSG films that are slightly less dense than thermal oxides due to the incorporation of hydrogen in the films. LTO films can, however, be densified by an annealing step at high temperature (1000 °C). The low density of LTO and PSG films is partially responsible for the increased etch rate in HF.

Thermal SiO_2 and LTO are electrical insulators used in numerous MEMS applications. The dielectric constants of thermal oxide and LTO are 3.9 and 4.3, respectively. The dielectric strength of thermal SiO_2 is 1.1×10^6 V/cm, and for LTO it is about 80% of that value [11.21]. The stress in thermal SiO_2 is compressive with a magnitude of about 300 MPa [11.21]. For LTO, however, the typical as-deposited residual stress is tensile, with a magnitude of about 100–400 MPa [11.21]. The addition of phosphorus to LTO decreases the tensile residual stress to about 10 MPa for phosphorus concentrations of 8% [11.22]. As with polysilicon, the properties of LTO and PSG are dependent on processing conditions.

Plasma enhanced chemical vapor deposition (PECVD) is another common method to produce oxides of silicon. Using a plasma to dissociate the gaseous precursors, the deposition temperatures needed to deposit PECVD oxide films is lower than for LPCVD films. For this reason, PECVD oxides are quite commonly used as masking, passivation, and protective layers, especially on devices that have been coated with metals.

Quartz is the crystalline form of SiO_2 and has interesting properties for MEMS. Quartz is optically transparent, piezoelectric, and electrically insulating. Like single-crystal Si, quartz substrates are available as high-quality, large-area wafers that can be bulk micromachined using anisotropic etchants. A short review of the basics of quartz etching was written by *Danel* et al. [11.23] and is recommended for those interested in the subject. Quartz has recently become a popular substrate material for microfluidic devices due to its optical, electronic, and chemical properties.

Another SiO_2-related material that has recently found uses in MEMS is spin-on-glass (SOG). SOG is a polymeric material with a viscosity suitable for spin coating. Two recent publications illustrate the potential for SOG in MEMS fabrication. In the first example, *Yasseen* et al. [11.24] detailed the development of SOG as a thick-film sacrificial molding material for thick polysilicon films. The authors reported a process to deposit, polish, and etch SOG films that were 20 μm thick. The thick SOG films were patterned into molds and filled with 10 μm thick LPCVD polysilicon films, planarized by selective CMP, and subsequently

dissolved in a wet etchant containing HCl, HF, and H_2O to reveal the patterned polysilicon structures. The cured SOG films were completely compatible with the polysilicon deposition process. In the second example, *Liu* et al. [11.25] fabricated high aspect ratio channel plate microstructures from SOG. Electroplated nickel (Ni) was used as a molding material, with Ni channel plate molds fabricated using a conventional LIGA process. The Ni molds were then filled with SOG, and the sacrificial Ni molds were removed in a reverse electroplating process. In this case, the fabricated SOG structures (over 100 μm tall) were micromachined glass structures fabricated using a molding material more commonly used for structural components.

11.1.5 Silicon Nitride

Silicon nitride (Si_3N_4) is widely used in MEMS for electrical isolation, surface passivation, etch masking, and as a mechanical material typically for membranes and other suspended structures. Two deposition methods are commonly used to deposit Si_3N_4 thin films, LPCVD, and PECVD. PECVD silicon nitride is generally nonstoichiometric (sometimes denoted as Si_xN_y:H) and may contain significant concentrations of hydrogen. Use of PECVD silicon nitride in micromachining applications is somewhat limited because it has a high etch rate in HF (e.g., often higher than that of thermally grown SiO_2). However, PECVD offers the ability to deposit nearly stress-free silicon nitride films, an attractive property for encapsulation and packaging.

Unlike its PECVD counterpart, LPCVD Si_3N_4 is extremely resistant to chemical attack, thereby making it the material of choice for many Si bulk and surface micromachining applications. LPCVD Si_3N_4 is commonly used as an insulating layer because it has a resistivity of $10^{16}\,\Omega\,\mathrm{cm}$ and field breakdown limit of $10^7\,\mathrm{V/cm}$. LPCVD Si_3N_4 films are deposited in horizontal furnaces similar to those used for polysilicon deposition. Typical deposition temperatures and pressures range between 700 and 900 °C and 200 and 500 mtorr, respectively. The standard source gases are dichlorosilane (SiH_2Cl_2) and ammonia (NH_3). To produce stoichiometric Si_3N_4 a NH_3 to SiH_2Cl_2 ratio 10:1 is commonly used. The microstructure of films deposited under these conditions is amorphous.

The residual stress in stoichiometric Si_3N_4 is large and tensile, with a magnitude of about 1 GPa. Such a large residual stress causes films thicker than a few thousand angstroms to crack. Nonetheless thin stoichiometric Si_3N_4 films have been used as mechanical support structures and electrical insulating layers in piezoresistive pressure sensors [11.26]. To enable the use of Si_3N_4 films for applications that require micrometer-thick, durable, and chemically resistant membranes, Si_xN_y films can be deposited by LPCVD. These films, often referred to as Si-rich or low-stress nitride, are intentionally deposited with an excess of Si by simply decreasing the ratio of NH_3 to SiH_2Cl_2 during deposition. Nearly stress-free films can be deposited using a NH_3-to-SiH_2Cl_2 ratio of 1/6, a deposition temperature of 850 °C, and a pressure of 500 mtorr [11.27]. The increase in Si content not only leads to a reduction in tensile stress, but also a decrease in the etch rate in HF. Such properties have enabled the development of fabrication techniques that would otherwise not be feasible with stoichiometric Si_3N_4. For example, low-stress silicon nitride has been surface micromachined using polysilicon as the sacrificial material [11.28]. In this case, Si anisotropic etchants such as KOH and EDP were used for dissolving the sacrificial polysilicon. *French* et al. [11.29] used PSG as a sacrificial layer to surface micromachine low-stress nitride, capitalizing on the HF resistance of the nitride films.

11.2 Germanium-Based Materials

11.2.1 Polycrystalline Ge

Like Si, Ge has a long history as a semiconductor device material, dating back to the development of the earliest transistors and semiconductor strain gauges. Issues related to germanium oxide, however, stymied the development of Ge for microelectronic devices. Nonetheless, there is a renewed interest in using Ge in surface micromachined devices due to the relatively low processing temperatures required to deposit the material and its compatibility with Si.

Thin polycrystalline Ge (poly-Ge) films can be deposited by LPCVD at temperatures as low as 325 °C on Si, Ge, and SiGe substrates [11.30]. Ge does not nucleate on SiO_2 surfaces, which prohibits the use of thermal oxides and LTO films as sacrificial layers but enables the use of these films as sacrificial molds. Residual stress in poly-Ge films deposited on Si substrates can

be reduced to nearly zero after short anneals at modest temperatures (30 s at 600 °C). Poly-Ge is essentially impervious to KOH, TMAH, and BOE, enabling the fabrication of Ge membranes on Si substrates [11.30]. The mechanical properties of poly-Ge are comparable to those of polysilicon, having a Young's modulus of 132 GPa and a fracture stress ranging between 1.5 and 3.0 GPa [11.31]. Mixtures of HNO_3, H_2O, and HCl and H_2O, H_2O_2, and HCl, as well as the RCA SC-1 cleaning solution, isotropically etch Ge. Since these mixtures do not etch Si, SiO_2, Si_3N_4, and SiN, poly-Ge can be used as a sacrificial substrate layer in polysilicon surface micromachining. Using these techniques, devices such as poly-Ge-based thermistors and Si_3N_4 membrane-based pressure sensors made using poly-Ge sacrificial layers have been fabricated [11.30]. *Franke* et al. [11.31] found no performance degradation in Si CMOS devices following the fabrication of surface micromachined poly-Ge structures, thus demonstrating the potential for on-chip integration of Ge electromechanical devices with Si circuitry.

11.2.2 Polycrystalline SiGe

Like poly-Ge, polycrystalline SiGe (poly-SiGe) is a material that can be deposited at temperatures lower than polysilicon. Deposition processes include LPCVD, APCVD, and RTCVD (rapid thermal CVD) using SiH_4 and GeH_4 as precursor gases. Deposition temperatures range between 450 °C for LPCVD [11.32] and 625 °C by rapid thermal CVD (RTCVD) [11.33]. In general, the deposition temperature is related to the concentration of Ge in the films, with higher Ge concentrations resulting in lower deposition temperatures. Like polysilicon, poly-SiGe can be doped with boron and phosphorus to modify its conductivity. In situ boron doping can be performed at temperatures as low as 450 °C [11.32]. *Sedky* et al. [11.33] showed that the deposition temperature of conductive films doped with boron could be further reduced to 400 °C if the Ge content was kept at or above 70%.

Unlike poly-Ge, poly-SiGe can be deposited on a number of sacrificial substrates, including SiO_2 [11.33], PSG [11.31], and poly-Ge [11.31]. For Ge-rich films, a thin polysilicon seed layer is sometimes used on SiO_2 surfaces since Ge does not readily nucleate on oxide surfaces. Like many compound materials, variations in film composition can change the physical properties of the material. For instance, etching of poly-SiGe by H_2O_2 becomes significant for Ge concentrations over 70%. *Sedky* et al. [11.33] has shown that the microstructure, film conductivity, residual stress, and residual stress gradient are related to the concentration of Ge in the material. With respect to residual stress, *Franke* et al. [11.32] produced in situ boron-doped films with residual compressive stresses as low as 10 MPa.

The poly-SiGe, poly-Ge material system is particularly attractive for surface micromachining since H_2O_2 can be used as a release agent. It has been reported that poly-Ge etches at a rate of 0.4 μm/min in H_2O_2, while poly-SiGe with Ge concentrations below 80% have no observable etch rate after 40 h [11.34]. The ability to use H_2O_2 as a sacrificial etchant makes the combination of poly-SiGe and poly-Ge extremely attractive for surface micromachining from processing, safety, and materials compatibility points of view. Due to the conformal nature of LPCVD processing, poly-SiGe structural elements, such as gimbal-based microactuator structures have been made by high-aspect-ratio micromolding [11.34]. Capitalizing on the low deposition temperatures, poly-SiGe MEMS integrated with Si ICs has been demonstrated [11.32]. In this process, CMOS structures are first fabricated on Si wafers. Poly-SiGe mechanical structures are then surface micromachined using a poly-Ge sacrificial layer. A significant advantage of this design lies in the fact that the MEMS structure is positioned directly above the CMOS structure, thus reducing the parasitic capacitance and contact resistance characteristic of interconnects associated with side-by-side integration schemes. Use of H_2O_2 as the sacrificial etchant eliminates the need for layers to protect the underlying CMOS structure during release. In addition to its utility as a material for integrated MEMS devices, poly-SiGe has been identified as a material well suited for micromachined thermopiles [11.35] to its lower thermal conductivity relative to Si.

11.3 Metals

It can be argued that of all the material categories associated with MEMS, metals may be among the most enabling, since metallic thin films are used in many different capacities, from etch masks used in device

fabrication to interconnects and structural elements in microsensors and microactuators. Metallic thin films can be deposited using a wide range of techniques, including evaporation, sputtering, CVD, and electroplating. Since a complete review of the metals used in MEMS is far beyond the scope of this chapter, the examples presented in this section were selected to represent a broad cross section where metals have found uses in MEMS.

Aluminum (Al) and gold (Au) are among the most widely employed metals in microfabricated electronic and electromechanical devices as a result of their use as innerconnect and packaging materials. In addition to these critical electrical functions, Al and Au are also desirable as electromechanical materials. One such example is the use of Au micromechanical switches for RF MEMS. For conventional RF applications, chip level switching is currently performed using FET and PIN diode-based solid state devices fabricated from gallium arsenide (GaAs) substrates. Unfortunately, these devices suffer from insertion losses and poor electrical isolation. In an effort to develop replacements for GaAs-based solid state switches, *Hyman* et al. [11.36] reported the development of an electrostatically actuated, cantilever-based micromechanical switch fabricated on GaAs substrates. The device consisted of a silicon-nitride-encased Au cantilever constructed on a sacrificial silicon dioxide layer. The silicon nitride and silicon dioxide layers were deposited by PECVD, and the Au beam was electroplated from a sodium sulfite solution inside a photoresist mold. A thin multilayer of Ti and Au was sputter deposited in the mold prior to electroplating. The trilayer cantilever structure was chosen to minimize the deleterious effects of thermal- and process-related stress gradients in order to produce unbent and thermally stable beams. After deposition and pattering, the cantilevers were released in HF. The processing steps proved to be completely compatible with GaAs substrates. The released cantilevers demonstrated switching speeds of better than 50 µs at 25 V with contact lifetimes exceeding 10^9 cycles.

In a second example from RF MEMS, *Chang* et al. [11.37] reported the fabrication of an Al-based micromachined switch as an alternative to GaAs FETs and PIN diodes. In contrast to the work by *Hyman* et al. [11.36], this switch utilizes the differences in the residual stresses in Al and Cr thin films to create bent cantilever switches that capitalize on the stress differences in the materials. Each switch is comprised of a series of linked bimorph cantilevers designed in such a way that the resulting structure bends significantly out of the plane of the wafer due to the stress differences in the bimorph. The switch is drawn closed by electrostatic attraction. The bimorph consists of metals that can easily be processed with GaAs wafers, thus making integration with GaAs devices possible. The released switches were relatively slow, at 10 ms, but an actuation voltage of only 26 V was needed to close the switch.

Direct bulk micromachining of metal substrates is being developed for MEMS applications requiring structures with the dimensional complexity associated with Si DRIE and the physical properties of metals. One such example is Ti, which has a higher fracture toughness, a greater biocompatibility, and a more stable passivating oxide than Si. A process to fabricate high-aspect-ratio, three-dimensional structures from bulk Ti substrates has recently been developed [11.38]. This process involves inductively coupled plasma etching of a TiO_2-capped Ti substrate. The TiO_2 capping layer is deposited by DC reactive sputtering and photolithographically patterned using a CHF_3-based dry etch. The deep Ti etch is then performed using a Cl/Ar-based plasma that exhibits a selectivity of 40:1 with the masking TiO_2 layer. The etch process consists of a series of two-step sequences, where the first step involves Ti removal by the Cl/Ar plasma while the second step involves sidewall passivation using an oxygen plasma. After the prescribed etch period, the masking thin film can be removed by HF etching. High-aspect-ratio comb-drive actuators and other beam-based structures have been fabricated directly from bulk Ti using this method.

Thin-film metallic alloys that exhibit the shape-memory effect are of particular interest to the MEMS community for their potential in microactuators. The shape-memory effect relies on the reversible transformation from a ductile martensite phase to a stiff austenite phase in the material with the application of heat. The reversible phase change allows the shape-memory effect to be used as an actuation mechanism since the material changes shape during the transition. It has been found that high forces and strains can be generated from shape-memory thin films at reasonable power inputs, thus enabling shape memory actuation to be used in MEMS-based microfluidic devices such as microvalves and micropumps. Titanium-nickel (TiNi) is among the most popular of the shape-memory alloys owing to its high actuation work density, ($50\,MJ/m^3$), and large bandwidth (up to 0.1 kHz) [11.39]. TiNi is also attractive because conventional sputtering techniques can be employed to deposit thin films, as detailed

in a recent report by *Shih* et al. [11.39]. In this study, TiNi films were deposited by cosputtering elemental Ti and Ni targets and cosputtering TiNi alloy and elemental Ti targets. It was reported that cosputtering from TiNi and Ti targets produced better films due to process variations related to roughening of the Ni target in the case of Ti and Ni cosputtering. The TiNi/Ti cosputtering process has been used to produce shape-memory material for a silicon spring-based microvalve [11.40].

Use of thin-film metal alloys in magnetic actuator systems is another example of the versatility of metallic materials in MEMS. Magnetic actuation in microdevices generally requires the magnetic layers to be relatively thick (tens to hundreds of micrometer) to generate magnetic fields of sufficient strength to generate the desired actuation. To this end, magnetic materials are often deposited by thick-film methods such as electroplating. The thicknesses of these layers exceeds what can feasibly be patterned by etching, so plating is often performed in microfabricated molds made from materials such as polymethylmethacrylate (PMMA). The PMMA mold thickness can exceed several hundred micrometer, so x-rays are used as the exposure source during the patterning steps. When necessary a metallic thin-film seed layer is deposited prior to plating. After plating, the mold is dissolved, which frees the metallic component. Known as LIGA (short for lithography, galvanoforming, and abformung), this process has been used to produce a wide variety of high-aspect-ratio structures from plateable materials, such as nickel-iron (NiFe) magnetic alloys [11.41] and Ni [11.42].

In addition to elemental metals and simple compound alloys, more complex metallic alloys commonly used in commerical macroscopic applications are finding their way into MEMS applications. One such example is an alloy of titanium known as Ti-6Al-4V. Composed of 88% titanium, 6% aluminum, and 4% vanadium, this alloy is widely used in commercial avation due to its weight, strength, and temperature tolerance. *Pornsin-Sirirak* et al. [11.43] have explored the use of this alloy in the manufacture of MEMS-based winged structures for micro aerial vehicles. The authors considered this alloy not only because of its weight and strength, but also because of its ductility and its etching rate at room temperature. The designs for the wing prototype were modeled after the wings of bats and various flying insects. For this application, Ti-alloy structures patterned from bulk (250 μm thick) material by an $HF/HO_3/H_2O$ etching solution were used rather than thin films. Parylene-C (detailed in a later section) was deposited on the patterned alloy to serve as the wing membrane. The miniature micromachined wings were integrated into a test setup, and several prototypes actually demonstrated short duration flight.

11.4 Harsh-Environment Semiconductors

11.4.1 Silicon Carbide

Silicon carbide (SiC) has long been recognized as the leading semiconductor for use in high-temperature and high-power electronics and is currently being developed as a material for harsh-environment MEMS. SiC is a polymorphic material that exists in cubic, hexagonal, and rhombehedral polytypes. The cubic polytype, called 3C-SiC, has an electronic bandgap of 2.3 eV, which is over twice that of Si. Numerous hexagonal and rhombehedral polytypes have been identified, with the two most common being 4H-SiC and 6H-SiC. The electronic bandgaps of 4H- and 6H-SiC are even higher than 3C-SiC, being 2.9 and 3.2 eV, respectively. SiC films can be doped to create n-type and p-type materials. The Young's modulus of SiC is still the subject of research, but most reported values range from 300 to 450 GPa, depending on the microstructure and measurement technique. SiC is not etched in any wet Si etchants and is not attacked by XeF_2, a popular dry Si etchant used for releasing device structures [11.44]. SiC is a material that does not melt, but rather sublimes at temperatures in excess of 1800 °C. Single-crystal 4H- and 6H-SiC wafers are commercially available, but they are smaller in diameter (3 inch) and much more expensive than Si wafers.

SiC thin films can be grown or deposited using a number of different techniques. For high-quality single-crystal films, APCVD and LPCVD processes are most commonly employed. Homoepitaxial growth of 4H- and 6H-SiC yields high-quality films suitable for microelectronic applications but typically only on substrates of the same polytype. These processes usually employ dual precursors, such as SiH_4 and C_3H_8, and are performed at temperatures ranging from 1500 to 1700 °C. Epitaxial films with p-type or n-type conductivity can be grown using Al and B for p-type films and N and P for n-type films. Nitrogen is so effective

at modifying the conductivity of SiC that growth of undoped SiC films is extremely challenging because the concentrations of residual nitrogen in typical deposition systems are sufficient for n-type doping.

APCVD and LPCVD can also be used to deposit 3C-SiC on Si substrates. Heteroepitaxy is possible despite a 20% lattice mismatch because 3C-SiC and Si have the same lattice structure. The growth process involves two key steps. The first step, called carbonization, converts the near surface region of the Si substrate to 3C-SiC by simply exposing it to a hydrocarbon/hydrogen mixture at high substrate temperatures (> 1200 °C). The carbonized layer forms a crystalline template on which a 3C-SiC film can be grown by adding a silicon-containing gas to the hydrogen/hydrocarbon mix. The lattice mismatch between Si and 3C-SiC results in the formation of crystalline defects in the 3C-SiC film, with the density being highest in the carbonization layer and decreasing with increasing thickness. The crystal quality of 3C-SiC films is nowhere near that of epitaxially grown 4H- and 6H-SiC films; however, the fact that 3C-SiC can be grown on Si substrates enables the use of Si bulk micromachining techniques for fabrication of a host of 3C-SiC-based mechanical devices. These include microfabricated pressure sensors [11.45] and nanoelectromechanical resonant structures [11.46]. For designs that require electrical isolation from the substrate, 3C-SiC devices can be made directly on SOI substrates [11.45] or by wafer bonding and etchback, such as the capacitive pressure sensor developed by *Young* et al. [11.47].

Polycrystalline SiC (poly-SiC) is a more versatile material for SiC MEMS than its single-crystal counterparts. Unlike single-crystal versions of SiC, poly-SiC can be deposited on a variety of substrate types, including common surface micromachining materials such as polysilicon, SiO_2, and Si_3N_4. Commonly used deposition techniques include LPCVD [11.44, 48, 49] and APCVD [11.50, 51]. The deposition of poly-SiC requires much lower substrate temperatures than epitaxial films, ranging from roughly 700 to 1200 °C. Amorphous SiC can be deposited at even lower temperatures (25–400 °C) by PECVD [11.52] and sputtering [11.53]. The microstructure of poly-SiC films is temperature, substrate, and process dependent. For amorphous substrates such as SiO_2 and Si_3N_4, APCVD poly-SiC films deposited from SiH_4 and C_3H_8 are randomly oriented with equiaxed grains [11.51], whereas for oriented substrates such as polysilicon, the texture of the poly-SiC film matches that of the substrate itself [11.50]. By comparison, poly-SiC films deposited by LPCVD from SiH_2Cl_2 and C_2H_2 are highly textured (111) films with a columnar microstructure [11.48], while films deposited from disilabutane have a distribution of orientations [11.44]. This variation suggests that device performance can be tailored by selecting the proper substrate and deposition conditions.

SiC films deposited by AP- and LPCVD generally suffer from large tensile stresses on the order of several hundred MPa. Moreover, the residual stress gradients in these films tend to be large, leading to significant out-of-plane bending of structures that are anchored at a single location. The thermal stability of SiC makes a postdeposition annealing step impractical for films deposited on Si substrates, since the temperatures needed to significantly modify the film are likely to exceed the melting temperature of the wafer. For LPCVD processes using SiH_2Cl_2 and C_2H_2 precursors, *Fu* et al. [11.54] has described a relationship between deposition pressure and residual stress that enables the deposition of undoped poly-SiC films with nearly zero residual stresses and negligible stress gradients. This work has recently been extended to include films doped with nitrogen [11.55].

Direct bulk micromachining of SiC is very difficult, due to its chemical inertness. Although conventional wet chemical techniques are not effective, several electrochemical etch processes have been demonstrated and used in the fabrication of 6H-SiC pressure sensors [11.56]. The etching processes are selective to the conductivity of the material, so dimensional control of the etched structures depends on the ability to form doped layers, which can only be formed by in situ or ion-implantation processes since solid source diffusion is not possible at reasonable processing temperatures. This constraint somewhat limits the geometrical complexity of the patterned structures as compared with conventional plasma-based etching. To fabricate thick (hundreds of micrometer), 3-D, high-aspect-ratio SiC structures, a molding technique has been developed [11.42]. The molds are fabricated from Si substrates using deep reactive ion etching and then filled with SiC using a combination of thin epitaxial and thick polycrystalline film CVD processes. The thin-film process is used to protect the mold from pitting during the more aggressive mold-filling SiC growth step. The mold-filling process coats all surfaces of the mold with a SiC film as thick as the mold is deep. To release the SiC structure, the substrate is first mechanically polished to expose sections

of the Si mold; then the substrate is immersed in a Si etchant to completely dissolve the mold. This process has been used to fabricate solid SiC fuel atomizers [11.42], and a variant has been used to fabricate SiC structures for micropower systems [11.57]. Recently, *Min* et al. [11.58] reported a process to fabricate reusable glass press molds made from SiC structures that were patterned using Si molding masters. SiC was selected as the material for the glass press mold because the application requires a hard, mechanically strong, and chemically stable material that can withstand and maintain its properties at temperatures between 600 and 1400 °C.

In addition to CVD processes, bulk micromachined SiC structures can be fabricated using sintered SiC powders. *Tanaka* et al. [11.59] describe a process where SiC components, such as micro gas turbine engine rotors, can be fabricated from SiC powders using a microreaction-sintering process. The molds are microfabricated from Si using DRIE and filled with SiC and graphite powders mixed with a phenol resin. The molds are then reaction-sintered using a hot isostatic pressing technique. The SiC components are then released from the Si mold by wet chemical etching. The authors reported that the component shrinkage was less than 3%. The bending strength and Vickers hardness of the microreaction-sintered material was roughly 70 to 80% of commercially available reaction-sintered SiC, the difference being attributed to the presence of unreacted Si in the microscale components.

In a related process, *Liew* et al. [11.60] detail a technique to create silicon carbon nitride (SiCN) MEMS structures by molding injectable polymer precursors. Unlike the aforementioned processes, this technique uses SU-8 photoresists for the molds. To be detailed later in this chapter, SU-8 is a versatile photodefinable polymer in which thick films (hundreds of micrometer) can be patterned using conventional UV photolithographic techniques. After patterning, the molds are filled with the SiCN-containing polymer precursor, lightly polished, and then subjected to a multistep heat-treating process. During the thermal processing steps, the SU-8 mold decomposes and the SiCN structure is released. The resulting SiCN structures retain many of the same properties of stoichiometric SiC.

Although SiC cannot be etched using conventional wet etch techniques, SiC can be patterned using conventional dry etching techniques. RIE processes using fluorinated compounds such as CHF_3 and SF_6 combined with O_2 and sometimes with an inert gas or H_2 are used to pattern thin films. The high oxygen content in these plasmas generally prohibits the use of photoresist as a masking material; therefore, hard masks made of Al, Ni, and ITO are often used. RIE-based SiC surface micromachining processes with polysilicon and SiO_2 sacrificial layers have been developed for single-layer devices [11.61, 62]. ICP RIE of SiC using SF_6 plasmas and Ni or ITO etch masks has been developed for bulk micromachining SiC substrates, with structural depths in excess of 100 μm reported [11.63].

Until recently, multilayer thin-film structures were very difficult to fabricate by direct RIE because the etch rates of the sacrificial layers were much higher than the SiC structural layers, making dimensional control very difficult. To address this issue, a micromolding process for patterning SiC films on sacrificial-layer substrates was developed [11.64]. In essence, the micromolding technique is the thin-film analog to the molding-based, bulk micromachining technique presented earlier. The micromolding process utilizes polysilicon and SiO_2 films as both molds and sacrificial substrate layers, with SiO_2 molds used with polysilicon sacrificial layers and vice versa. These films are deposited and patterned using conventional methods, thus leveraging the well-characterized and highly selective processes developed for polysilicon MEMS. Poly-SiC films are simply deposited into the micromolds and mechanical polishing is used to remove poly-SiC from atop the molds. Appropriate etchants are then used to dissolve the molds and sacrificial layers. The micromolding method utilizes the differences in chemical properties of the three materials in this system in a way that bypasses the difficulties associated with chemical etching of SiC. This technique has been developed specifically for multilayer processing and has been used successfully to fabricate SiC micromotors [11.64] and the lateral resonant structure shown in Fig. 11.4 [11.65].

Recent advancements in the area of SiC RIE show that significant progress has been made in developing etch recipes with selectivities to nonmetal mask and sacrificial layers that are suitable for multilayer SiC surface micromachining. For instance, *Gao* et al. [11.66] have developed a transformer-coupled RIE process using a HBr-based chemistry for thin-film poly-SiC etching. The recipe exhibits a SiC-to-SiO_2 selectivity of 20:1 and a SiC-to-Si_3N_4 selectivity of 22:1, which are the highest reported thus far. In addition, the anisotropy of the etch was quite high, and micromasking, a common problem when metal masks are used, was not an issue. This process has since been used to fabricate multilayered lateral resonant structures that utilize poly-SiC as the main structural material and polysilicon as

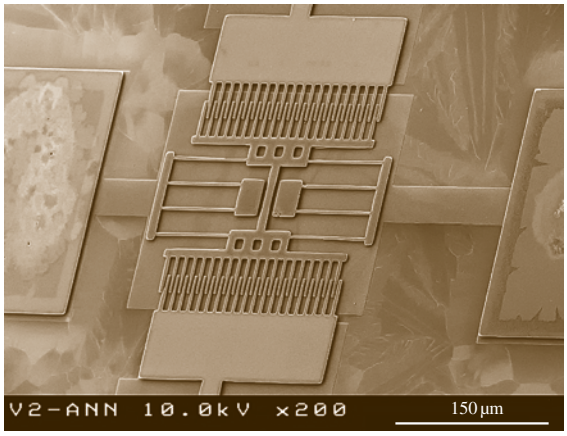

Fig. 11.4 SEM micrograph of a poly-SiC lateral resonant structure fabricated using a multilayer, micromolding-based micromachining process (after [11.65])

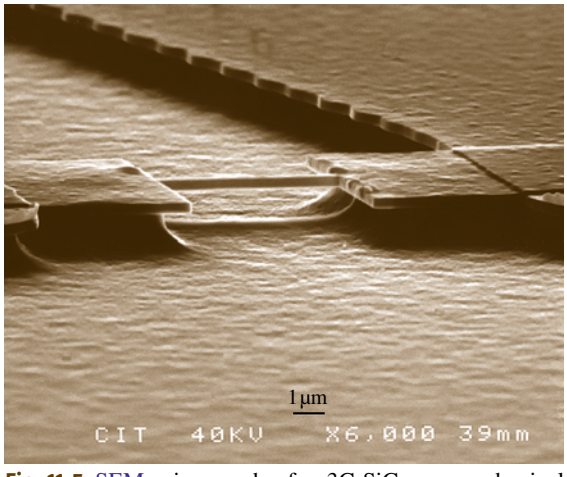

Fig. 11.5 SEM micrograph of a 3C-SiC nanomechanical beam resonator fabricated by electron-beam lithography and dry etching processes (courtesy of M. Roukes, Caltech)

a conducting plane that underlies the resonating shuttle [11.66].

Yang et al. [11.46] have recently shown that the chemical inertness of SiC facilitates the fabrication of NEMS devices. In this work, the authors present a fabrication method to realize SiC mechanical resonators with submicrometer thickness and width dimensions. The resonators were fabricated from ≈ 260 nm thick 3C-SiC films epitaxially grown on (100) Si wafers. The films were patterned into 150 nm wide beams ranging in length from 2 to 8 µm. The beams were etched in a $NF_3/O_2/Ar$ plasma using an evaporated Cr etch mask. After patterning, the beams were released by etching the underlying Si isotropically using a NF_3/Ar plasma. The inertness of the SiC film to the Si etchant enables the dry release of the nanomechanical beams. An example of a 3C-SiC nanomechanical beam is shown in Fig. 11.5.

11.4.2 Diamond

Diamond is commonly known as nature's hardest material, making it ideal for high wear environments. Diamond has a very large electronic bandgap (5.5 eV), which makes it attractive for high temperature electronics. Undoped diamond is a high-quality insulator with a dielectric constant of 5.5; however, it can be relatively easily doped with boron to create p-type conductivity. Diamond has a very high Young's modulus (1035 GPa), making it suitable for high-frequency micromachined resonators, and it is among nature's most chemically inert materials, making it well suited for harsh chemical environments.

Unlike SiC, fabrication of diamond MEMS is currently restricted to polycrystalline and amorphous material, since single-crystal diamond wafers are not yet commercially available. Polycrystalline diamond films can be deposited on Si and SiO_2 substrates by CVD methods, but the surfaces must often be seeded by diamond powders or biased with a negative charge to initiate growth. In general, diamond nucleates much more readily on Si surfaces than on SiO_2 surfaces, an effect that has been used to selectively pattern diamond films into micromachined AFM cantilever probes using SiO_2 molding masks [11.67].

Bulk micromachining of diamond using wet and dry etching is extremely difficult given its extreme chemical inertness. Diamond structures have nevertheless been fabricated using bulk micromachined Si molds to pattern the structures [11.68]. The Si molds were fabricated using conventional micromachining techniques and filled with polycrystalline diamond deposited by hot filament chemical vapor deposition (HFCVD). The HFCVD process uses H_2 and CH_4 precursors. The process was performed at a substrate temperature of 850–900 °C and a pressure of 50 mtorr. The Si substrate was seeded prior to deposition using a diamond particle/ethanol solution. After deposition, the top surface of the structure was polished using a hot iron plate. After polishing, the Si mold was removed in a Si etchant, leaving behind the micromachined diamond structure. This process was used to produce high-aspect-ratio capillary channels for microfluidic applications [11.69] and components for diffractive op-

tics, laser-to-fiber alignment, and power device cooling structures [11.70].

Due to the nucleation processes associated with diamond film growth, surface micromachining of polycrystalline diamond thin films requires modifications to conventional micromachining to facilitate film growth on sacrificial substrates. Initially, conventional RIE methods were generally ineffective, so work was focused on developing selective deposition techniques. One early method used selective seeding to form patterned templates for diamond nucleation. The selective seeding process employed the lithographic patterning of photoresist that contained diamond powders [11.71]. The diamond-loaded photoresist was deposited and patterned onto a Cr-coated Si wafer. During the onset of diamond growth, the patterned photoresist rapidly evaporates, leaving behind the diamond seed particles in the desired locations. A patterned diamond film is then selectively grown on these locations.

A second process utilized selective deposition directly on sacrificial substrate layers. This process combined conventional diamond seeding with photolithographic patterning and etching to fabricate micromachined diamond structures on SiO_2 sacrificial layers [11.72]. The process was performed in one of two ways. The first approach begins with the seeding of an oxidized Si wafer. The wafer is coated with a photoresist and photolithographically patterned. Unmasked regions of the seeded SiO_2 film are then partially etched, forming a surface unfavorable for diamond growth. The photoresist is then removed and a diamond film is deposited on the seeded regions. The second approach also begins with an oxidized Si wafer. The wafer is coated with a photoresist, photolithographically patterned, and then seeded with diamond particles. The photoresist is removed, leaving behind a patterned seed layer suitable for selective growth. These techniques have been successfully used to fabricate cantilever beams and bridge structures.

A third method to surface micromachine polycrystalline diamond films follows the conventional approach of film deposition, dry etching, and release. The chemical inertness of diamond renders most conventional plasma chemistries useless; however, oxygen-based ion-beam plasmas can be used to etch diamond thin films [11.73]. A simple surface micromachining process begins with the deposition of a polysilicon sacrificial layer on a Si_3N_4-coated Si wafer. The polysilicon layer is seeded using diamond slurry, and a diamond film is deposited by HFCVD. Since photoresists are not resistant to O_2 plasmas, an Al masking film is deposited and patterned. The diamond films are then etched in the O_2 ion-beam plasma, and the structures are released by etching the polysilicon with KOH. This process has been used to create lateral resonant structures, but a significant stress gradient in the films rendered the devices inoperable.

In general, conventional HFCVD requires that the substrate be pretreated with a seeding layer prior to diamond film growth. However, a method called biased enhanced nucleation (BEN) has been developed that enables the growth of diamond on unseeded Si surfaces. *Wang* et al. [11.74] have shown that if Si substrates are masked with patterned SiO_2 films, selective diamond growth will occur primarily on the exposed Si surfaces, and a slight HF etch is sufficient to remove the adventitious diamond from the SiO_2 mask. This group was able to use this method to fabricate diamond micromotor rotors and stators on Si surfaces.

Diamond is a difficult, but not impossible, material to etch using conventional RIE techniques. It is well known that diamond can be etched in oxygen plasmas, but these plasmas can be problematic for device fabrication because the etching tends to be isotropic. A recent development, however, suggests that RIE processes for diamond are close at hand. *Wang* et al. [11.74] describe a process to fabricate a vertically actuated, doubly clamped micromechanical diamond beam resonator using RIE. The process outlined in this paper addresses two key issues related to diamond surface micromachining, namely, residual stress gradients in the diamond films and diamond patterning techniques. A microwave plasma CVD (MPCVD) reactor was used to grow the diamond films on sacrificial SiO_2 layers pretreated with a nanocrystalline diamond powder, resulting in a uniform nucleation density at the diamond/SiO_2 interface. The diamond films were etched in a CF_4/O_2 plasma using Al as a hard mask. Reasonably straight sidewalls were created, with roughness attributable to the surface roughness of the faceted diamond film. An Au/Cr drive electrode beneath the sacrificial oxide remained covered throughout the diamond-patterning steps and thus was undamaged during the diamond-etching process. This work has since been extended to develop a 1.51 GHz diamond micromechanical disk resonator [11.74]. In this instance, the nanocrystalline diamond film was deposited my MPCVD, coated with an oxide film that had been patterned into an etch mask, and then etched in a O_2/CF_4 RIE plasma under conditions that yielded a fairly anisotropic etch with a diamond-to-oxide selectivity of 15:1. The disk was suspended over the substrate on a polysilicon stem using

an oxide sacrificial layer. Polysilicon was also used as the drive and sense electrodes. The material mismatch between the step and the resonating disk substantially reduced anchor losses, thus allowing for very high-quality factors (11, 500) for 1.5 GHz resonators tested in a vacuum.

In conjunction with recent advances in RIE and micromachining techniques, work is being performed to develop diamond-deposition processes specifically for MEMS applications. Diamond films grown using conventional techniques, especially processes that require pregrowth seeding, tend to have high residual stress gradients and roughened surface morphologies as a result of the highly faceted, large-grain polycrystalline films that are produced by these methods (Fig. 11.6). The rough surface morphology degrades the patterning process, resulting in roughened sidewalls in etched structures and roughened surfaces of films deposited over these layers. Unlike polysilicon and SiC, a postdeposition polishing process is not technically feasible for diamond due to its extreme hardness. For the fabrication of multilayer diamond devices, methods to reduce the surface roughness of the as-deposited films are highly desirable. Along these lines, *Krauss* et al. [11.75] have reported on the development of an ultrananocrystalline diamond (UCND) film that exhibits a much smoother surface morphology than comparable diamond films grown using conventional methods. Unlike conventional CVD diamond films that are grown using a mixture of H_2 and CH_4, the ultrananocrystalline diamond films are grown from mixtures of Ar, H_2, and C_{60} or Ar, H_2, and CH_4. Films produced by this method have proven to be effective as conformal coatings on Si surfaces and have been used successfully in several surface micromachining processes. Recently, this group has extended the UCND deposition technology to low deposition temperatures, with high-quality nanocrystalline diamond films being deposited at rates of 0.2 μm/h at substrate temperatures of 400 °C, making these films compatible from a thermal budget perspective with Si IC technology [11.76].

Another alternative deposition method that is proving to be well suited for diamond MEMS is based on pulsed laser deposition [11.77]. The process is performed in a high vacuum chamber and uses a pulsed eximer laser to ablate a pyrolytic graphite target. Material from the ejection plume deposits on a substrate, which is kept at room temperature. Background gases composed of N_2, H_2, and Ar can be introduced to adjust the deposition pressure and film properties. The as-deposited films consist of tetrahedrally bonded carbon that is amorphous in microstructure, hence the name amorphous diamond. Nominally stress-free films can be deposited by proper selection of deposition parameters [11.78] or by a short postdeposition annealing step [11.77]. The amorphous diamond films exhibit many of the properties of single-crystal diamond, such as a high hardness (88 GPa), a high Young's modulus (1100 GPa), and chemical inertness. Many single-layer surface micromachined structures have been fabricated using these films, in part because the films can be readily deposited on oxide sacrificial layers and etched in an oxygen plasma. Recently, amorphous diamond films have been used as a dielectric isolation layer in vertically actuated microbridges in micromachined RF capacitive switches [11.79]. The diamond films sit atop fixed tungsten electrodes to provide dielectric isolation from an Au microbridge that spans the fixed electrode structure. The diamond films are particularly attractive for such applications since the surfaces are hydrophobic and thus do not suffer from stiction and are highly resistant to wear over repeated use.

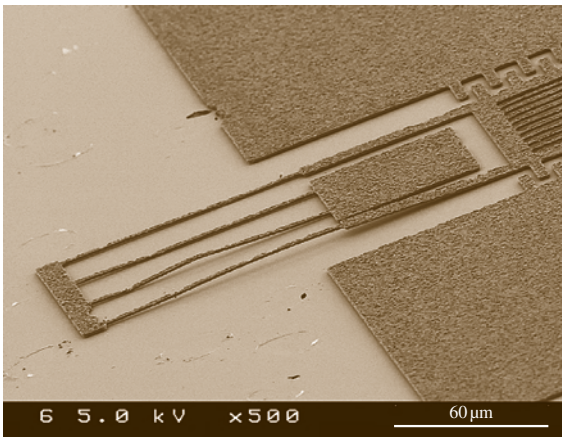

Fig. 11.6 SEM micrograph of the folded beam truss of diamond lateral resonator. The diamond film was deposited using a seeding-based hot filament CVD process. The micrograph illustrates the challenges facing MEMS structures made from polycrystalline material, namely roughened surfaces and residual stress gradients

11.5 GaAs, InP, and Related III–V Materials

Gallium arsenide (GaAs), indium phosphide (InP), and related III–V compounds have favorable piezoelectric and optoelectric properties, high piezoresistive constants, and wide electronic bandgaps relative to Si, making them attractive for various sensor and optoelectronic applications. Like Si, significant research in bulk crystal growth has led to the development of GaAs and InP substrates that are commercially available as high-quality, single-crystal wafers. Unlike compound semiconductors such as SiC, III–V materials can be deposited as ternary and quaternary alloys with lattice constants that closely match the binary compounds from which they are derived (i. e., $Al_xGa_{1-x}As$ and GaAs), thus permitting the fabrication of a wide variety of heterostructures that facilitate device performance.

Crystalline GaAs has a zinc blend crystal structure with an electronic bandgap of 1.4 eV, enabling GaAs electronic devices to function at temperatures as high as 350 °C [11.80]. High-quality, single-crystal wafers are commercially available, as are well-developed metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) growth processes for epitaxial layers of GaAs and its alloys. GaAs does not outperform Si in terms of mechanical properties; however, its stiffness and fracture toughness are still suitable for micromechanical devices.

Micromachining of GaAs is relatively straightforward, since many of its lattice-matched ternary and quaternary alloys have sufficiently different chemical properties to allow their use as sacrificial layers [11.81]. For example, the most common ternary alloy for GaAs is $Al_xGa_{1-x}As$. For values of x less than or equal to 0.5, etchants containing mixtures of HF and H_2O will etch $Al_xGa_{1-x}As$ without attacking GaAs, while etchants containing NH_4OH and H_2O_2 attack GaAs isotropically but do not etch $Al_xGa_{1-x}As$. Such selectivity enables the micromachining of GaAs wafers using lattice-matched etch stops and sacrificial layers. Devices fabricated using these methods include comb drive lateral resonant structures [11.81], pressure sensors [11.82, 83], thermopile sensors [11.83], Fabry–Perot detectors [11.84], and cantilever-based sensors and actuators [11.85, 86]. In addition, nanoelectromechanical devices, such as suspended micromechanical resonators [11.87] and tethered membranes [11.88], have been fabricated using these techniques. An example of a nanoelectromechanical beam structure fabricated from GaAs is shown in Fig. 11.7.

In addition to using epitaxial layers as etch stops, ion-implantation methods can also be used to produce etch stops in GaAs layers. *Miao* et al. [11.89] describe a process that uses electrochemical etching to selectively remove n-type GaAs layers. The process relies on the creation of a highly resistive near-surface GaAs layer on an n-type GaAs substrate by low-dose nitrogen implantation in the MeV energy range. A pulsed electrochemical etch method using an H_2PtCl_6, H_3PO_4, H_2SO_4 platinum electrolytic solution at 40 °C with 17 V, 100 ms pulses is sufficient to selectively remove n-type GaAs at about 3 μm/min. Using this method, stress-free, tethered membranes could readily be fabricated from the highly resistive GaAs layer. The high implant energies enable the fabrication of membranes several micrometer thick. Moreover, the authors demonstrated that if the GaAs wafer were etched in such a way as to create an undulating surface prior to ion implantation, corrugated membranes could be fabricated. These structures can sustain much higher deflection amplitudes than flat structures.

Micromachining of InP closely resembles the techniques used for GaAs. Many of the properties of InP are similar to GaAs in terms of crystal structure, mechanical stiffness, and hardness; however, the optical properties of InP make it particularly attractive for microoptomechanical devices to be used in the 1.3–1.55 μm wavelength range [11.90]. Like GaAs, single-crystal

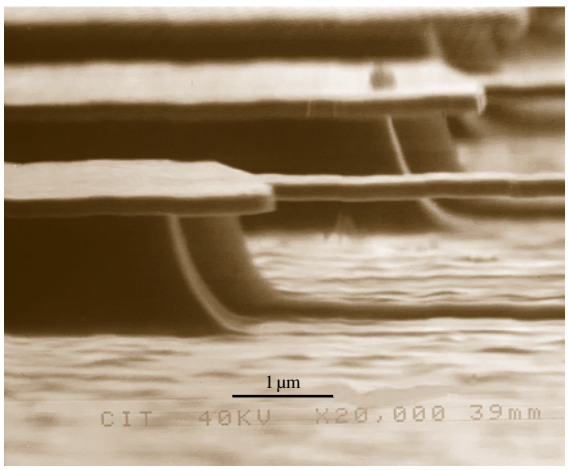

Fig. 11.7 SEM micrograph of a GaAs nanomechanical beam resonator fabricated by epitaxial growth, electron-beam lithography, and selective etching (courtesy of M. Roukes, Caltech)

wafers of InP are readily available, and ternary and quaternary lattice-matched alloys, such as InGaAs, InAlAs, InGaAsP, and InGaAlAs, can be used as either etch stop and/or sacrificial layers depending on the etch chemistry [11.81]. For instance, InP structural layers deposited on $In_{0,53}Al_{0,47}As$ sacrificial layers can be released using etchants containing $C_6H_8O_7$, H_2O_2, and H_2O. In addition, InP films and substrates can be etched in solutions containing HCl and H_2O using $In_{0,53}Ga_{0,47}As$ films as etch stops. Using InP-based micromachining techniques, multiair gap filters [11.91] bridge structures [11.90], and torsional membranes [11.84] have been fabricated from InP and its related alloys.

In addition to GaAs and InP, materials such as indium arsenide (InAs) can be micromachined into device structures. Despite a 7% lattice mismatch between InAs and (111) GaAs, high-quality epitaxial layers can be grown on GaAs substrates. As described by *Yamaguchi* et al. [11.92], the surface Fermi level of InAs/GaAs structures is pinned in the conduction band, enabling the fabrication of very thin conductive membranes. In fact, the authors have successfully fabricated free-standing InAs structures that range in thickness from 30 to 300 nm. The thin InAs films were grown directly on GaAs substrates by MBE and etched using a solution containing H_2O, H_2O_2, and H_2SO_4. The structures, mainly doubly clamped cantilevers, were released by etching the GaAs substrate using an $H_2O/H_2O_2/NH_4OH$ solution.

11.6 Ferroelectric Materials

Piezoelectric materials play an important role in MEMS technology for sensing and mechanical actuation applications. In a piezoelectric material, mechanical stress produces a polarization, and conversely a voltage-induced polarization produces a mechanical stress. Many asymmetric materials, such as quartz, GaAs, and zinc oxide (ZnO), exhibit some piezoelectric behavior. Recent work in MEMS has focused on the development of ferroelectric compounds such as lead zirconate titanate, $Pb(Zr_xTi_{1-x})O_3$, or PZT for short, because such compounds have high piezoelectric constants that result in high mechanical transduction. It is relatively straightforward to fabricate a PZT structure on top of a thin free-standing structural layer (i. e., cantilever, diaphragm). Such a capability enables the piezoelectric material to be used in sensor applications or actuator applications where piezoelectric materials are particularly well suited. Like Si, PZT films can be patterned using dry etch techniques based on chlorine chemistries, such as Cl_2/CCl_4, as well as ion-beam milling using inert gases like Ar.

PZT has been successfully deposited in thin-film form using cosputtering, CVD, and sol-gel processing. So-gel processing is particularly attractive because the composition and homogeneity of the deposited material over large surface areas can be readily controlled. The sol gel process outlined by *Lee* et al. [11.93] uses PZT solutions made from liquid precursors containing Pb, Ti, Zr, and O. The solution is deposited by spin coating on a Si wafer that has been coated with a $Pt/Ti/SiO_2$ thin-film multilayer. The process is executed to produce a PZT film in layers, with each layer consisting of a spin-coated layer that is dried at 110 °C for 5 min and then heat-treated at 600 °C for 20 min. After building up the PZT layer to the desired thickness, the multilayer was heated at 600 °C for up to 6 h. Prior to this anneal, a PbO top layer was deposited on the PZT surface. An Au/Cr electrode was then sputter-deposited on the surface of the piezoelectric stack. This process was used to fabricate a PZT-based force sensor. *Xu* et al. [11.94] describe a similar sol-gel process to produce 12 μm thick, crack-free PZT films on Pt-coated Si wafers and 5 μm thick films on insulating ZrO_2 layers to produce micromachined MHz-range two-dimensional transducer arrays for acoustic imaging.

Thick-film printing techniques for PZT have been developed to produce thick films in excess of 100 μm. Such thicknesses are desired for applications that require actuation forces that cannot be achieved with the much thinner sol-gel films. *Beeby* et al. [11.95] describe a thick-film printing process whereby a PZT paste is made from a mixture of 95% PZT powder, 5% lead borosilicate powder, and an organic carrier. The paste was then printed through a stainless steel screen using a thick-film printer. Printing was performed on an oxidized Si substrate that is capped with a Pt electrode. After printing, the paste was dried and then fired at 850–950 °C. Printing could be repeated to achieve the desired thickness. The top electrode consisted of an evaporated Al film. The authors found that it was possible to perform plasma-based processing on the printed substrates but that the porous nature of the printed PZT films made them unsuitable for wet chemical processing.

11.7 Polymer Materials

11.7.1 Polyimide

Polyimides comprise an important class of durable polymers that are well suited for many of the techniques used in conventional MEMS processing. In general, polyimides can be acquired in bulk or deposited as thin films by spin coating, and they can be patterned using conventional dry etching techniques and processed at relatively high temperatures. These attributes make polyimides an attractive group of polymers for MEMS that require polymer structural and/or substrate layers, such as microfabricated biomedical devices where inertness and flexibility are important parameters.

Shearwood et al. [11.96] explored the use of polyimides as a robust mechanical material for microfabricated audio membranes. The authors fabricated 7 μm thick, 8 mm diameter membranes on GaAs substrates by bulk micromachining the GaAs substrate using a NH_3/H_2O_2 solution. They realized 100% yield and, despite a low Young's modulus (≈ 3 GPa), observed flat membranes to within 1 nm after fabrication.

Jiang et al.[11.97] capitalized on the strength and flexibility of polyimides to fabricate a flexible sheer-stress sensor array based on Si sensors. The sensor array consisted of a collection of Si islands linked by two polyimide layers. Each Si sensor island was 250 × 250 μm^2 in area and 80 μm in thickness. Al was used as an electrical innerconnect layer. The two polyimide layers served as highly flexible hinges, making it possible to mount the sensor array on curved surfaces. The sensor array was successful in profiling the shear-stress distribution along the leading edge of a rounded delta wing.

The chemical and temperature durability of polyimides enables their use as a sacrificial layer for a number of commonly used materials, such as evaporated or sputter-deposited metals. *Memmi* et al. [11.98] developed a fabrication process for capacitive micromechanical ultrasonic transducers using a polyimide as a sacrificial layer. The authors showed that the polyimide could withstand the conditions used to deposit silicon monoxide by evaporation and silicon nitride by PECVD at 400 °C. Recent work by *Bagolini* et al. [11.99] has shown that polyimides can even be used as sacrificial layers for PECVD SiC.

In the area of microfabricated biomedical devices, polyimides are receiving attention as a substrate material for implantable devices, owing to their potential biocompatiblity and mechanical flexibility. *Stieglitz* [11.100] reported on the fabrication of multichannel microelectrodes on polyimide substrates. Instead of using polyimide sheets as starting substrates, Si carrier wafers coated with a 5 μm thick polyimide film were used. Pt microelectrodes were then fabricated on these substrates using conventional techniques. Thin polyimide layers were deposited between various metal layers to serve as insulating layers. A capping polyimide layer was then deposited on the top of the substrates, and then the entire polyimide/metal structure was peeled off the Si carrier wafers. Backside processing was then performed on the free-standing polyimide structures to create devices that have exposed electrodes on both surfaces. In a later paper, *Stieglitz* et al. [11.101] describe a variation of this process for neural prostheses.

11.7.2 SU-8

SU-8 is a negative-tone epoxylike photoresist that is receiving much attention for its versatility in MEMS processing. It is a high-aspect-ratio, UV-sensitive resist designed for applications requiring single-coat resists with thicknesses on the order of 500 μm [11.102]. SU-8 has favorable chemical properties that enable it to be used as a molding material for high-aspect-ratio electroplated structures (as an alternative to LIGA) and as a structural material for microfluidics [11.102]. In terms of mechanical properties, *Lorenz* et al. [11.103] reported that SU-8 has a modulus of elasticity of 4.02 GPa, which compares favorably with a commonly-used polyamid (3.4 GPa).

In addition to the above-mentioned conventional uses for SU-8, several interesting alternative uses are beginning to appear in the literature. *Conradie* et al. [11.104] have used SU-8 to trim the mass of silicon paddle oscillators as a means to adjust the resonant frequency of the beams. The trimming process involves the patterning of SU-8 posts on Si paddles. The process capitalizes on the relative chemical stability of the SU-8 resin in conjunction with the relatively large masses that can be patterned using standard UV exposure processes.

SU-8 is also of interest as a bonding layer material for wafer bonding processes using patterned bonding layers. *Pan* et al. [11.105] compared several UV photodefinable polymeric materials and found that SU-8 exhibited the highest bonding strength (20.6 MPa) for layer thicknesses up to 100 μm.

11.7.3 Parylene

Parylene (poly-paraxylylene) is another emerging polymeric MEMS material due in large part to its biocompatibility. It is particularly attractive from the fabrication point of view because it can be deposited by CVD at room temperature. Moreover, the deposition process is conformal, which enables parylene coatings to be applied to prefabricated structures, such as Si microneedles [11.106], low-stress silicon nitride membrane particle filters [11.73], and micromachined polyimide/Au optical scanners [11.107]. In the former cases, the parylene coating served to strengthen the microfabricated structures, while in the latter case it served to protect the structure from condensing water vapor.

In addition to its function as a protective coating, parylene can actually be micromachined into free-standing components. *Noh* et al. [11.108] demonstrated a method to create bulk micromachined parylene microcolumns for miniature gas chromatographs. The structure is fabricated using a micromolding technique where Si molds are fabricated by DRIE and coated with parylene to form three sides of the microcolumn. A second wafer is coated with parylene, and the two are bonded together via a fusion bonding process. After bonding, the structure is released from the Si mold by KOH etching. In a second example, *Yao* et al. [11.109] describe a dry release process for parylene surface micromachining. In this process, sputtered Si is used as a sacrificial layer onto which a thick sacrificial photoresist is deposited. Parylene is then deposited on the photoresist and patterned into the desired structural shape. The release procedure is a two-step process. First the photoresist is dissolved in acetone. This results in the parylene structure sticking to the sputtered Si. Next, a dry BrF_3 etch is performed that dissolves the Si and releases the parylene structures. Parylene beams that were 1 mm long and 4.5 μm thick were successfully fabricated using this technique.

11.7.4 Liquid Crystal Polymer

Liquid crystal polymer (LCP) is a high-performance thermoplastic currently being used in printed circuit board and electronics packaging applications and has recently been investigated for use in MEMS applications requiring a material that is mechanically flexible, electrically insulating, chemically durable, and impermeable to moisture. LCP can be bonded to itself and other substrate materials such as glass and Si by thermal lamination. It can be micromachined using an oxygen plasma and yet is highly resistant to HF and many metal etchants [11.110]. The moisture absorption is less than 0.02% as compared with about 1% for polyimide [11.111], making it well suited as a packaging material.

Applications where LCPs are used as a key component in a MEMS device are beginning to emerge. *Faheem* et al. [11.112] reported on the use of LCP for encapsulation of variable RF MEMS capacitors. In this example, LCP, dispensed in liquid form, was used to join and seal a glass microcap to a prefabricated, microbridge capacitor. LCP was chosen in part because in addition to the aforementioned properties, it has very low RF loss characteristics, making it very well suited as an RF MEMS packaging material. *Wang* et al. [11.110] showed that LCP is a very versatile material that is highly compatible with many standard Si-based processing techniques. They also showed that micromachining techniques can be used to make LCP cantilever flow sensors that incorporate metal strain gauges and LCP membrane tactile sensors using NiCr strain gauges. *Lee* et al. [11.111] has developed a LCP-based, mechanically flexible, multichannel microelectrode array structure for neural stimulation and recording.

11.8 Future Trends

The rapid expansion of MEMS in recent years is due in large part to the inclusion of new materials that have expanded the functionality of microfabricated devices beyond what is achievable in silicon. This trend will certainly continue as new application areas for micro- and nanofabricated devices are identified. Many of these applications will likely require both new materials and new processes to fabricate the micro- and nanomachined devices for these yet-to-be-identified applications. Currently, conventional micromachining techniques employ a *top-down* approach that begins with either bulk substrates or thin films. Future MEMS and NEMS will likely incorporate materials that are created using a *bottom-up* approach. A significant chal-

lenge facing device design and fabrication engineers alike will be how to marry top-down and bottom-up approaches to create devices and systems that cannot be made using either process alone.

References

11.1 C.S. Smith: Piezoresistive effect in germanium and silicon, Phys. Rev. **94**, 1–10 (1954)

11.2 A.N. Cleland, M.L. Roukes: Fabrication of high frequency nanometer scale mechanical resonators from bulk Si crystals, Appl. Phys. Lett. **69**, 2653–2655 (1996)

11.3 D.W. Carr, H.G. Craighead: Fabrication of nanoelectromechanical systems in single crystal silicon using silicon on insulator substrates and electron beam lithography, J. Vac. Sci. Technol. B **15**, 2760–2763 (1997)

11.4 T. Kamins: *Polycrystalline Silicon for Integrated Circuits and Displays*, 2nd edn. (Kluwer, Boston 1988)

11.5 J.J. McMahon, J.M. Melzak, C.A. Zorman, J. Chung, M. Mehregany: Deposition and characterization of in-situ boron doped polycrystalline silicon films for microelectromechanical systems applications, Mater. Res. Symp. Proc. **605**, 31–36 (2000)

11.6 L. Cao, T.S. Kin, S.C. Mantell, D. Polla: Simulation and fabrication of piezoresistive membrane type MEMS strain sensors, Sens. Actuators **80**, 273–279 (2000)

11.7 H. Guckel, T. Randazzo, D.W. Burns: A simple technique for the determination of mechanical strain in thin films with application to polysilicon, J. Appl. Phys. **57**, 1671–1675 (1983)

11.8 R.T. Howe, R.S. Muller: Stress in polysilicon and amorphous silicon thin films, J. Appl. Phys. **54**, 4674–4675 (1983)

11.9 X. Zhang, T.Y. Zhang, M. Wong, Y. Zohar: Rapid thermal annealing of polysilicon thin films, J. Microelectromech. Syst. **7**, 356–364 (1998)

11.10 J. Yang, H. Kahn, A.-Q. He, S.M. Phillips, A.H. Heuer: A new technique for producing large-area as-deposited zero-stress LPCVD polysilicon films: The multipoly process, J. Microelectromech. Syst. **9**, 485–494 (2000)

11.11 P. Gennissen, M. Bartek, P.J. French, P.M. Sarro: Bipolar-compatible epitaxial poly for smart sensors: Stress minimization and applications, Sens. Actuators A **62**, 636–645 (1997)

11.12 P. Lange, M. Kirsten, W. Riethmuller, B. Wenk, G. Zwicker, J.R. Morante, F. Ericson, J.A. Schweitz: Thick polycrystalline silicon for surface-micromechanical applications: deposition, structuring, and mechanical characterization, Sens. Actuators A **54**, 674–678 (1996)

11.13 S. Greek, F. Ericson, S. Johansson, M. Furtsch, A. Rump: Mechanical characterization of thick polysilicon films: Young's modulus and fracture strength evaluated with microstructures, J. Micromech. Microeng. **9**, 245–251 (1999)

11.14 K. Funk, H. Emmerich, A. Schilp, M. Offenberg, R. Neul, F. Larmer: A surface micromachined silicon gyroscope using a thick polysilicon layer, Proc. 12th Int. Conf. Microelectromech. Syst. (IEEE, Piscataway 1999) pp. 57–60

11.15 T. Abe, M.L. Reed: Low strain sputtered polysilicon for micromechanical structures, Proc. 9th Int. Workshop Microelectromech. Syst. (IEEE, Piscataway 1996) pp. 258–262

11.16 K. Honer, G.T.A. Kovacs: Integration of sputtered silicon microstructures with pre-fabricated CMOS circuitry, Sens. Actuators A **91**, 392–403 (2001)

11.17 J. Gaspar, T. Adrega, V. Chu, J.P. Conde: Thin-film paddle microresonators with high quality factors fabricated at temperatures below 110 °C, Proc. 18th Int. Conf. Microelectromech. Syst. (IEEE, Piscataway 2005) pp. 125–128

11.18 R. Anderson, R.S. Muller, C.W. Tobias: Porous polycrystalline silicon: A new material for MEMS, J. Microelectromech. Syst. **3**, 10–18 (1994)

11.19 W. Lang, P. Steiner, H. Sandmaier: Porous silicon: A novel material for microsystems, Sens. Actuators A **51**, 31–36 (1995)

11.20 R. He, C.J. Kim: On-chip hermetic packaging enabled by post-deposition electrochemical etching of polysilicon, Proc. 18th Int. Conf. Microelectromech. Syst. (IEEE, Piscataway 2005) pp. 544–547

11.21 S.K. Ghandhi: *VLSI Fabrication Principles – Silicon and Gallium Arsenide* (Wiley, New York 1983)

11.22 W.A. Pilskin: Comparison of properties of dielectric films deposited by various methods, J. Vac. Sci. Technol. **21**, 1064–1081 (1977)

11.23 J.S. Danel, F. Michel, G. Delapierre: Micromachining of quartz and its application to an acceleration sensor, Sens. Actuators A **21–23**, 971–977 (1990)

11.24 A. Yasseen, J.D. Cawley, M. Mehregany: Thick glass film technology for polysilicon surface micromachining, J. Microelectromech. Syst. **8**, 172–179 (1999)

11.25 R. Liu, M.J. Vasile, D.J. Beebe: The fabrication of nonplanar spin-on glass microstructures, J. Microelectromech. Syst. **8**, 146–151 (1999)

11.26 B. Folkmer, P. Steiner, W. Lang: Silicon nitride membrane sensors with monocrystalline transducers, Sens. Actuators A **51**, 71–75 (1995)

11.27 M. Sekimoto, H. Yoshihara, T. Ohkubo: Silicon nitride single-layer x-ray mask, J. Vac. Sci. Technol. **21**, 1017–1021 (1982)

11.28 D.J. Monk, D.S. Soane, R.T. Howe: Enhanced removal of sacrificial layers for silicon surface micromachining, 7th Int. Conf. Solid State Sens. Actuators, Technical Digest (Institute of Electrical Engineers of Japan, Tokyo 1993) pp. 280–283

11.29 P.J. French, P.M. Sarro, R. Mallee, E.J.M. Fakkeldij, R.F. Wolffenbuttel: Optimization of a low-stress silicon nitride process for surface micromachining applications, Sens. Actuators A **58**, 149–157 (1997)

11.30 B. Li, B. Xiong, L. Jiang, Y. Zohar, M. Wong: Germanium as a versatile material for low-temperature micromachining, J. Microelectromech. Syst. **8**, 366–372 (1999)

11.31 A. Franke, D. Bilic, D.T. Chang, P.T. Jones, T.J. King, R.T. Howe, C.G. Johnson: Post-CMOS integration of germanium microstructures, Proc. 12th Int. Conf. Microelectromech. Syst. (IEEE, Piscataway 1999) pp. 630–637

11.32 A.E. Franke, Y. Jiao, M.T. Wu, T.J. King, R.T. Howe: Post-CMOS modular integration of poly-SiGe microstructures using poly-Ge sacraficial layers, Solid State Sens. Actuator Workshop, Technical Digest (Transducers Research Foundation, Hilton Head 2000) pp. 18–21

11.33 S. Sedky, P. Fiorini, M. Caymax, S. Loreti, K. Baert, L. Hermans, R. Mertens: Structural and mechanical properties of polycrystalline silicon germanium for micromachining applications, J. Microelectromech. Syst. **7**, 365–372 (1998)

11.34 J.M. Heck, C.G. Keller, A.E. Franke, L. Muller, T.-J. King, R.T. Howe: High aspect ratio polysilicon-germanium microstructures, Proc. 10th Int. Conf. Solid State Sens. Actuators (Institute of Electrical Engineers of Japan, Tokyo 1999) pp. 328–334

11.35 P. Van Gerwen, T. Slater, J.B. Chevrier, K. Baert, R. Mertens: Thin-film boron-doped polycrystalline $silicon_{70\%}$-$germanium_{30\%}$ for thermopiles, Sens. Actuators A **53**, 325–329 (1996)

11.36 D. Hyman, J. Lam, B. Warneke, A. Schmitz, T.Y. Hsu, J. Brown, J. Schaffner, A. Walson, R.Y. Loo, M. Mehregany, J. Lee: Surface micromachined RF MEMS switches on GaAs substrates, Int. J. Radio Freq. Microw. Commun. Eng. **9**, 348–361 (1999)

11.37 C. Chang, P. Chang: Innovative micromachined microwave switch with very low insertion loss, Sens. Actuators **79**, 71–75 (2000)

11.38 M.F. Aimi, M.P. Rao, N.C. MacDonald, A.S. Zuruzi, D.P. Bothman: High-aspect-ratio bulk micromachining of Ti, Nat. Mater. **3**, 103–105 (2004)

11.39 C.L. Shih, B.K. Lai, H. Kahn, S.M. Phillips, A.H. Heuer: A robust co-sputtering fabrication procedure for TiNi shape memory alloys for MEMS, J. Microelectromech. Syst. **10**, 69–79 (2001)

11.40 G. Hahm, H. Kahn, S.M. Phillips, A.H. Heuer: Fully microfabricated silicon spring biased shape memory actuated microvalve, Solid State Sens. Actuator Workshop, Technical Digest (Transducers Research Foundation, Hilton Head Island 2000) pp. 230–233

11.41 S.D. Leith, D.T. Schwartz: High-rate through-mold electrodeposition of thick (> 200 micron) NiFe MEMS components with uniform composition, J. Microelectromech. Syst. **8**, 384–392 (1999)

11.42 N. Rajan, M. Mehregany, C.A. Zorman, S. Stefanescu, T. Kicher: Fabrication and testing of micromachined silicon carbide and nickel fuel atomizers for gas turbine engines, J. Microelectromech. Syst. **8**, 251–257 (1999)

11.43 T. Pornsin-Sirirak, Y.C. Tai, H. Nassef, C.M. Ho: Titanium-alloy MEMS wing technology for a microaerial vehicle application, Sens. Actuators A **89**, 95–103 (2001)

11.44 C.R. Stoldt, C. Carraro, W.R. Ashurst, D. Gao, R.T. Howe, R. Maboudian: A low temperature CVD process for silicon carbide MEMS, Sens. Actuators A **97/98**, 410–415 (2002)

11.45 M. Eickhoff, H. Moller, G. Kroetz, J. von Berg, R. Ziermann: A high temperature pressure sensor prepared by selective deposition of cubic silicon carbide on SOI substrates, Sens. Actuators **74**, 56–59 (1999)

11.46 Y.T. Yang, K.L. Ekinci, X.M.H. Huang, L.M. Schiavone, M.L. Roukes, C.A. Zorman, M. Mehregany: Monocrystalline silicon carbide nanoelectromechanical systems, Appl. Phys. Lett. **78**, 162–164 (2001)

11.47 D. Young, J. Du, C.A. Zorman, W.H. Ko: High-temperature single crystal 3C-SiC capacitive pressure sensor, IEEE Sens. J. **4**, 464–470 (2004)

11.48 C.A. Zorman, S. Rajgolpal, X.A. Fu, R. Jezeski, J. Melzak, M. Mehregany: Deposition of polycrystalline 3C-SiC films on 100 mm-diameter (100) Si wafers in a large-volume LPCVD furnace, Electrochem. Solid State Lett. **5**, G99–G101 (2002)

11.49 I. Behrens, E. Peiner, A.S. Bakin, A. Schlachetzski: Micromachining of silicon carbide on silicon fabricated by low-pressure chemical vapor deposition, J. Micromech. Microeng. **12**, 380–384 (2002)

11.50 C.A. Zorman, S. Roy, C.H. Wu, A.J. Fleischman, M. Mehregany: Characterization of polycrystalline silicon carbide films grown by atmospheric pressure chemical vapor deposition on polycrystalline silicon, J. Mater. Res. **13**, 406–412 (1996)

11.51 C.H. Wu, C.H. Zorman, M. Mehregany: Growth of polycrystalline SiC films on SiO_2 and Si_3N_4 by APCVD, Thin Solid Films **355/356**, 179–183 (1999)

11.52 P. Sarro: Silicon carbide as a new MEMS technologyctuators, Sens. Actuators A **82**, 210–218 (2000)

11.53 N. Ledermann, J. Baborowski, P. Muralt, N. Xantopoulos, J.M. Tellenbach: Sputtered silicon carbide thin films as protective coatings for MEMS applications, Surf. Coat. Technol. **125**, 246–250 (2000)

11.54 X.A. Fu, R. Jezeski, C.A. Zorman, M. Mehregany: Use of deposition pressure to control the residual stress in polycrystalline SiC films, Appl. Phys. Lett. **84**, 341–343 (2004)

11.55 J. Trevino, X.A. Fu, M. Mehregany, C. Zorman: Low-stress, heavily-doped polycrystalline silicon carbide for MEMS applications, Proc. 18th Int. Conf. Microelectromech. Syst. (IEEE, Piscataway 2005) pp. 451–454

11.56 R.S. Okojie, A.A. Ned, A.D. Kurtz: Operation of a 6H-SiC pressure sensor at 500 °C, Sens. Actuators A **66**, 200–204 (1998)

11.57 K. Lohner, K.S. Chen, A.A. Ayon, M.S. Spearing: Microfabricated silicon carbide microengine structures, Mater. Res. Soc. Symp. Proc. **546**, 85–90 (1999)

11.58 K.O. Min, S. Tanaka, M. Esashi: Micro/nano glass press molding using silicon carbide molds fabricated by silicon lost molding, Proc. 18th Int. Conf. Microelectromech. Syst. (IEEE, Miami 2005) pp. 475–478

11.59 S. Tanaka, S. Sugimoto, J.-F. Li, R. Watanabe, M. Esashi: Silicon carbide micro-reaction-sintering using micromachined silicon molds, J. Microelectromech. Syst. **10**, 55–61 (2001)

11.60 L.A. Liew, W. Zhang, V.M. Bright, A. Linan, M.L. Dunn, R. Raj: Fabrication of SiCN ceramic MEMS using injectable polymer-precursor technique, Sens. Actuators A **89**, 64–70 (2001)

11.61 A.J. Fleischman, S. Roy, C.A. Zorman, M. Mehregany: Polycrystalline silicon carbide for surface micromachining, Proc. 9th Int. Workshop Microelectromech. Syst. (IEEE, San Diego 1996) pp. 234–238

11.62 A.J. Fleischman, X. Wei, C.A. Zorman, M. Mehregany: Surface micromachining of polycrystalline SiC deposited on SiO_2 by APCVD, Mater. Sci. Forum **264–268**, 885–888 (1998)

11.63 G. Beheim, C.S. Salupo: Deep RIE process for silicon carbide power electronics and MEMS, Mater. Res. Soc. Symp. Proc. **622**, T8.8.1–T8.8.6 (2000)

11.64 A. Yasseen, C.H. Wu, C.A. Zorman, M. Mehregany: Fabrication and testing of surface micromachined polycrystalline SiC micromotors, Electron. Device Lett. **21**, 164–166 (2000)

11.65 X. Song, S. Rajgolpal, J.M. Melzak, C.A. Zorman, M. Mehregany: Development of a multilayer SiC surface micromachining process with capabilities and design rules comparable with conventional polysilicon surface micromachining, Mater. Sci. Forum **389–393**, 755–758 (2001)

11.66 D. Gao, M.B. Wijesundara, C. Carraro, R.T. Howe, R. Maboudian: Recent progress toward and manufacturable polycrystalline SiC surface micromachining technology, IEEE Sens. J. **4**, 441–448 (2004)

11.67 T. Shibata, Y. Kitamoto, K. Unno, E. Makino: Micromachining of diamond film for MEMS applications, J. Microelectromech. Syst. **9**, 47–51 (2000)

11.68 H. Bjorkman, P. Rangsten, P. Hollman, K. Hjort: Diamond replicas from microstructured silicon masters, Sens. Actuators **73**, 24–29 (1999)

11.69 P. Rangsten, H. Bjorkman, K. Hjort: Microfluidic components in diamond, Proc. 10th Int. Conf. Solid State Sens. Actuators (IEEE, Sendai 1999) pp. 190–193

11.70 H. Bjorkman, P. Rangsten, K. Hjort: Diamond microstructures for optical microelectromechanical systems, Sens. Actuators **78**, 41–47 (1999)

11.71 M. Aslam, D. Schulz: Technology of diamond microelectromechanical systems, Proc. 8th Int. Conf. Solid State Sens. Actuators (IEEE, Stockholm 1995) pp. 222–224

11.72 R. Ramesham: Fabrication of diamond microstructures for microelectromechanical systems (MEMS) by a surface micromachining process, Thin Solid Films **340**, 1–6 (1999)

11.73 X. Yang, J.M. Yang, Y.C. Tai, C.M. Ho: Micromachined membrane particle filters, Sens. Actuators **73**, 184–191 (1999)

11.74 X.D. Wang, G.D. Hong, J. Zhang, B.L. Lin, H.Q. Gong, W.Y. Wang: Precise patterning of diamond films for MEMS application, J. Mater. Process. Technol. **127**, 230–233 (2002)

11.75 A.R. Krauss, O. Auciello, D.M. Gruen, A. Jayatissa, A. Sumant, J. Tucek, D.C. Mancini, N. Moldovan, A. Erdemire, D. Ersoy, M.N. Gardos, H.G. Busmann, E.M. Meyer, M.Q. Ding: Ultrananocrystalline diamond thin films for MEMS and moving mechanical assembly devices, Diam. Relat. Mater. **10**, 1952–1961 (2001)

11.76 X. Xiao, J. Birrell, J.E. Gerbi, O. Auciello, J.A. Carlisle: Low temperature growth of ultrananocrystalline diamond, J. Appl. Phys. **96**, 2232–2239 (2004)

11.77 T.A. Friedmann, J.P. Sullivan, J.A. Knapp, D.R. Tallant, D.M. Follstaedt, D.L. Medlin, P.B. Mirkarimi: Thick stress-free amorphous-tetrahedral carbon films with hardness near that of diamond, Appl. Phys. Lett. **71**, 3820–3822 (1997)

11.78 J.P. Sullivan, T.A. Friedmann, K. Hjort: Diamond and amorphous carbon MEMS, MRS Bulletin **26**, 309–311 (2001)

11.79 J.R. Webster, C.W. Dyck, J.P. Sullivan, T.A. Friedmann, A.J. Carton: Performance of amorphous diamond RF MEMS capacitive switch, Electron. Lett. **40**, 43–44 (2004)

11.80 K. Hjort, J. Soderkvist, J.-A. Schweitz: Galium arsenide as a mechanical material, J. Micromech. Microeng. **4**, 1–13 (1994)

11.81 K. Hjort: Sacrificial etching of III–V compounds for micromechanical devices, J. Micromech. Microeng. **6**, 365–370 (1996)

11.82 K. Fobelets, R. Vounckx, G. Borghs: A GaAs pressure sensor based on resonant tunnelling diodes, J. Micromech. Microeng. **4**, 123–128 (1994)

11.83 A. Dehe, K. Fricke, H.L. Hartnagel: Infrared thermopile sensor based on AlGaAs-GaAs micromachining, Sens. Actuators A **46/47**, 432–436 (1995)

11.84 A. Dehe, J. Peerlings, J. Pfeiffer, R. Riemenschneider, A. Vogt, K. Streubel, H. Kunzel, P. Meissner,

H.L. Hartnagel: III–V compound semiconductor micromachined actuators for long resonator tunable Fabry-Perot detectors, Sens. Actuators A **68**, 365–371 (1998)

11.85 T. Lalinsky, S. Hascik, Z. Mozolova, E. Burian, M. Drzik: The improved performance of GaAs micromachined power sensor microsystem, Sens. Actuators **76**, 241–246 (1999)

11.86 T. Lalinsky, E. Burian, M. Drzik, S. Hascik, Z. Mozolova, J. Kuzmik, Z. Hatzopoulos: Performance of GaAs micromachined microactuator, Sens. Actuators **85**, 365–370 (2000)

11.87 H.X. Tang, X.M.H. Huang, M.L. Roukes, M. Bichler, W. Wegscheider: Two-dimensional electron-gas actuation and transduction for GaAs nanoelectromechanical systems, Appl. Phys. Lett. **81**, 3879–3881 (2002)

11.88 T.S. Tighe, J.M. Worlock, M.L. Roukes: Direct thermal conductance measurements on suspended monocrystalline nanostructure, Appl. Phys. Lett. **70**, 2687–2689 (1997)

11.89 J. Miao, B.L. Weiss, H.L. Hartnagel: Micromachining of three-dimensional GaAs membrane structures using high-energy nitrogen implantation, J. Micromech. Microeng. **13**, 35–39 (2003)

11.90 C. Seassal, J.L. Leclercq, P. Viktorovitch: Fabrication of inp-based freestanding microstructures by selective surface micromachining, J. Micromech. Microeng. **6**, 261–265 (1996)

11.91 J. Leclerq, R.P. Ribas, J.M. Karam, P. Viktorovitch: III–V micromachined devices for microsystems, Microelectron. J. **29**, 613–619 (1998)

11.92 H. Yamaguchi, R. Dreyfus, S. Miyashita, Y. Hirayama: Fabrication and elastic properties of InAs freestanding structures based on InAs/GaAs(111) a heteroepitaxial systems, Physica E **13**, 1163–1167 (2002)

11.93 C. Lee, T. Itoh, T. Suga: Micromachined piezoelectric force sensors based on PZT thin films, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **43**, 553–559 (1996)

11.94 B. Xu, L.E. Cross, J.J. Bernstein: Ferroelectric and antiferroelectric films for microelectromechanical systems applications, Thin Solid Films **377/378**, 712–718 (2000)

11.95 S.P. Beeby, A. Blackburn, N.M. White: Processing of PZT piezoelectric thick films on silicon for microelectromechanical systems, J. Micromech. Microeng. **9**, 218–229 (1999)

11.96 C. Shearwood, M.A. Harradine, T.S. Birch, J.C. Stevens: Applications of polyimide membranes to MEMS technology, Microelectron. Eng. **30**, 547–550 (1996)

11.97 F. Jiang, G.B. Lee, Y.C. Tai, C.M. Ho: A flexible micromachine-based shear-stress sensor array and its application to separation-point detection, Sens. Actuators **79**, 194–203 (2000)

11.98 D. Memmi, V. Foglietti, E. Cianci, G. Caliano, M. Pappalardo: Fabrication of capacitive micromechanical ultrasonic transducers by low-temperature process, Sens. Actuators A **99**, 85–91 (2002)

11.99 A. Bagolini, L. Pakula, T.L.M. Scholtes, H.T.M. Pham, P.J. French, P.M. Sarro: Polyimide sacrificial layer and novel materials for post-processing surface micromachining, J. Micromech. Microeng. **12**, 385–389 (2002)

11.100 T. Stieglitz: Flexible biomedical microdevices with double-sided electrode arrangements for neural applications, Sens. Actuators A **90**, 203–211 (2001)

11.101 T. Stieglitz, G. Matthias: Flexible BioMEMS with electrode arrangements on front and back side as key component in neural prostheses and biohybrid systems, Sens. Actuators B **83**, 8–14 (2002)

11.102 H. Lorenz, M. Despont, N. Fahrni, J. Brugger, P. Vettiger, P. Renaud: High-aspect-ratio, ultrathick, negative-tone-near-UV photoresist and its applications in MEMS, Sens. Actuators A **64**, 33–39 (1998)

11.103 H. Lorenz, M. Despont, N. Fahrni, N. LaBianca, P. Renaud, P. Vettiger: SU-8: A low-cost negative resist for MEMS, J. Micromech. Microeng. **7**, 121–124 (1997)

11.104 E.H. Conradie, D.F. Moore: SU-8 thick photoresist processing as a functional material for MEMS applications, J. Micromech. Microeng. **12**, 368–374 (2002)

11.105 C.T. Pan, H. Yang, S.C. Shen, M.C. Chou, H.P. Chou: A low-temperature wafer bonding technique using patternable materials, J. Micromech. Microeng. **12**, 611–615 (2002)

11.106 P.A. Stupar, A.P. Pisano: Silicon, parylene, and silicon/parylene micro-needles for strength and toughness, 11th Int. Conf. Solid State Sens. Actuators, Technical Digest (Springer, Berlin 2001) pp. 1368–1389

11.107 J.M. Zara, S.W. Smith: Optical scanner using a MEMS actuator, Sens. Actuators A **102**, 176–184 (2002)

11.108 H.S. Noh, P.J. Hesketh, G.C. Frye-Mason: Parylene gas chromatographic column for rapid thermal cycling, J. Microelectromech. Syst. **11**, 718–725 (2002)

11.109 T.J. Yao, X. Yang, Y.C. Tai: BrF_3 dry release technology for large freestanding parylene microstructures and electrostatic actuators, Sens. Actuators A **97/98**, 771–775 (2002)

11.110 X. Wang, J. Engel, C. Liu: Liquid crystal polymer (LCP) for MEMS: Processing and applications, J. Micromech. Microeng. **13**, 628–633 (2003)

11.111 C.J. Lee, S.J. Oh, J.K. Song, S.J. Kim: Neural signal recording using microelectrode arrays fabricated on liquid crystal polymer material, Mater. Sci. Eng. C **4**, 265–268 (2004)

11.112 F.F. Faheem, K.C. Gupta, Y.C. Lee: Flip-chip assembly and liquid crystal polymer encapsulation for variable MEMS capacitors, IEEE Trans. Microw. Theory Tech. **51**, 2562–2567 (2003)