A Vertical Sidewall Surface Piezoresistor Technology Based on DRIE and Its Typical Application in Micro xy-Stages

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Abstract. A vertical sidewall surface piezoresistor technology is developed for single-wafer-processed MEMS of in-plane lateral piezoresistors configuration. The technology based on the deep reactive ion etching (DRIE) and the ion implantation technology can be used to integrate piezoresistive sensor on the vertical sidewall of trench or beam easily. The developed technology has been successfully applied to a nano-positioning micro xy-stage integrated with displacement sensor based on the piezo-resistance effect, in which the piezoresistor has been fabricated on the vertical sidewall surface of the detecting beam to improve the displacement sensitivity and resolution of sensor. Besides satisfactory electric principles of the piezoresistors obtained, the experimental results also verify the sensitivity of the fabricated piezoresistive sensors is better than 0.903mV/μm without amplification, the linearity is better than 0.814%, which are well with design.

Keywords: MEMS, DRIE, Vertical sidewall piezoresistor, micro xy-stage.

1 Introduction

With the development of the surface micromachining and bulk micromachining, varieties of formation fabricated piezoresistor technology based on inductively coupled plasma (ICP) deep reactive ion etching (DRIE) process have been developed for single-wafer-processed MEMS of in-plane lateral piezoresistor configuration, such as oblique ion implantation technology[1][2][3] and the trench-sidewall single-wafer-MEMS technology[4][5]. In the former process, the piezoresistors are formed by ion implantation technology, so the trenches have to be widely opened enough for oblique implantation which may make difficulties in squeeze-film damping and electrostatic actuating designed, besides, this process has the disadvantage of integration incompatibility. For the latter process, the piezoresistors are formed by ion diffusion technology, so it is not limited by the width of the trench, but this process is more complicated and the piezoresistive region is more difficult to be controlled. New technology featuring improved integration capability, low cost and high yield is in demand. A vertical sidewall surface piezoresistor technology based on DRIE and ion

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implantation technique is proposed in this paper. With this process, the piezoresistor can be integrated on the trench or beam sidewall easily. The technical details of the proposed vertical sidewall surface piezoresistor and the typical application will be described in following sections.

2 Processes of the Vertical Sidewall Piezoresistor

The fabrication process of the vertical sidewall surface piezoresistor is mainly based on DRIE technology and ion implantation technology. The process includes four patterning and one DRIE etching step. The fabrication process for sidewall piezoresistor is depicted in fig. 1 and described as follows.

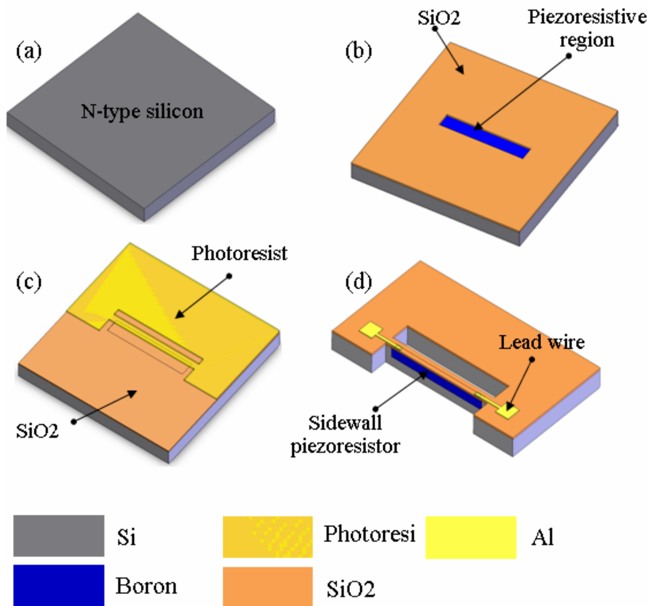

Fig. 1. Fabrication process of the vertical sidewall piezoresistor

(1) Starting from double polished n-type (100)-oriented 4 inch ordinary silicon wafers with a resistivity of 1～10 Ω·cm;
(2) The SiO_2 layer is grown on both side of the silicon wafers by the thermally oxidation process; The SiO2 layer thickness is controlled to be approximately 0.5μm and then the first time photolithography is conducted on the front side of the wafer to pattern the resistor region, then buffer HF acid is used to etch SiO_2 with photoresist as the etching mask;
(3) The surface piezoresistors are formed by boron ion implantation process. In order to reduce the temperature sensitivity of piezoresistors and form better ohmic contact in the next step, the impurity concentration on the wafer surface is controlled at about 10^{19} atoms/cm^{-3};

(4) After the second time photolithography, the contact hole is formed by buffer HF acid etching, and then aluminum is sputtered and patterned with the third time photolithography, metallization process is performed for interconnection. Finally, the fourth photolithography is used to shape the detecting beam and the sidewall piezoresistor based on the formed surface piezoresistor, the inductive coupled plasma (ICP) deep RIE is performed to release detecting beam and form veridical sidewall piezoresistors, synchronously, the protective layer on the surface of the sidewall piezoresistor is form with the polymer by the protective gas of C_4F_8 during the DRIE.

3 Experiments and Typical Application

For evaluating the capability of the vertical sidewall surface piezoresistors technique, a nano-positioning micro xy-stage integrating displacement sensor based on the piezo-resistance effect is fabricated by the process proposed in this paper, as shown in fig.2.

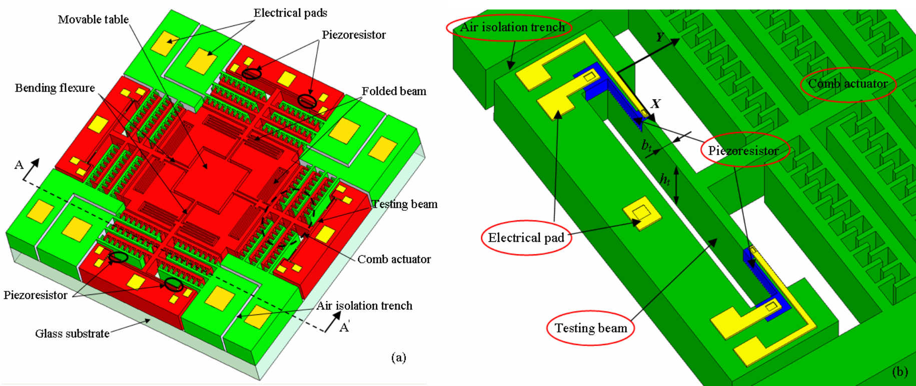

Fig. 2. (a) Schematic of the micro xy-stage and (b) a 3D sketch of the testing beam and piezoresistors

Fig. 2(b) shows a 3D schematic of the detecting beam and the sensor configuration. The sensing direction of the displacement sensor base on piezoresistor is in the wafer plane. The transversely deflecting clamped-clamped beam (detecting beam) is designed to measure the lateral displacement of the movable stage. The aspect ratio of the detecting beam cross section is designed as 1:3.75 to decrease the cross-sensitivity of orthogonal direction. Two vertical sidewall surface piezoresistors have been fabricated on the outboard surface of the both end of the detecting beam respectively, and there are two detecting beams with the identical construction located at the both side of the movable stage. At the middle of which are connected to the movable stage. Fig. 3 shows a simplified mechanism of the fabricated micro xy-stage. When the movable stage moves along the *x*-direction, the detecting beams deflect along the *x*-direction

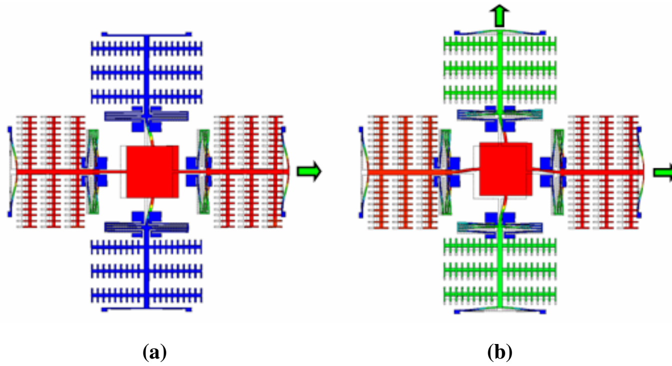

Fig. 3. The driving mechanism of the micro xy-stage :(a) x-actuation; (b) x-and y-actuation

too, Two resistors increase their resistance, whereas, the others decrease. So the four piezoresistors can be used to form a full Wheatstone bridge (see fig.2 (a)).

Fig.4 shows a brief process flow of the micro xy-stage as a cross-sectional process at the dash-dotted line A-A' in fig.2 (a). Fig. 5(a) and (b) show the top-view CCD micrograph of the piezoresistor. In figure 5(a) shows the surface piezoresistor before forming the vertical sidewall surface piezoresistor by using DRIE, and (b) shows the fabricated vertical sidewall surface piezoresistor after being released by the DRIE. The fig. 5(c) shows the close-up views of the end of the detecting beam, on the vertical sidewall surface of which there is a fabricated piezoresistor and fig. 5(d) shows the SEM photo of the fabricated micro xy-stage chip.

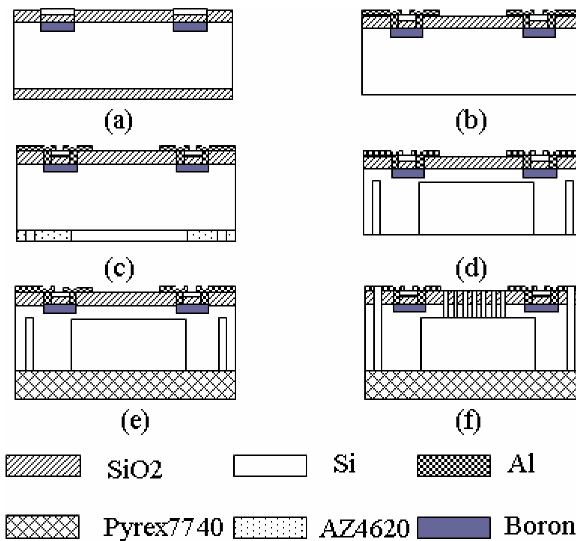

Fig. 4. Cross-sectional process flow of the xy-stage at the dash-dotted line A-A' in fig.2 (a)

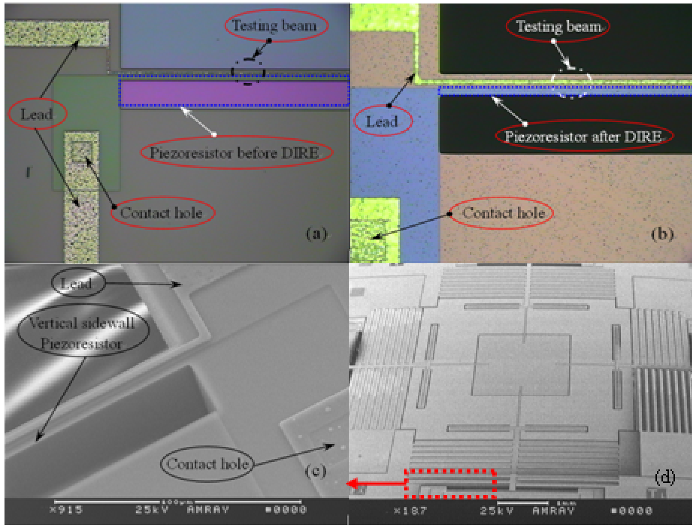

Fig. 5. The photograph of piezoresistor during the fabricating process, the fabricated micro xy-stage and the close-up view of the fabricated testing beam and piezoresistors

Using the fabricated micro xy-stage structure, the vertical sidewall piezoresistor technique can be evaluated by electric principle characterization. Fig. 6(a) shows measured *I-V* principle of a sidewall piezoresistors. About 5.4kΩ sidewall-piezoresistance with sheet resistance of about 95Ω/□ is also measured. Fig. 6(b) shows the measured breakdown voltage of two adjacent piezoresistors. Higher than 45V breakdown voltage is measured this is enough for the sensor operation. From the measured electric principles, the feasibility of the vertical sidewall piezoresistors technique can be approved.

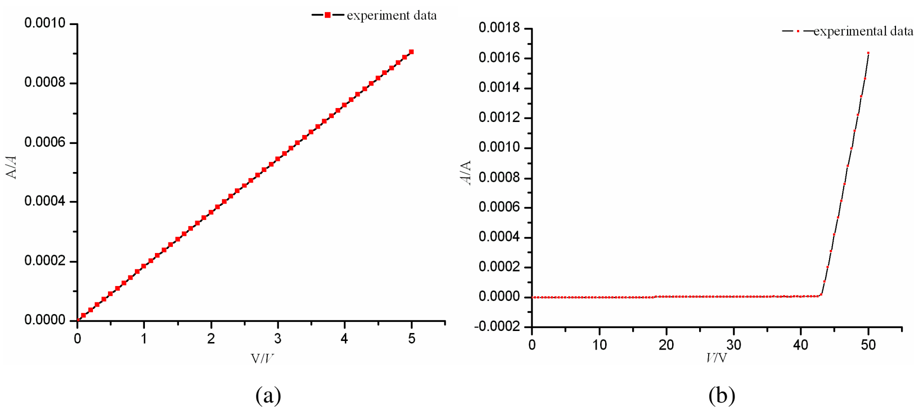

Fig. 6. Measure sidewall piezoresistors electric principles. (a) Linear *I-V* principle of a sidewall piezoresistor with sheet resistance of about 95Ω, and (b) Higher than 45V breakdown voltage is measured between two adjacent piezoresistors.

Fig. 7 shows the curve relationship between the displacement and the measured voltage of the displacement sensor without amplification. The experimental data are estimated by the method of least squares. After the fitting, the relationship between the displacement of stage and the measured voltage can be, respectively, expressed as:

$$\begin{aligned} y &= -0.00177x + 0.37519, \quad in+x\ direction \\ y &= +0.00129x + 0.36308, \quad in-x\ direction \\ y &= +0.00117x + 0.23696, \quad in+y\ direction \\ y &= -0.00090x + 0.23963, \quad in-y\ direction \end{aligned} . \tag{1}$$

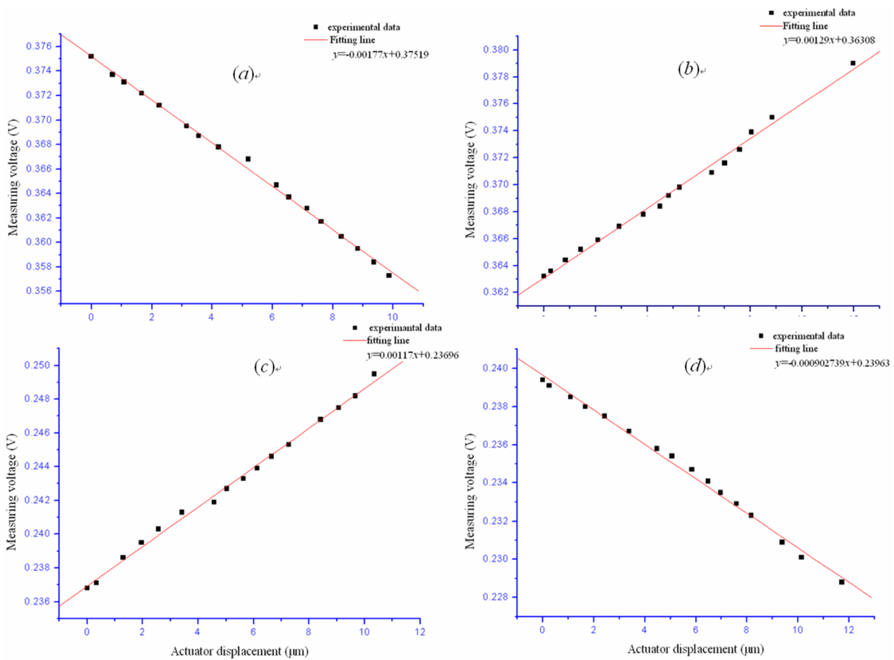

Fig. 7. Curve between the displacement and measured voltage. (a) relationship between displacement and measured voltage in +x direction; (b) relationship between displacement and measured voltage in -x direction; (c) relationship between displacement and measured voltage in +y direction and (d) relationship between displacement and measured voltage in -y direction.

Table 1. The sensitivity and linearity of displacement sensor

Actuator(direction)	+x	-x	+y	-y
Sensitivity(mV/μm)	-1.77	1.29	1.17	-0.903
Linearity (%)	0.814%	0.510%	0.429%	0.346%

The sensitivity of response to the displacement of the xy-stage and linearity of the piezoresistive sensor are listed in Table 1. If taking fabrication imperfections into consideration, the measured results agree well with design.

Using the displacement sensor composed of sidewall piezoresistors, the dynamic behavior (natural frequency) of the stage is also obtained experimentally. Fig. 8 is a bode plot. The measured first resonant frequency is found at 983Hz as shown in fig. 8. It is 15.9% lower than the simulated first undamped natural frequency, 1169Hz. The discrepancy that is observed may arise from fabrication imperfections and the since the stiffness of the flexures is sensitive to their dimensions. Further, approximations made in the finite element modeling and the effect of the damping condition is not to be taken into account during the experiment all may also contribute to this discrepancy. So the measured results also agree well with design.

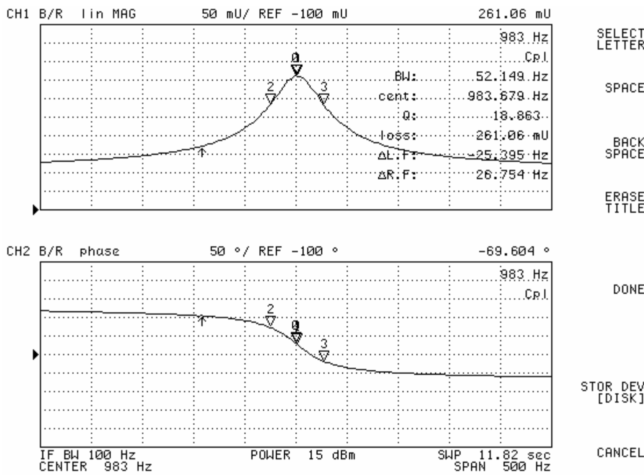

Fig. 8. Measured frequency response of the in-plane component, both amplitude (upper traces) and phases (lower traces). Response curves yielded values o f0=983Hz, Q=18.86.

4 Conclusions

From the results of the micro xy-stage integrated with the sidewall piezoresistive sensor, the capability of the vertical sidewall surface piezoresistors technique is verified. As a standard process for single wafer integration of in-plane MEMS configuration, the proposed technology is promising to be widely used.

Acknowledgments

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