9

A Centre-of-Mass Tracker Integrated Circuit Design in Nanometric CMOS for Robotic Visual Object Position Tracking

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Summary. Object position tracking is a well-known problem in robotic vision system design. This chapter proposes a new centre-of-mass(COM) object position tracker integrated circuit design using standard low-cost digital CMOS process technology without the need for a floating gate poly2 layer. The proposed COM tracker is designed using an IBM 130-nm CMOS process with a 1 V supply voltage and can be used for single-chip robotic visual feedback object tracking application. It uses an analogue sampled-data technique and is operated by a two-phase clocking system. The clock frequency can be varied to suit the real-time throughput requirements of the specific robotic object tracking tasks. A 6-input COM detector (easily extendable to 12-input or higher) was simulated and the results for various COM positions was found to be correctly tracked by the circuit. In addition, Monte Carlo simulations were carried out to prove the robustness of the technique.

Keywords: robotic vision, analogue CMOS VLSI, centre-of-mass, robotic object tracking.

9.1 Introduction

Centre-of-mass (COM), the first moment of an object's intensity distribution represents the position of an object. Consequently it has wide applications in robotic vision for visual feedback object tracking [1]. The COM of an object has to be determined in real-time with minimal delay for robotic vision image processing. Compared to digital image processing techniques, analogue processing of image signals provides faster COM response time since no A/D conversion of image signals is required. Yu et al. [2] proposed a COM tracker circuit based on implementation by neuron MOS technology [4]. Although neuron MOS technology simplifies implementation of many robotic and neural

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network circuits [3], it requires extra CMOS processing steps (e.g. POLY2) which is not usually available in many low-cost CMOS process technologies. In this chapter a novel COM detector circuit is proposed which replaces the need for floating gate neuron MOSFETs with the use of a capacitive sampled-data technique following [5]. The proposed circuit uses a 1 V supply voltage and is quite robust to process related threshold voltage variations. The circuit can be extended to any number of analogue image signal inputs and produces a binary (thresholding) COM decision which can be stored as a digital signal in a micro-controller status register. The preliminary work was reported in [7].

9.2 Proposed COM Circuit Architecture

Figure 9.1 shows the basic algorithm to be implemented in each axis for a 2D separable image intensity distribution of an object (e.g. a creature object) for the determination of its COM. Each axis thus requires a separate block of the proposed COM detector. Figure 9.2 shows the circuit architecture of the proposed sampled-data centre-of-mass tracker circuit. It essentially consists of (n+1) capacitive moment-of-intensity circuits and n sampled-data inverter comparators for an n-position COM tracker circuit. The location (position) of the moment-of-intensity for a set of analogue sampled intensities $[v_1,\ v_2,\ v_3, \ldots, v_n]$ using capacitive position-scalars [C, 2C, 3C, . . . , nC] is given by,

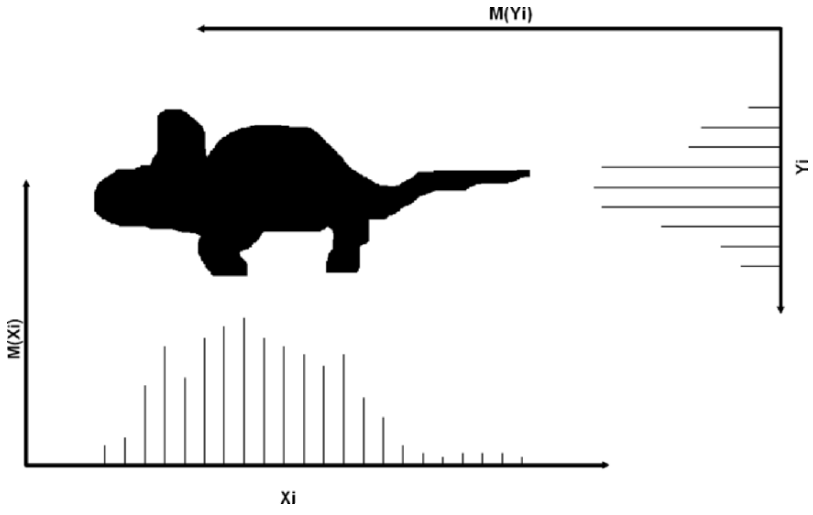

Fig. 9.1. Illustration of the centre-of-mass (COM) detection algorithm. 2D separable image intensity distribution projections in X and Y directions are separately obtained and processed

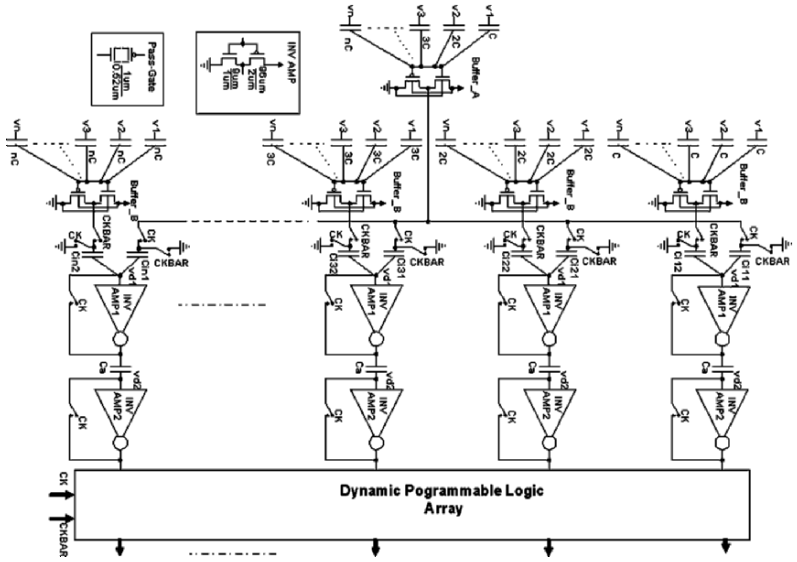

Fig. 9.2. Architecture of the proposed sampled-data real-time centre-of-mass detector circuit for each axis of the 2D separable image

$$C_x = \frac{\sum_{r=1}^{n} rCv_r}{\sum_{r=1}^{n} v_r} \tag{9.1}$$

where C_x is the capacitive COM position-scalar.

Next, (9.1) can be rearranged as,

$$C_x \sum_{r=1}^{n} v_r = \sum_{r=1}^{n} rCv_r \tag{9.2}$$

Now, introducing a proportionality constant, k, (9.2) can be written as,

$$\left[\frac{C_x \sum_{r=1}^{n} v_r}{nC_x}\right] * k * nC_x = \left[\frac{\sum_{r=1}^{n} rCv_r}{\sum_{r=1}^{n} rC}\right] * k * \sum_{r=1}^{n} rC \tag{9.3}$$

Next, dividing both sides by,

$k * nC_x + k * \sum_{r=1}^{n} rC$, and changing sides, we have,

$$\frac{\left[\frac{C_x \sum_{r=1}^{n} v_r}{nC_x}\right] * k * nC_x - \left[\frac{\sum_{r=1}^{n} rCv_r}{\sum_{r=1}^{n} rC}\right] * k * \sum_{r=1}^{n} rC}{k * nC_x + k * \sum_{r=1}^{n} rC} = 0 \tag{9.4}$$

In the proposed COM circuit, the closest value $C_x = rC$ is sought so that (9.4) holds. So, making this replacement in (9.4), we have,

$$\frac{\left[\frac{rC \sum_{r=1}^{n} v_r}{nrC}\right] * k * nrC - \left[\frac{\sum_{r=1}^{n} rCv_r}{C * \frac{n(n+1)}{2}}\right] * k * C * \frac{n(n+1)}{2}}{k * nrC + k * C * \frac{n(n+1)}{2}} = M \tag{9.5}$$

where, the specific value r is sought for which the difference M changes sign. The proposed COM tracker is an implementation of the (9.5) with the value r (for which M changes sign) being the COM position detected by the circuit. In the implementation architecture of Fig. 9.2, n sampled data comparison paths are shown (for an n position COM tracker) with the top path (position) for r=1 and the bottom path (position) for r=n. For all the paths,

$$C_{i11} = C_{i21} = C_{i31} = \ldots.. = C_{ir1} = \ldots.... = C_{in1} = k * C * \frac{n(n+1)}{2} \tag{9.6}$$

And, for any path r,

$$C_{ir2} = knrC \tag{9.7}$$

Ca is an appropriately chosen value for sampled-data input to the second inverter-amplifier. The rth path (position) source-follower Buffer_B produces the output voltage, $\frac{rC \sum_{r=1}^{n} v_r}{nrC} = Vr$ (say). Also, the source-follower Buffer_A produces the output voltage, $\frac{\sum_{r=1}^{n} rCv_r}{\sum_{r=1}^{n} rC} = Vc$(say). The two inputs Vc and Vr along the rth path are sampled during setup phase, PH1 (using clock-signal, CK) and the comparison phase, PH2 (using the clock-bar-signal, CKBAR) intervals, respectively, of a 50% duty cycle global truly single phase clock (TSPC) signal. In a TSPC scheme [6] CKBAR is derived directly by inverting CK instead of using a non-overlapping clock generator, which provides considerable savings in silicon real-estate that would otherwise be consumed by the clock generator circuit. The perturbation signal at the input of the inverter-amplifier 1 (V_{d1}) in the rth path during PH2 interval is due to the difference of two capacitively divided voltages and is then given by,

$$V_{d1} = \frac{(Vc * C_{ir1} - Vr * C_{ir2})}{(C_{ir1} + C_{ir2} + C_{ip})} \tag{9.8}$$

where, C_{ip} is the input parasitic capacitance of the inverter-amplifier. Due to electrostatic coupling of only the weighted difference signal, $(Vc * C_{ir1} - Vr * C_{ir2})$, both the inputs Vc and Vr can individually vary over a wide dynamic range. Both the inverter-amplifiers are self-biased at the common mode voltage (V_{cm}) which is set at half the supply-voltage in order to provide maximum bipolar signal swing at the output. The two inverter-amplifiers are disabled during the setup phase (i.e. during the PH1 interval) via a short-circuit switched by a pass-gate using the CK signal. During the comparison phase (i.e. during the PH2 interval) the perturbation input voltage V_{d1} (given by (9.8)) at the input of the inverter-amplifier 1 is amplified by its gain A1. As a result the perturbation input V_{d2} at the input of the inverter-amplifier 2 in the rth path, which is also due to a capacitive voltage division, is given by,

$$v_{d2} = \left[\frac{(Vc * Cir1 - Vr * Cir2)}{(Cir1 + Cir2 + C_{ip})} * A1\right] * \frac{Ca}{Ca + C_{ip}} \tag{9.9}$$

Finally, this perturbation signal V_{d2} is amplified by the gain A2 of the inverter-amplifier 2 (which is also enabled during the PH2 period). The rth path (position) starting at which the output of the inverter-amplifier 2 switches to opposite polarity compared to the (r−1)th path (position) is the tracked COM position for the input image intensity distribution. A Programmable logic array (PLA) or other simplified logic can be used to flag the COM position using the truth table in Table 9.1. The simple logic implementation using CMOS Nand & Inverter logic gates is shown in Fig. 9.3. The problem

Table 9.1. PLA truth table of the COM tracker output logic

PLA Input	PLA ouput	Comment
011111111111	100000000000	COM @ boundary of object
001111111111	010000000000	COM @ axis_position_2
000111111111	001000000000	COM @ axis_position_3
000011111111	000100000000	COM @ axis_position_4
000001111111	000010000000	COM @ axis_position_5
000000111111	000001000000	COM @ axis_position_6
000000011111	000000100000	COM @ axix_position_7
000000001111	000000010000	COM @ axis_position_8
000000000111	000000001000	COM @ axis_position_9
000000000011	000000000100	COM @ axis_position_10
000000000001	000000000010	COM @ axis_position_11
000000000000	000000000001	COM @ boundary of object

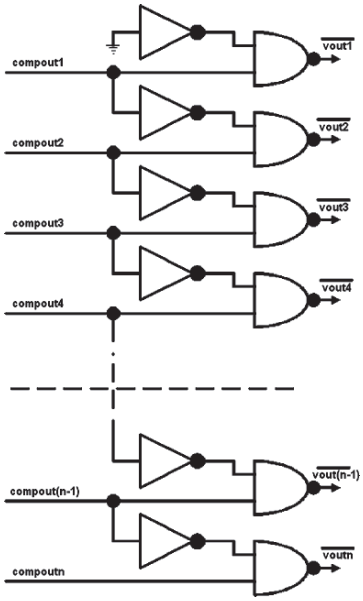

Fig. 9.3. Simple CMOS circuit for the implementation of the PLA truth table of the COM tracker output logic

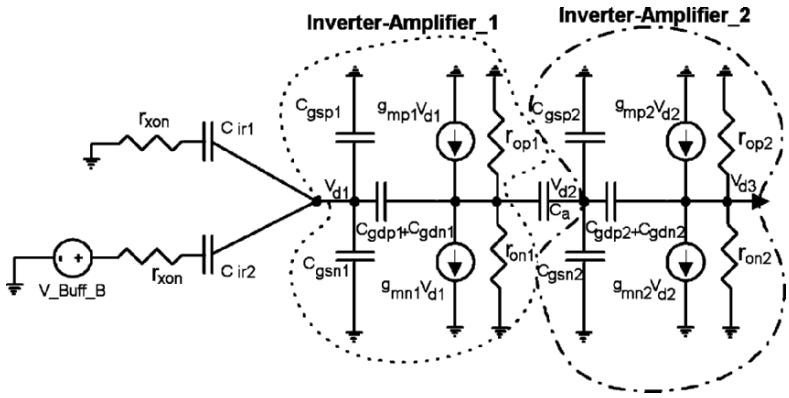

Fig. 9.4. Equivalent circuit of the COM detector's analogue sampled-data signal path during PH2 interval for response time estimation

of charge injection and charge absorption along the pass-transistor controlled signal path can be minimized by using dummy pass gates. The optimum size of the capacitors were determined based on the consideration of response time, parasitic input capacitance of the inverter-amplifiers and charge leakage. The final COM output is available during the comparison phase (PH2) for the input read cycle of any back-end robotic vision logic/instrumentation. Figure 9.4 shows a small signal (perturbation signal) equivalent circuit of the

COM detector's analogue sampled data signal path during the comparison phase (PH2) using standard models for the P-channel MOSFET(PMOS) and N-channel MOSFET(NMOS) devices. Also, standard component notations are used for the resistors, capacitors, voltage and current sources.

9.3 Circuit Simulation and Analysis Results

In order to verify the operation of the proposed novel COM tracker circuit extensive simulations were carried out using the 8M1P 0.13 µm IBM CMOS process technology parameters (BSIM level 49 parameters from a MOSIS wafer lot) using Tanner T-SPICE v.12. The supply voltage was 1.0 V and an input unit capacitance position-scalar of 0.1 pF was used. A 125 kHz clock (time-period = 8 µs) was used as the CK signal for switching the pass gates which is fast enough for many robotic vision systems. Rise-time and fall-time for the clock was set at around 5 ns which can be easily implemented on-chip using standard static CMOS circuit. The inverter-amplifiers are designed using relatively long channel devices for obtaining higher output impedance and resulting higher voltage gain. That way the polarity switch of the 2nd inverter-amplifier's output can be easily detected by the COM tracker output logic (due to a higher noise margin). A six position COM tracker was simulated so that n = 6. Ca was set at 1 pF. k was set to 1, and, the maximum value of capacitance used was 3.6 pF. The circuit design of the pass-gates and the inverter-amplifiers is shown in Fig. 9.2. The device sizes are shown next to the transistors. The tracked COM output is indicated with an active-low signal during PH2 in the COM output logic. Figure 9.5 shows the output of the 6-input COM detector circuit with discrete positions of 0.1 through 0.6, for an exact COM capacitive position-scalar value of 0.46. Figure 9.5a shows the outputs for positions 1, 2, 3, 4 and 6 (all 'HIGH') while Fig. 9.5b shows the output for position 5 ('LOW' during PH2), and, Fig. 9.5c shows the clock PH2 signal. So the nearest COM position 5 (corresponding to the capacitive position-scalar value of 0.5) is tracked by the circuit corresponding to the exact value of 0.46. Similarly, COM position is also correctly tracked for an exact COM of 0.28 as indicated in Fig. 9.6, resulting in a tracked COM position of 3. Next, 100 iterations of Monte Carlo simulations are carried out for process related threshold voltage variation of 25% using a Gaussian distribution function. An exact COM position of 0.38 was applied at the input. The COM was correctly tracked to position 4 as shown in Fig. 9.7. This proves that the proposed architecture is quite robust under process variations in any low-cost digital CMOS technology. The static power dissipated by the COM tracker from a 1 V supply voltage was under 100 µW making it extremely suitable for mobile robotic systems. The response time constraint of the COM tracker circuit can be determined by identifying the major time-constant nodes of the circuit. For this purpose, Fig. 9.4 showing the small signal (perturbation signal) equivalent circuit for the COM detector's signal path (along any rth path)

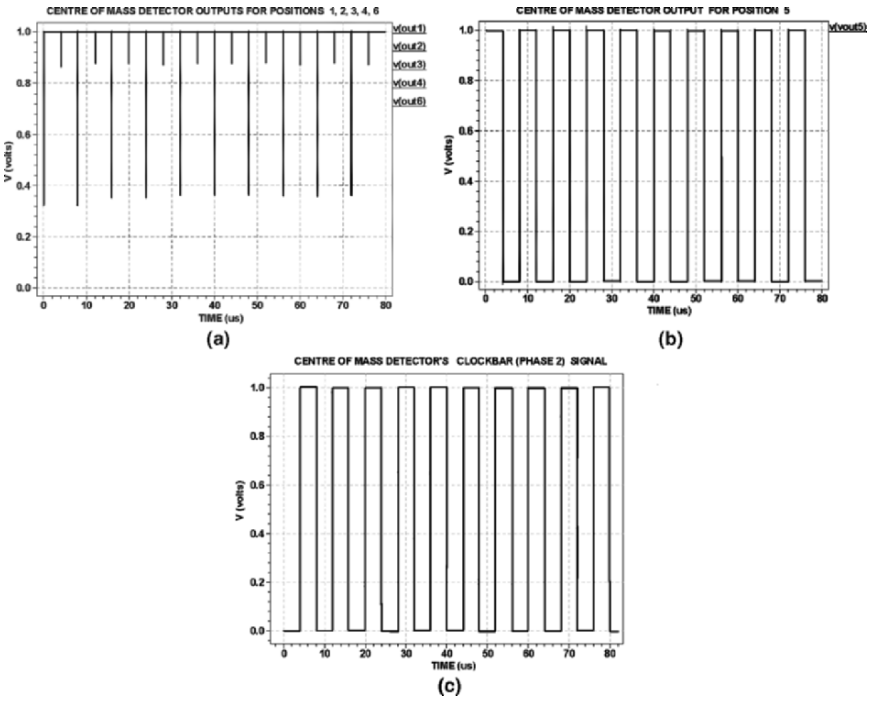

Fig. 9.5. Final output of the 6-input COM detector circuit for a COM of 0.46, (**a**) outputs for positions 1, 2, 3, 4 and 6, (**b**) output for position 5 and (**c**) the clock phase 2(PH2)

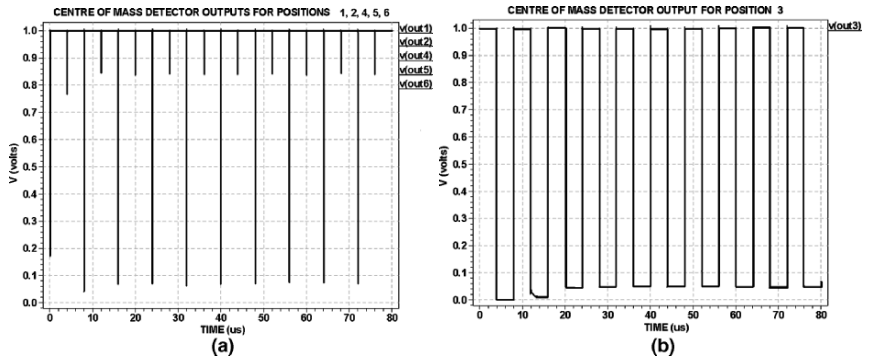

Fig. 9.6. Final output of the 6-input COM detector circuit for a COM of 0.28, (**a**) outputs for positions 1, 2, 4, 5 and 6, (**b**) output for position 3

during the comparison phase can be utilized. The dotted lines enclose equivalent circuits for the sub-block components. Here r_{xon} is the finite on-resistance of the transmission-gate switches (ideally should be very small). All other symbols and notations have their usual meaning for standard small signal

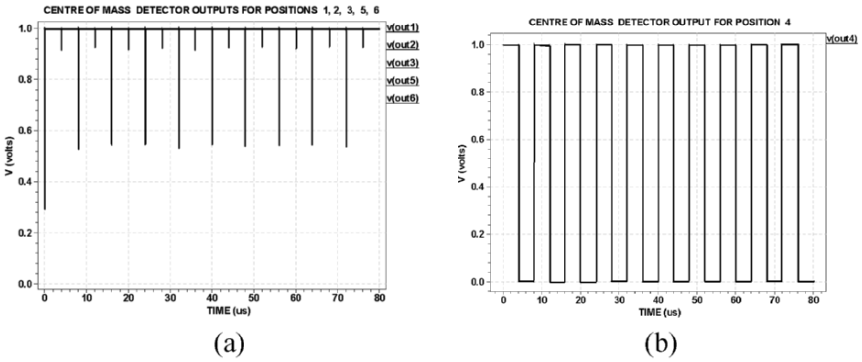

Fig. 9.7. Final output of the 6-input COM detector circuit for a COM of 0.38, (**a**) outputs for positions $1, 2, 3, 5$ and 6, (**b**) output for position 4, considering threshold voltage variation by over 25% after 100 iterations of Monte Carlo simulations

MOSFET model as follows: C_{gsp} is the PMOS gate-to-source capacitance, C_{gsn} is the NMOS gate-to-source capacitance, C_{gdp} is the PMOS gate-to-drain capacitance, C_{gdn} is the NMOS gate-to-drain capacitance, r_{op} is the PMOS output impedance, r_{on} is the NMOS output impedance, g_{mp} is the PMOS transconductance and finally g_{mn} is the NMOS transconductance. The dominant time constants are at the *outputs* of the inverter-amplifier 1 and the inverter-amplifier 2. The time constant (τ_1) at the *output* of inverter-amplifier 1 is given by (including the miller equivalent capacitance due to the gate-to-drain capacitances of inverter-amplifier 2),

$$\tau_1 \approx \left[\frac{r_{op1}r_{on1}}{r_{op1}+r_{on1}}\right] * \left[\begin{array}{l}(C_{gdp1}+C_{gdn1})+\\ \frac{Ca*(C_{gsp2}+C_{gsn2}+g_{mp2}r_{op2}C_{gdp2}+g_{mn2}r_{on2}C_{gdn2})}{Ca+(C_{gsp2}+C_{gsn2}+g_{mp2}r_{op2}C_{gdp2}+g_{mn2}r_{on2}C_{gdn2})}\end{array}\right] \quad (9.10)$$

where, the overall resistance at this node is the parallel combination of the NMOS and PMOS output impedances of the inverter-amplifier 1, r_{op1} and r_{on1}. Also, the sampling capacitor Ca is in series with the parallel combination of the capacitances C_{gsn2}, C_{gsp2} and the miller multiplied capacitances $g_{mp2}r_{op2}C_{gdp2}$ and $g_{mn2}r_{on2}C_{gdn2}$. Also, this equivalent capacitance is in parallel with the sum of the capacitances C_{gdp1} and C_{gdn1}.

Next, the time constant (τ_2) at the *output* of the inverter-amplifier 2 is given by,

$$\tau_2 \approx \frac{r_{op2}r_{on2}}{(r_{op2}+r_{on2})} * (C_{gsnL}+C_{gspL}+C_{gdn2}+C_{gdp2}) \quad (9.11)$$

where, the overall resistance at this node is the parallel combination of the NMOS and PMOS output impedances of the inverter-amplifier 2, r_{op2} and r_{on2}. Also, C_{gsnL} and C_{gspL} are the logic gate input capacitances which are in parallel with the miller equivalent capacitances C_{gdp2} and C_{gdn2} at the output

of inverter-amplifier 2. The overall −3dB clock bandwidth for the COM tracker is then given by,

$$\omega_{\mathrm{3dBClock}} = \frac{1}{\tau_1 + \tau_2} \tag{9.12}$$

Inspecting the (9.10) and (9.11), it is clear that the response is dominated by the time constant τ_1 at the *output* of the inverter-amplifier 1. Since Ca (1 pF in this design) is large compared to the parasitic device capacitances and the miller multiplied capacitances by an order of magnitude, the −3dB clock bandwidth of the comparator can then be approximated by,

$$\omega_{\mathrm{3dBClock}} \approx \frac{1}{\frac{r_{op1} r_{on1}}{(r_{op1}+r_{on1})} * C_{tot}} \tag{9.13}$$

where,

$$\begin{aligned} C_{tot} &= C_{gdp1} + C_{gdn1} + \\ & C_{gsp2} + C_{gsn2} + g_{mn2} r_{on2} C_{gdn2} + g_{mp2} r_{op2} C_{gdp2} \end{aligned} \tag{9.14}$$

The −3dB clock bandwidth thus depends on the size (W∗L) of the transistors channel-area and the bias drain current (I_D). As the intrinsic inverter-amplifier gain ($g_m r_o$) is $\propto \sqrt{\frac{W*L}{I_D}}$ and output impedance r_o is $\propto \frac{1}{I_D}$, for a given drain current, I_D, the response time will trade with the output signal swing (using higher voltage gains) driving the logic gates, and hence the noise margins.

9.4 Conclusion

A low-voltage centre-of-mass tracker circuit design using only 1 V supply voltage has been achieved. The significance of this circuit compared to other recent COM tracker circuits is that it does not require floating-gate POLY2 process layer and can be conveniently fabricated in any standard low-cost digital CMOS process technology. Also, although a 6-position COM tracker is presented in this chapter, the novel architecture is very modular and can be easily extended to any number of COM positions. Thus, the precision achievable by the COM tracker circuit at such low supply voltage makes it favourable for applications in mobile robot visual object tracking system.

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