Technology and Device Modeling in Micro and Nano-electronics: Current and Future Challenges*

Andrea Marmiroli, Gianpietro Carnevale and Andrea Ghetti

STMicroelectronics, 20041 Agrate Brianza, Italy andrea.marmiroli@st.com

Abstract
The number of physical effects that have to be taken into account to accurately model and design current and future micro- and nano-electronics devices is continuously increasing. At the same time, the importance of the coupling among them is increasing as well. An accurate simulation of such effects with strong interactions is often non-trivial and in many cases a satisfactory solution is not yet available. Two challenging problems are presented in more detail: the first one refers to the thermo-mechanical problem of silicon oxidation, the second is the electrical coupling which occurs in strained silicon substrate.

1 Introduction

The peculiar driving force of micro- and nano-electronic industry is the shrink of dimensions. This shrink allows to use less silicon and to pack more devices on the same wafer, reducing the production costs. At the same time it results in the increase of transistors' driven current and in the reduction of the total capacitance (as the coupling capacitance remains roughly constant and the capacitance between different layers reduces). Moreover, such shrinkage allows the reduction of the dimensions of the final equipments (cellular phones, portable computers, etc.), increasing the added value of the integrated circuits. Along this shrink path, the minimum features defined by today's technology are in few tens of nanometers range [ITR05].
A second driving force is the integration of different functions in the same integrated circuit or in the same package. This is driven by the reduction of dimensions of the final equipment and by the increase of performances of the same equipments, thanks to faster communications between different blocks.
A further driving force deals with innovation: to increase the added value of integrated circuit, new functions have to be included in the circuits.
Because of this continuous shrinkage, increased integration of functions and new features development, to design and to manufacture semiconductor devices, more and more physical mechanisms, which were previously negligible, have now to be taken into account. Among the most important there are:

* Invited Paper at SCEE-2006

- diffraction and interference effects in lithography
- modeling of coupled electro-thermal phenomena
- electrical behavior of strained silicon
- electro-magnetic coupling between conduction lines which are closer and closer
- resistance of the parasitic interconnect metal lines
- effects of power dissipation

In this paper, in the next section we will present different examples of coupled problems, with a particular emphasis on the modeling aspects. Next two examples are discussed in details to show our modeling approach: the coupling between thermal and mechanical effects which will be discussed in section 3 and the coupling between electrical and mechanical effects presented in section 4, with particular attention to the application of the simulation methodology and tool to a silicon nano-wire MOSFET case.

2 Coupled Problems: general case studies

The first case we address refers to the coupling between electrical and thermal effects which has to be taken into account to understand the phenomena involved in the principles of operation of Phase Change Memories (see [Pir05] and references therein). The principle is described in fig. 1:

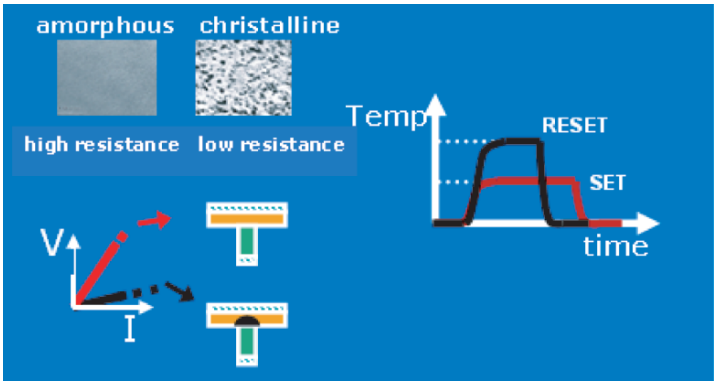

Fig. 1: Phase Change Memory (PCM) description: low and high resistivity of PCM material is associated to the crystalline and amorphous state, respectively. At the left side, bottom part of the figure the schematic pictures of a cross section of the bit architecture are sketched: the "T" shape at the lower side correspond to the low resistance state, with the material partially modified in the crystalline configuration. The upper "T" shape corresponds to the high resistance state, with the material in the amorphous phase.

a) Top left: the storing mechanism of the bit information is based on the different conductivity of the amorphous and of the poly-crystalline phases of the selected material (chalcogenide). The TEM photographs show the two different states.
b) Bottom left: the sensing mechanism exploits the different resistance of the two states. The two different current/voltage characteristics are reported.
c) Right: Finally the writing mechanism based on the joule effect due to the current flow in the chalcogenide film. The temperature profiles to reach the reset (amorphous) and set (crystalline) are reported.

The second case deals with the coupling between electrical and mechanical aspects. The conductivity in semiconductors depends on crystals strain. To accurately model the current flowing in the devices it is necessary to take such strain into account. Fig. 2 shows the impact of this effect (see [Fan05]). At the upper left corner a top view of the layout of an MOS transistor is reported. As shown at the lower right corner, the electrical behaviour depends, besides the obvious W, L values on the total active area dimension LOD (Length Of Device, is given by "2a+L"). The lower left corner shows the stress field in 2 dimensions, while the upper right corner shows the 1-Dimensional cutline for different LOD values.

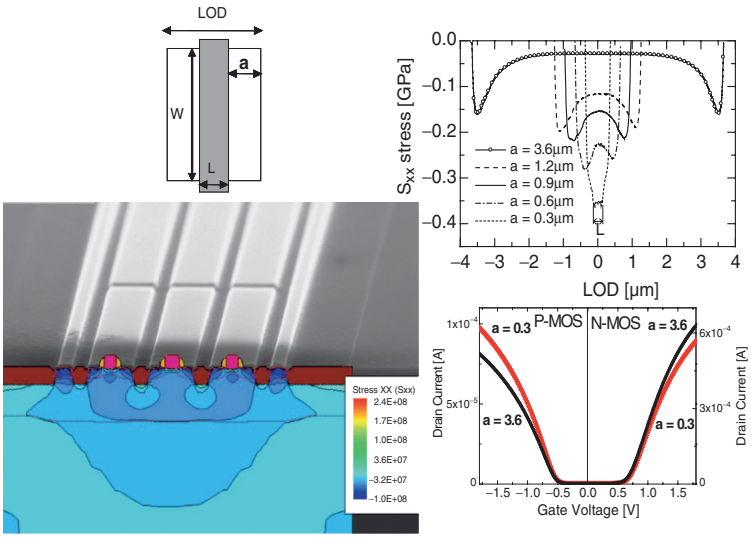

Fig. 2: Strain effect in mosfet transistors

3 Silicon Oxidation study

In this section we will discuss in detail the modeling of silicon oxidation. The modeling of such phenomenon has two main objectives: first to predict the exact shape of silicon and of silicon dioxide, then to evaluate the stress and strain in the two films as the electrical performances, some failure and degradation mechanisms are strongly dependent on the stress/strain level [Rim01], [Tho04]. An accurate modeling of silicon oxidation, has to deal with two linked problems: the diffusion of the oxidizing species in silicon oxide and the solution of the mechanical problem related to the formation of silicon dioxide (whose volume is twice as large as that of the original silicon). These two issues are strongly linked by means of a nonlinear dependence of the main physical quantities which are used in the diffusion-reaction problem: the diffusivity, the reaction rate and the oxide viscosity (respectively $\mathbf{D}^{diff}$, $\mathbf{K}^{react}$, ν^{oxi}) and the stress quantities which are calculated in the mechanical problem: pressure and maximum shear stress (P, σ), as shown in Fig.3.

This coupled algorithm has been published for the first time by Kao [Kao88] et al. who studied the oxidation of concave and convex silicon surfaces. During these studies they observed that the thickness of the oxide growth along cylinders with different radius was very different and that it was not related only to a geometrical effect. It was in particular noticed that the silicon oxide growth in a convex surface was even smaller with respect to the one growth on a flat silicon surface. This is in contrast with the expected consideration based on purely geometrical issues: a convex structure exposes more area than a flat surface, therefore the oxidant flux should be larger. It has been supposed that diffusivity of oxidant in the oxide layer and reaction rate and the silicon interface were both reduced by the stress field inside oxide and normal at the silicon surface. Furthermore, it was also supposed on the basis of previous studies on silica performed by Eyring [Eyr36] that silicon oxide viscosity was affected by the stress inside the material, reducing its value when larger amount of stress were accumulated in oxide. To our knowledge the non-linear relationship between stress and viscosity has not been further investigated.

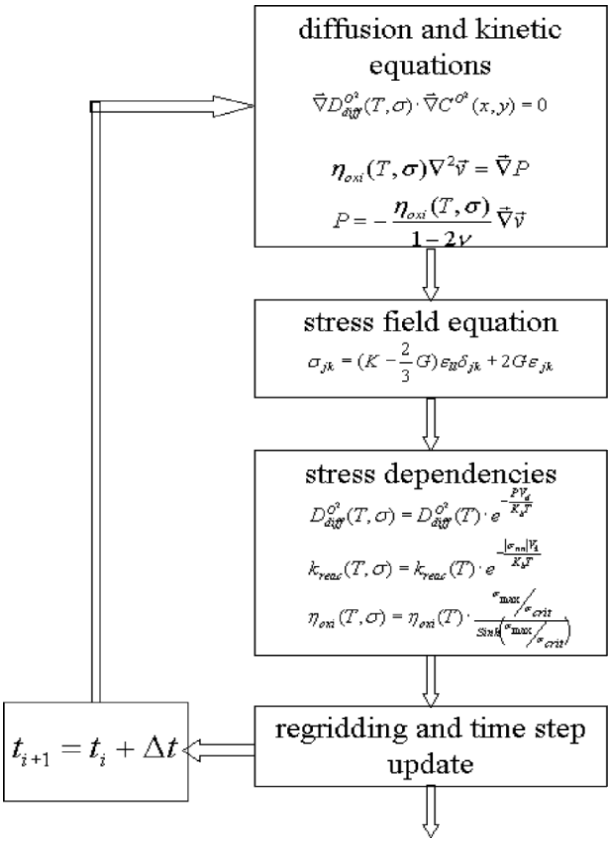

Fig. 3: Solution algorithm coupling oxidation rates and stress calculations

This model has been widely accepted by the scientific community and most of the simulation program adopted it for the correct calculation in two dimensions of the isolation oxide shape in flash memory arrays.
In a more recent past, it has become more and more important to evaluate the stress field distribution not only in the memory cell array, but also in the devices devoted to manage the internal voltage (circuitry or logic circuits). These structures are basically 3D (see fig.4), and are strongly affected by stress in silicon due to the impact on carrier mobility, as highlighted in the next section.

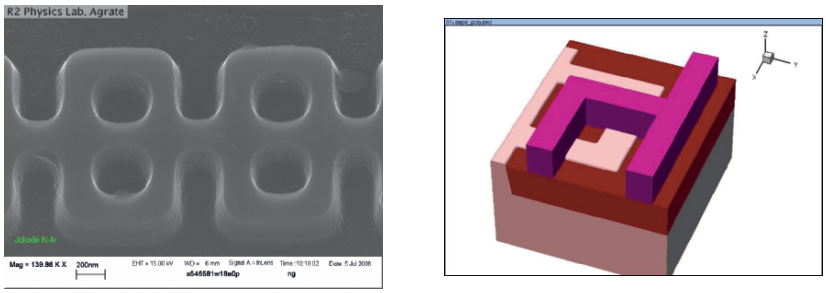

Fig. 4: A SEM picture of a silicon active area (oxide has been removed during stripping operation) and the corresponding 3D structure (pink region are silicon, brown is oxide and violet is poly-silicon material).

Unfortunately, the complexity of this task is largely increased by the computational/ mathematical problem of managing in three dimensions (3D) the moving boundaries describing the silicon-silicon oxide and the silicon-gas interfaces. At the present time, the commercial tool [Syn07] available for the industrial research activity only allows to manage the stress related effects due to thermal mismatch between different materials for a given fixed, but 3D, geometry. The simple continuous model suitable to calculate the strain induced by thermal mismatch between two materials is expressed by the following equation:

$$\varepsilon(x,y) = (\alpha_{sil} - \alpha_{ox}) \times (T_{fin} - T_{ini})$$

where α_{sil},α_{ox} are the linear coefficient thermal expansion for silicon and oxide, respectively, and T_{fin}, T_{ini} are the initial and final temperatures.
The strain, calculated at the interface between the materials, is a isotropic quantity acting in the plane parallel to the same interface.
The results in terms of accuracy and CPU time are largely affected by the solution given by the meshing strategy used in the program.
The state-of-the-art for what regards silicon oxidation in a 3D framework is represented by FEDOS [Tuv06] simulator program, a code which is developed at the University of Vienna and which is still under development. The models implemented in this code are based on a new approach, which calculates the growth of silicon oxide starting from a diffusion-reaction approach. In fact, one assumes the following mechanism: the oxidant species reaches the silicon interface after a diffusion step in silicon oxide and then the reaction with silicon is able to create a new product which is the silicon oxide molecule, consuming a single silicon atom and two oxygen atoms. The equation set is the following:

$$\frac{\partial \rho_{ox}}{\partial t} = D\frac{\partial^2 \rho_{ox}}{\partial x^2} - k\rho_{ox}\rho_{sil}$$

$$\frac{\partial \rho_{sil}}{\partial t} = -k\rho_{ox}\rho_{sil}$$

In the above equations D and k are respectively the diffusion of oxidant in silicon oxide and the reaction rate of oxidant at silicon / silicon dioxide interface, and ρ_{ox}, ρ_{sil} are the density of oxide and silicon, respectively.
For given process parameters (temperature, oxidant gas flow, time) this model incorporates oxidation when dealing in non-stationary regime. The largest difficulty is represented in the modeling of the silicon oxide interface: in fact, in order to solve the mechanical problem it is necessary to define a material interface for each time step after the solution of diffusion-reaction problem and to apply to the interface the correct velocity fields which are derived from the solution of the previous problem.

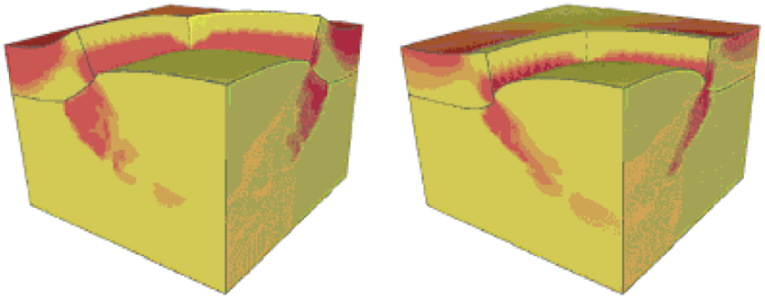

Fig. 5: At the left, the pressure distribution calculated with FEDOS without stress dependent oxidation. At the right stress dependent oxidation is included [Hol05].

4 Transport in NanoWire mosfets study

The second detailed case deals with device simulation of silicon NanoWire MOSFETs. NanoWire MOSFETs (NW MOSFETs) like the one reported in [Yan04] are gaining increasingly popularity due to their superior channel control. This is achieved by reducing the silicon channel to a thin wire surrounded as much as possible by the gate. This makes this kind of devices intrinsically 3D.
In addition, highly non-equilibrium transport still dominated by scattering is expected in this kind of devices [Gil05]. This complex non-stationary/ballistic transport can be accurately accounted for by semi-classical Monte Carlo (MC) simulation. However, for such small devices, quantum mechanical and strain-induced effects play a fundamental role that must be accounted for in conjunction with the real 3D geometry of the device. Therefore it is necessary to include quantum mechanical (QM) and strain effects in the framework of semi-classical 3D MC device simulation.
In this section we report on a new MC simulator (called MC++ [Ghe06]) that solves self-consistently in 1D, 2D or 3D, the Schrdinger Eq. for the QM correction of the potential, while mechanical strain effects are accounted for by an appropriate change

of the band structure. We will show that QM corrected 3D semi-classical Monte Carlo device simulation can accurately address all the above issues.

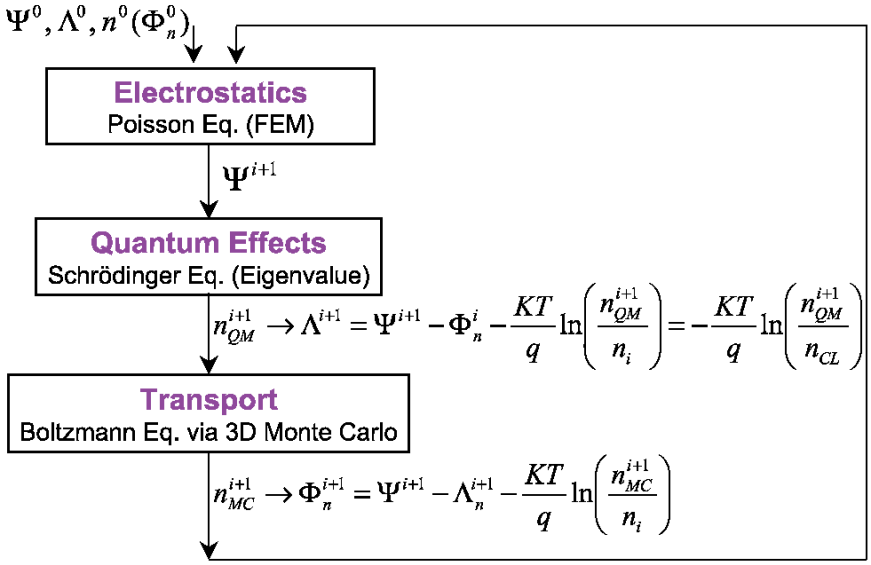

Fig. 6: Main blocks of the simulation program and their interactions. Simulation starts by reading an initial guess computed with conventional programs.

Fig. 6 graphically depicts the interaction among the main blocks of MC++. It solves the Schrdinger Eq. (SE) and the Poisson Eq. (PE) self-consistently with the semi-classical 3D Monte Carlo simulation of carrier transport through an iterative procedure. The linear PE is solved using standard box methods for the potential (Ψ) profile frequently enough (every 2fs) to assure time stability. The solution of the SE provides the QM correction term (Λ) of the potential accounting for charge quantization [Kat03]. Both Ψ and Λ act as driving force in the Boltzmann Transport Equation that is solved for via semi-classical 3D Monte Carlo simulation providing carrier/pseudo-potential profiles to be used in the solution of both PE and SE.
In case of 3D structures, the SE is solved using a "Quasi 3D" approach [Wan04]: the simulation domain is cut in several sections normal to the channel in which the 2D SE is solved for. Then, a continuous 3D description of the QM charge is recovered by interpolating the results of two adjacent sections. This approach is valid as long as the confinement region does not change shape, as in the case of NW-MOSFET [Wan04]. The 2D SE is solved as in [Abr00]. Assuming a rectangular domain with zero boundary conditions the solution can be expanded as $\Phi(x,y) = \sum_{ij}^{N} A_{ij} sin\left(k_x^i x\right) sin\left(k_y^j y\right)$. Hence, the 2D SE can be transformed into a standard eigenvalue problem (solved by highly optimized libraries [And99]) involving the Fourier transform of the potential that can be efficiently computed exploiting FFT algorithms [Fri05].
This methodology can be applied to more arbitrary geometries, as illustrated in Fig. 7 for the case of a circular well with radius R. First, the initial domain (Fig. 7.a) is

mapped onto a uniformly spaced tensor product grid (Fig. 7.b) needed by the FFT algorithm. Then, the energy profile is interpolated on the new grid. Points outside the initial domain are assigned an arbitrary high value (Fig. 7.c, 7.d). This assures no wave penetration outside the original domain.

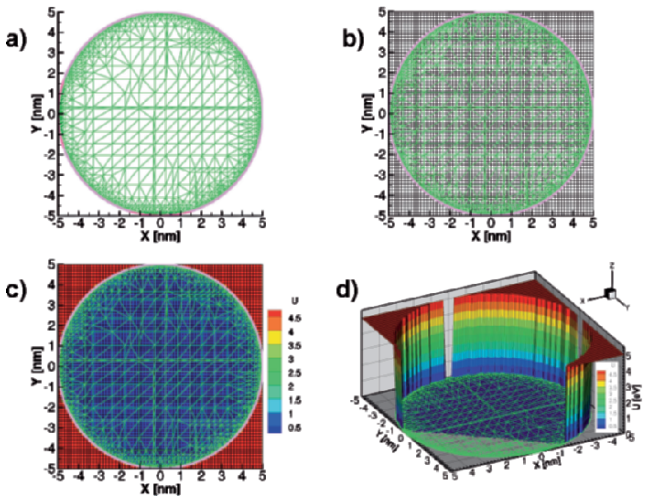

Fig. 7: Numerical solution of the 2D SE in the case of a circular well with R=5nm. a) initial finite element mesh; b) domain map to a uniform tensor product grid; c) contour plot of the energy profile; d) partial 3D view of the energy profile.

For the energy profile in Fig. 7, the 2D SE admits the following analytical solution:

$$\Psi_{mm} = A_{mm} J_m \left(z_{mm} r/R\right) \begin{cases} cos(m\varphi) \\ sin(m\varphi) \end{cases} \tag{1}$$

$$E_{mm} = \frac{\hbar^2 z_{mm}^2}{2m^* R^2} \tag{2}$$

where J_m is the Bessel function of first kind of order m, while z_{mm} is the $n-th$ zero of J_m. Fig. 8 demonstrates the accuracy of this procedure by comparing quantitatively the numerical and analytical solution.

Both physical and phase spaces are discretized with a tetrahedral mesh. This allows for the greatest flexibility in describing device geometry and makes the free-flight equations linear [Bud94], i.e. easy and fast to be solved.

The silicon band structure is computed with the Empirical Pseudo-potential Method [Rid06] that accounts for strain-induced band structure distortion. The Density of State (DOS) is computed by directly calculating the area of the equi-energy surfaces that are also stored in memory to speed up the determination of the state after scattering [Bud94].

Scattering mechanisms are assumed to be isotropic and to depend on strain through the variation of the DOS. Scattering mechanisms include: elastic acoustic phonon scattering, inelastic optical phonon scattering, ionized impurity scattering (isotropic model of [Buf00], impact ionization. Scattering against an interface is treated empirically as a mixture of reflecting and randomizing scattering [Buf00].

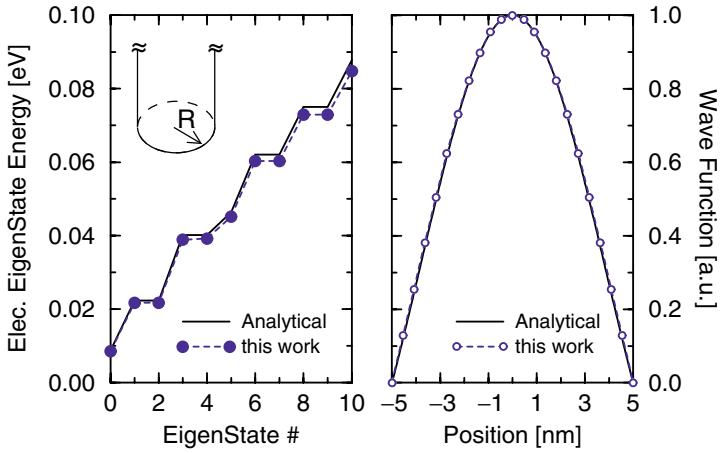

Fig. 8: Validation of the numerical solution of the 2D SE in the case of a circular well with R=5nm. Solid line: analytical solution; symbols: simulation. Left: eigenstate energy; right: first eigenstate wave function.

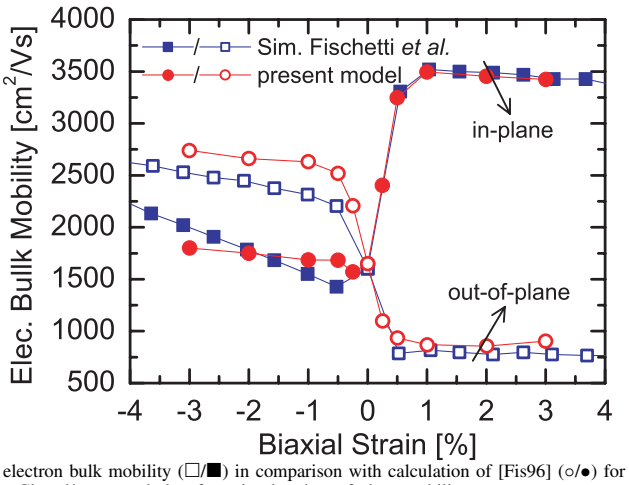

Fig. 9: Simulated electron bulk mobility (□/■) in comparison with calculation of [Fis96] (○/●) for un-doped silicon under biaxial strain. Closed/open symbols refer to in-plane/out-of-plane mobility.

Phonon scattering for electrons and holes has been extensively calibrated to reproduce a large variety of experiments including strain dependent mobility for electrons (Fig. 9) and holes (Fig. 10) [Fan05], [Ghe06], [Fer06].
As an application example we used MC++ to simulate the NW-MOSFET reported in [Yan04] and shown in Fig. 11. The actual iteration scheme is shown in Fig. 12.
The simulation starts by reading an initial bias profile computed with conventional QM, i.e. density-gradient, hydrodynamic simulation (QM HD).
Then, the Poisson and Schrdinger equations are solved self-consistently keeping the pseudo-potential Φ_n^0 found in the initial profile. This step has been introduced to provide a better initial guess for the potential QM correction (Λ^1 in Fig.13) than the one provided by QM HD (Λ^0), thus speeding up convergence.
Please notice in Fig. 13 that Λ^1 significantly deviates from Λ^0. Incidentally, this questions the accuracy of the standard density-gradient approach for 2D/3D cases.

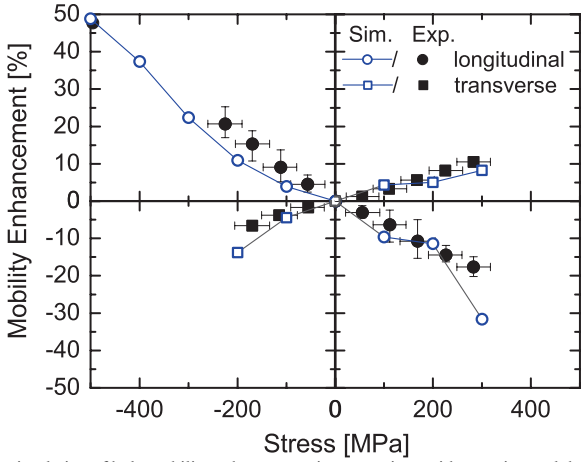

Fig. 10: Monte Carlo simulation of hole mobility enhancement in comparison with experimental data from wafer bending experiments of [Tho04] under uniaxial stress.

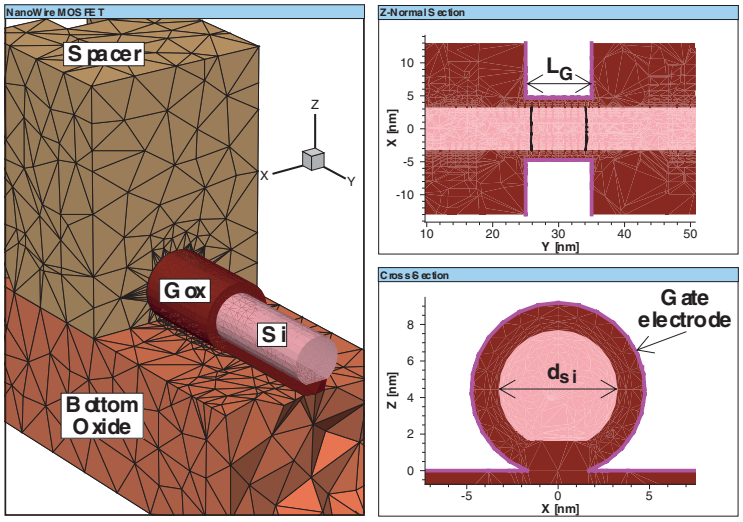

Fig. 11: Silicon NanoWire n-MOSFET reported in [Yan04] and simulated in this work. a) partial 3D view; b) horizontal (z-normal) section; c) channel cross-section. $L_G = 10nm$, $t_{ox} = 1.5nm$, $d_{si} = 6.5nm$. Not all dielectrics are shown.

Indeed, one observes that this density-gradient usually is calibrated to reproduce Poisson-Schrdinger results in 1D. Next, the real iteration loop is entered by performing a Monte Carlo-Poisson self-consistent simulation until a steady-state solution is reached. This is necessary to get a smooth solution for the potential and carrier pseudo-potential to be used in the Schrdinger Eq. solution to update Λ. Notice that any "noise" on $\Psi$and Φdirectly impacts Λ, and, if it is too large, may lead to unphysical results. The loop is then closed by solving the Schrödinger Equation as explained in the previous section. As it is possible to see in Fig. 13, only a couple of iterations are needed to get a stable solution for Λ. Finally, once a stable solution for Λ has

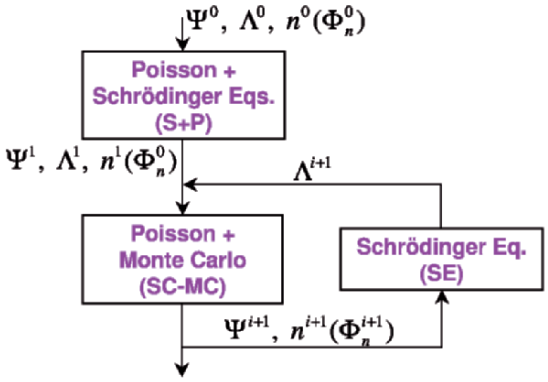

Fig. 12: Schematic representation of the iteration scheme. Convergence is reached after a few iterations. (Notice that $\Phi^1 = \Phi^0$)

been obtained, a longer Monte Carlo-Poisson loop is performed to collect smoother statistics data.

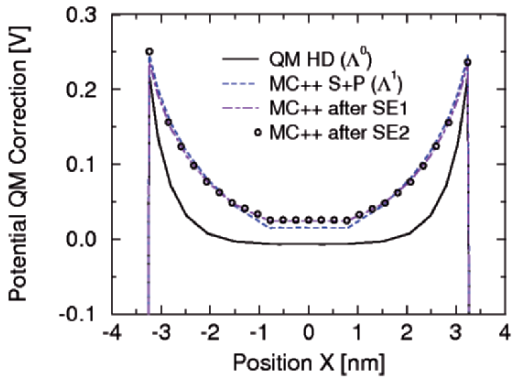

Fig. 13: Evolution of the potential QM correction during iterations. Λ^0 is the initial profile computed with conventional density-gradient hydrodynamic simulation (QM-HD). Λ^1 is the first guess provided by the self-consistent solution of the Schrödinger-Poisson Eq. (S+P).

All simulation results shown in the following have been obtained with the inclusion of strain. The strain tensor symmetry that can be inferred from the geometry of the device under investigation exhibits a biaxial compressive component in the plane perpendicular to the channel direction due to the gate all-around. Consequently, the current flows in the out-of-plane direction benefiting from the effect of mechanical strain (see Fig. 9).

Using the analytical model of [Kao88] and the process information available in [Yan04], the biaxial compressive strain is estimated to be 0.5%.

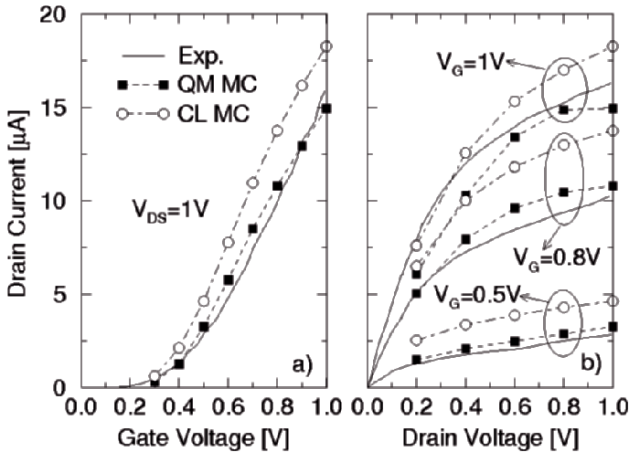

Fig. 14: Comparison of experimental (line) and simulated (symbols) drain current with (QM MC, ■) and without (Classic MC, ○) QM correction. a) trans-characteristics; b) output characteristics.

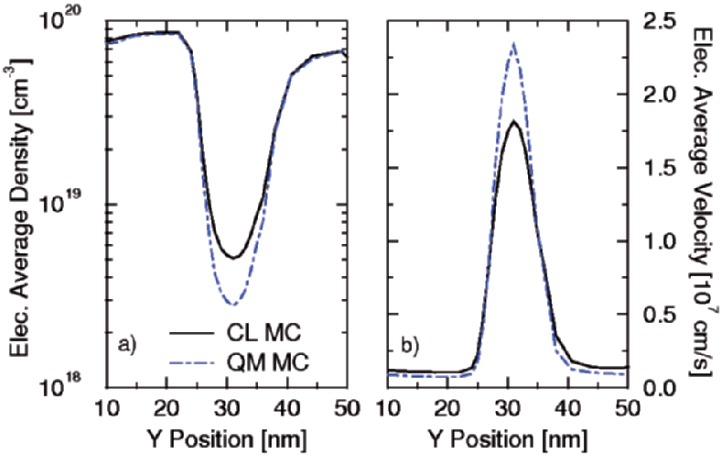

Fig. 15: Simulated electron density (a) and velocity (b) averaged on a channel cross-section as a function of the position for $V_G = 0.5V$, $V_{DS} = 1V$ with (QM MC, dot-dashed line) and without (CL MC, solid line) QM correction.

Simulated drain current with (QM MC) and without (Classic MC) QM correction is compared to experimental data in Fig. 14. A good agreement with experimental data is found only if QM effects are accounted for, while CL MC provides a higher current, as expected. This can be understood by looking at the electron concentration along the channel shown in Fig. 15.a. When QM effects are accounted for, there is a decrease of the free carrier density inside the channel, thus a smaller current, simply

because quantization reduces the number of allowed states. This effect is of particular importance for small devices such as NW-MOSFET. However, this is not the only effect due to quantization. Fig. 15.b also reports the average velocity along the channel in the two cases. When QM effects are accounted for, electrons attain a larger average velocity while transiting in the channel ($\approx +25$ %), thus partially compensating the reduced charge concentration (≈ -50 %). This is due to the particular shape of the carrier space distribution resulting from the inclusion of QM correction. QM effects push electrons away from the interface providing the maximum concentration at the center of the NanoWire. On the contrary, without QM correction the maximum carrier concentration is attained at the gate oxide interface. Thus, in this latter case, electrons will experience more surface scattering (as confirmed by the larger average number of surface scattering per simulated particle), resulting in a smaller velocity.

5 Conclusions

The continuous technology shrinking mandates the need to account for more and more coupled physical effects. We showed how this is the case for two of the most important problems in the technology and device modeling area. These developments require further investment and collaboration between industry, research centers and software vendors, in order to provide accurate tools in time for effective usage.

References

[Abr00] A. Abramo, A. Cardin, L. Selmi, E. Sangiorgi: Two-Dimensional Quantum Mechanical Simulation of Charge Distribution in Silicon MOSFETs, IEEE Trans. on Electron Devices, **Vol. 47**, p. 1858–1863, 2000

[And99] E.Anderson, Z.Bai, C.Bischof, S.Blackford, J.Demmel, J.Dongarra, J.DuCroz, A.Greenbaum, S.Hammarling, A.McKenney, D.Sorensen: LAPACK User Guide, Philadelphia, PA: Society for Industrial and Applied Mathematics, 3^{rd} edition, 1999

[Bud94] J. Bude, R.K.Smith: Phase-Space Simplex Monte Carlo for Semiconductor Transport, Semicond. Sci. Technol., **Vol. 9**, p. 840, 1994

[Buf00] F.Bufler, A.Schenk, W.Fichtner: Efficient Monte Carlo Device Modeling, IEEE Trans. on Electron Devices, **Vol.47, no.10**, p.1891–1897, 2000

[Eyr36] H. Eyring: Viscosity, plasticity and diffusion as examples of absolute reaction rate, Journal of Chemical Physics, pp. 283–291, 1936

[Fan05] P. Fantini, A. Ghetti, G.P. Carnevale, E. Bonera, D. Rideau: A full self-consistent methodology for strain-induced effects characterization in silicon devices, IEDM Tech. Digest, p. 1013–1016, 2005

[Fer06] M. Feraille, D. Rideau, A. Ghetti, A. Poncet, C. Tavernier, H. Jaouen: Low-field mobility in strained silicon with full-band Monte Carlo simulation using kp and EPM bandstructure, Proceedings SISPAD Conference, p. 264–266, 2006

[Fis96] M. Fischetti, S. Laux: Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys, journal of Applied Physics, **vol.80**, p. 2234–2252, 1996

[Fri05] M.Frigo, S.G.Johnson: The design and implementation of FFTW3, Proceedings of the IEEE, **vol.93, no.2**, pp. 216–231, 2005

[Ghe06] A.Ghetti, D.Rideau: 3D Monte Carlo Device Simulation of NanoWire MOSFETs including Quantum Mechanical and Strain Effects, Proceedings SISPAD Conference, p. 67–70, 2006

[Gil05] M.Gilbert, R.Akis, D.Ferry: Phonon-assisted ballistic to diffusive crossover in silicon nanowire transistors, Journal of Applied Physics, **vol.98**, p.094303.1–094303.8, 2005

[Hol05] C.Hollauer, H. Ceric, S. Selberherr: Three-Dimensional Simulation of stress dependent thermal oxidation, Proceedings SISPAD Conference, p. 183–186, 2005

[ITR05] International Technology Roadmap for Semiconductors 2005, *http://public.itrs.net*

[Kao88] D.-B. Kao, J.P. McVittie, W.D. Nix, K.C. Saraswat: Two-dimensional thermal oxidation of silicon II Modeling stress effects in wet oxides, IEEE Transaction on Electron Devices, **vol. 35, n. 1**, p. 25–37, 1988

[Kat03] G.Kathawala, U.Ravaioli: 3-D Monte Carlo Simulation of FinFETs, IEDM Tech. Digest, 2003

[Pir05] A.Pirovano, F.Pellizzer, A.Redaelli, I.Tortorelli, E.Varesi, F.Ottogalli, M.Tosi, P.Besana, R.Cecchini, R.Piva, M.Magistretti, M.Scaravaggi, G.Mazzone, P.Petruzza, F.Bedeschi, T.Marangon, A.Modelli, D.Ielmini, A.L.Lacaita, R.Bez: μ trench phase-change memory cell engineering and optimisation, Proc. ESSDERC, pp. 313–316, 2005

[Rid06] D. Rideau, M. Feraille, L. Ciampolini, M. Minondo, C. Tavernier, H. Jaouen: Strained Si, Ge and Si1-xGex alloys modeled with a first-principle-optimized full-zone kp method, Physical Review B, vol. 74, p. 195208:1–20, 2006

[Rim01] K.Kim, S.Koester, M.Hargrove, J.Chu, P.M.Mooney, J.Ott, T.Kanarsky, P.Ronsheim, M.Ieong, A.Grill, H.-S.P.WongK.Kim, S.Koester, M.Hargrove, J.Chu, P.M.Mooney, J.Ott, T.Kanarsky, P.Ronsheim, M.Ieong, A.Grill, H.-S.P.Wong

[Syn07] Synopsys User manuals, release Y-2006.06

[Tho04] S. E. Thompson, G. Sun, K. Wu, J. Kim, T. Nishida: Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs, Proceedings IEDM Conference 2004, p. 221–224

[ThoArm04] Thompson S.E., Armstrong M., Auth C., Alavi M., Buehler M., Chau R., Cea S., Ghani T., Glass G., Hoffman T., Jan C.-H., Kenyon C., Klaus J., Kuhn K., Zhiyong Ma., Mcintyre B., Mistry K., Murthy A., Obradovic B., Nagisetty R., Phi Nguyen., Sivakumar S., Shaheed R., Shifren L., Tufts B., Tyagi S., Bohr M., El-Mansy Y.: A 90-nm logic technology featuring strained silicon, IEEE Transaction on electron devices, **vol 51, n. 11**, p. 1790–1797, 2004

[Tuv06] *http://www.iue.tuwien.ac.at/99.0.html*

[Wan04] J.Wang, E.Polizzi, M.Lundstrom: A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approxiamtion, Journal of Applied Physics, **vol.96**, pp.2192–2203, 2004

[Yan04] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-H. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y.Li, J.-W. Lee, P.Chen, M.-S. Liang, and C.Hu: 5-nm-Gate Nanowire FinFET, Proc. VLSI Technology Symposium, pp. 196–197, 2004