A 160×120 Edge Detection Vision Chip for Neuromorphic Systems Using Logarithmic Active Pixel Sensor with Low Power Dissipation

Jae-Sung Kong, Dong-Kyu Sung, Hyo-Young Hyun, and Jang-Kyoo Shin

Department of Electronics, Kyungpook National University, 1370 Sankyuk-Dong, Buk-Gu, Daegu 702-701, South Korea
{kongjs, dksung}@ee.knu.ac.kr, hyhyun@knu.ac.kr, jkshin@ee.knu.ac.kr

Abstract. In this paper, a vision chip for edge detection based on the structure of a biological retina is introduced. The chip processes an image in a bio-inspired vision mechanism; therefore, it is proper for the neuromorphic systems. Logarithmic active pixel sensor (APS) was applied to the vision chip. By applying a MOS-type photodetector to the logarithmic APS, we could achieve sufficient output swing for the vision chip in natural illumination condition. A correlated-double sampling technique was applied to the chip for noise suppression. In addition, a CMOS buffer circuit is commonly used for both raw and smoothed images by using additional switches. This structure helps reduce the total number of MOSFETs for a unit-pixel and noise. A vision chip with a 160×120 pixel array was fabricated using a 0.35 μm double-poly four-metal CMOS technology, and its operation was successfully demonstrated.

1 Introduction

Vision systems, which have image sensors and subsequent processing units for a particular purpose, do not use a raw image from an image sensor such as charge-coupled devices (CCD) or complementary metal-oxide-semiconductor (CMOS) image sensors (CIS)[1, 2]. Indeed, they use a filtered image to improve its performance and reduce error rate. In particular, Laplacian filtering, which sends enhanced signal at the edge of an image, is used in many image processing fields such as pattern recognition and the treatment of noisy images (e.g. medical images, silhouettes, and infrared red images) [3-4]. Until now, computer vision systems, which use a CCD camera for capturing an incident image and a general purpose computer for acquisition of useful data from the captured image, have been used as an approach of vision systems. However, these systems are limited in terms of size, power consumption, and speed regarding real applications because they consist of two separate modules for image capturing and processing which do not interact. Recently, bio-inspired vision chips have been developed to overcome these problems [5-13]. The vision chips, which mimic the structure and functions of the human retina, offer several advantages including compact size, high speed, low power dissipation, and dense system integration.

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In order to implement real-time image processing in hardware, first, the time dissipation for image capturing should be minimized. Conventional APS requires light integration time for charge accumulation. In dim illumination condition, this time loss exceedingly increases and it limits continuous operation. On the other hand, logarithmic APS continuously sends output; thus, the combination of the logarithmic APS and the signal processing mechanism of a biological retina helps materialize a high-speed bio-inspired vision chip. Logarithmic APSs have advantages in a wide dynamic range and continuous output. However, they suffer from narrow output swing and low signal-to-noise ratio (SNR), compared with charge accumulation-type APSs [14-16]. In particular, conventional correlated-double sampling (CDS) technique is not adequate for these logarithmic APSs, because they have not a proper reference for pixel noise. Previously reported vision chips based on a logarithmic APS showed limitations in required illumination conditions and SNR due to these mentioned problems [14-16]. In this paper, we applied a metal-oxide-semiconductor (MOS)-type photodetector to the logarithmic APS to achieve a sufficient output swing in natural illumination condition. In order to increase SNR, a CDS technique was applied using a special circuit for a current-reference.

In particular, the vision chips require a resistive network, which functions as Gaussian filtering in digital image processing and a specialized circuit structure for acquisition of both raw and smoothed images [5-13]. These additional circuits can cause additional area consumption, power dissipation and noise. In particular, the design of the structure, as well as the other circuits, is very important for improvement of their final output image quality. Previously, two structures have been used. One type is a voltage division type [6, 8]. The other uses two analog buffers to achieve raw and smoothed images [7, 10]. These structures have their own disadvantages in power and area consumption, signal aliasing and additional noise. To overcome these challenges, a switch-selective resistive network was applied.

2 Theory

2.1 The Principle of Edge Detection

Figure 1(a) shows the structure of a biological retina, which consists of photoreceptors (rods and cones), horizontal cells, bipolar cells, amacrine cells, and ganglion cells. The information falling on the photoreceptors is not sent directly to the brain through the optic nerves, but is instead first processed in a number of ways by a variety of interactions among neurons within the retina. Photoreceptors, horizontal cells and bipolar cells are related to edge extraction and ganglion cells are related to signal digitization [17].

Figure 1(b) shows a simple example of edge extraction. The x-axis represents the position and the y-axis represents the normalized outputs of the photoreceptors, horizontal cells, and bipolar cells, respectively. If a bright light is projected only on the right-hand side of the photoreceptor array, the output of each photoreceptor sends a high-level signal. On the other hand, when a dim light is projected on the left-hand side of the photoreceptor array, the output of each photoreceptor sends a low-level signal. Horizontal cells receive signals from the photoreceptors and spatially smooth

them. Edge signals, resulting from the differences between outputs of photoreceptors and horizontal cells, are yielded through the bipolar cells. The smoothing function, so-called lateral inhibition, is mainly characterized by the resistive properties of the horizontal cells. If the diffusion length, the number of pixels that contributes to the smoothing function, is large, many pixels will be needed to represent the edge signal. A large diffusion length is directly related to a decrease of the spatial resolution. The difference between the outputs of the photoreceptors and the horizontal cells is directly related to the output of the bipolar cells. Generally, the gain of the electrical circuit for the bipolar cells is constant. In that case, the difference between the outputs of the photoreceptor and the horizontal cell will be the most important factor in deciding the magnitude of an edge.

The major advantage of the retinal structure is the speed of operation for edge extraction because all operations which contain the image capturing, smoothing, and differencing are done in a parallel manner. Another advantage is that each function of the structure is simple enough to realize in an electrical circuit; thus, the entire system size can be reduced.

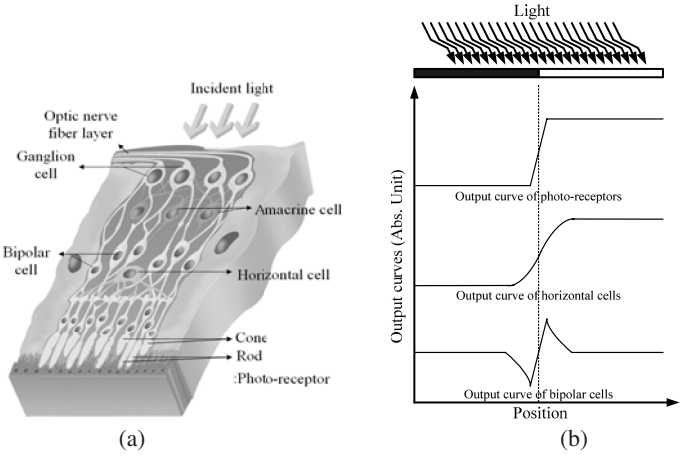


Fig. 1. (a) Structure of biological retina, (b) Principle of edge detection

2.2 Modeling of Retinal Structure in Electrical Devices

Photoreceptors, horizontal cells, and bipolar cells in the retina are the three key elements to embody in the vision chip for edge detection [5-13]. First, a raw image is necessary to extract the edge information. CCDs are useful for sensing the incident image in high quality. However, they require a special process for fabrication; thus, it is impossible to embed other circuits for image processing. The problem of on-chip integration can be solved by using CIS. The function of horizontal can be embodied by using the resistive network, which has been proposed by Mead's research group in which all the photosensors in unit pixels are connected in horizontal and vertical through resistive circuits [2]. The current flow from the higher potential area to the lower potential area contributes to the image smoothing. Smooth processing is done in spatially parallel manner;

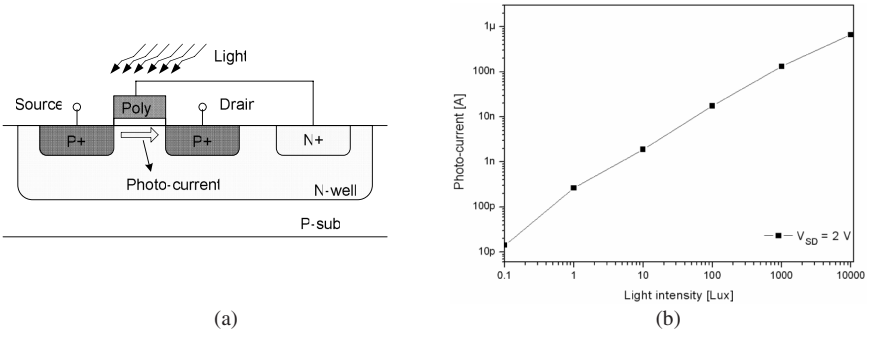
therefore, the mechanism is proper for real-time applications. The function of bipolar cells can be embodied by using differential circuits. In addition, addressing circuits and noise suppression circuits are necessary for practical design.

3 Implementation

3.1 MOS-Type Photodetector

Previous logarithmic APSs have used a photodiode or a photo-BJT as a photodetector [14-16]. They suffer from a narrow output swing range or large area consumption.

Several approaches have been introduced in order to enlarge their output swing. One method increases the resistivity of its diode-connected MOSFET. The disadvantage of this approach is that the increased resistivity is directly related to the amount of noise. By attaching an amplifier (which has a gain of over one) to the logarithmic APS, its output swing can be enlarged. The idea, however, is also not a proper approach, because the amplifier enlarges noise as well as signal. The other approach is to increase the photo-current. The photo-current can be increased by enlarging the size or the sensitivity of a photodetector. Since the enlargement of a photodetector reduces resolution, it may not be a suitable approach. In another approach to enhance the photo-current, photo-BJT has been used, because it has a high sensitivity. It, however, requires large area for fabrication compared with a photodiode.



(a) (b)

Fig. 2. MOS-type photodetector. (a) Circuit structure. (b) Photocurrent-illumination curve at $V_{SD} = 2V$.

We applied a MOS-type photodetector, which is embodied by connecting the gate and the body of a p-type MOSFET, to a logarithmic APS. The channel potential of the MOS-type photodetector varies according to the incident light intensity [18]. The MOS-type photodetector has several advantages, it has a high photo-sensitivity, and furthermore it is compatible with standard CMOS process. In addition, since it has a simple structure, it requires a small area of silicon die. Figure 2 shows the structure of a MOS-type photodetector and its photocurrent-illumination characteristic curves.

By using the MOS-type photodetector in a logarithmic APS, a large output swing could be achieved with a small area occupation.

3.2 Logarithmic APS and Simplified CDS

Conventional CISs use a CDS for noise suppression. However, logarithmic APS rarely used the CDS, because a proper noise-reference could not be achieved. Particularly, previously proposed logarithmic APS with noise reduction function were not adequate for the bio-inspired vision chip because of their complex structure, large area consumption, and sequential way of operation [14-16]. In order to apply a logarithmic APS to a bio-inspired vision chip, mentioned problem should be concerned.

Simplified CDS (SCDS), which was proposed by Kavadias, is a very effective method for noise reduction [19]. SCDS consists of 5 switches (SW1s and SW2s), one capacitor (C1), and two MOSFETs (MP3 and MP4). The key advantage of SCDS is that the circuit only requires one capacitor. Therefore, we can easily minimize area consumption. Compared with the SCDS, conventional CDSs use 2 capacitors for memorizing both the image and reference signals. A detailed operation of SCDS can be found in the Refs [8, 19].

Figure 3 shows the circuit schematic. Logarithmic APS, which consists of MOSFETs MPD, MN2 and MN3, continuously sends a voltage output according to the incident light intensity. MPD represents the MOS-type photodetector. MP1 offers a constant current source for a noise reference. In order to reduce the current variation due to the process variation, the MP1 was divided into 5 MOSFETs, and then they were spread over neighboring pixels. The reference current and the light-induced current are selected by VMODSL. MN1 and MP2 are switches. The area occupation could be reduced by using different types of MOSFETs for signal selection. Two diode-connected MOSFET, MN2 and MN3, were used for the current-voltage conversion. We have achieved the optimum results in output swing and FPN reduction when the number of the diode-connected MOSFETs is two by using SPICE simulation.

The light-induced voltage and the reference voltage are respectively sampled when the SW1 and SW2 are turned on at the drain node of MN2, and then these two signals are subtracted. Figure 4 shows its timing diagram.

3.3 Pixel-Level Adaptive Resistive Circuit (PLARC)

In order to improve an output image, a proper resistive circuit is required. Mead proposed a resistive network using linear resistors [2]. A linear resistor requires large area to make it by using standard CMOS process; thus, we should found another resistive circuit. A resistive circuit using a single MOSFET was also concerned in Refs. [7], [10]. The gate bias for the MOSFET was globally applied a single voltage. The results showed information loss due to the regionally improper bias condition.

The proposed resistive circuit is represented in Figure 3. The circuit consists of 4 MOSFETs, MP5, MN4, MN5, and MN6. The source/drain nodes of MP5 are respectively interconnected between itself and its neighboring pixel. The states of these nodes are exchanged according to potentials of these two pixels. The biasing circuit which consists of MN4, MN5, and MN6 keeps the source-gate potential difference on at particular level although source and drain potentials regionally varies. The uniform source-gate potential difference keeps the resistivity of resistive circuits at a certain value. It helps reduce information loss. The size of our proposed circuit was 13.5×17 μm^2 by using a 0.35 μm double-poly four-metal (2P4M) standard CMOS process.

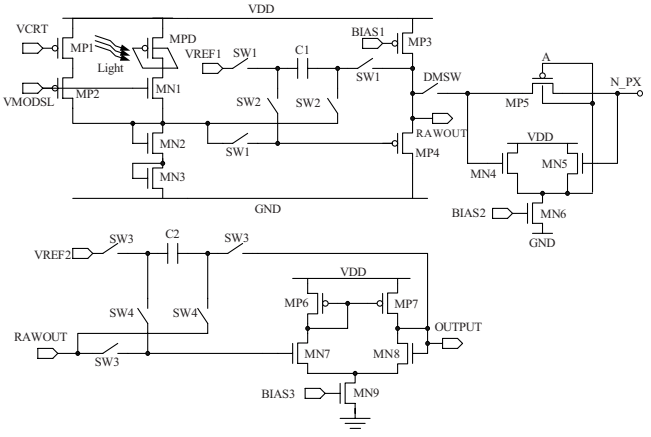


Fig. 3. Circuit schematic

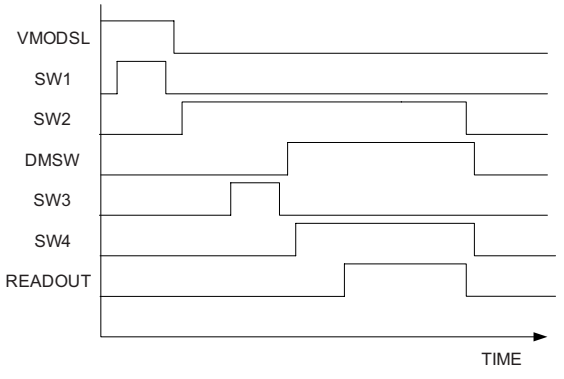


Fig. 4. Timing diagram

3.4 Switch-Selective Resistive Network

The proposed edge detection circuit uses only one source follower circuit, which consists of MP3 and MP4, for both raw and smoothed images [12]. Each image can be selected by a switch DMSW. This switch was embedded in each unit-pixel to connect a neighboring pixel via a resistive circuit; i.e. the node RAWOUT sends a raw image when the switch is open. RAWOUT, otherwise, sends a smoothed image when the switch is closed. The first advantage of this structure is low power dissipation, because the switch does not require extra current for its operation. Raw and smoothed images can be achieved at the same node; thus there is no additional noise between these two images. This is the second advantage. The third advantage is that the structure requires less area. The proposed circuit requires only a small additional switch. It is very area-effective method compared with a vertical resistive circuit or buffers of previous types [6, 9, 10]. The fourth advantage is that there is no aliasing problem

between the raw and the smoothed images, because the resistive network is physically disconnected when the switches are open. The other advantage is that the characteristic of resistive network is easily controlled, due to their simple structure. This advantage helps apply various resistive circuits to the vision chip in order to obtain a proper image for a particular purpose. Structural disadvantages include additional switching noise and control complexity, but they are not serious problems. The differential circuit extracts the edge signal from the raw and the smoothed images by switching SW3 and SW4. Figure 4 shows the timing diagram for the proposed circuit.

3.5 Circuit Arrangement: Pseudo 2-D Structure for Resolution Improvement

Conventional vision chips are built 2-dimensional (2-D) resistive network for high operation speed and mimicking a more retina-like model. A unit-pixel of this kind chip contains a photodetector, a noise suppression circuit, resistive circuits and a differential circuit. Particularly, both the noise suppression and the differential circuit require a capacitor for storage of analog data. Thus, the unit-pixel requires large area, approximately 100×100 μm^2 [6-9]. For the reason of area consumption, this type of vision chip suffers from critical lack of resolution. Figure 5(a) shows the structure of a vision chip with 2-D resistive network.

We have tried to solve this problem by restructuring circuits for photo-sensing and image processing. Figure 5(b) shows our structure. The signal processing circuits were separated from photo-sensing circuit; then the signal processing circuits were used in row-parallel. This structure has two advantages and disadvantages, respectively. The advantages are high resolution and low power dissipation. High resolution is caused by the small size of a unit-pixel. Lower power dissipation is caused by less current paths through the overall chip. The disadvantages are possibility of data loss and low operation speed. Data loss can be appeared at horizontal or vertical edges according to the direction of resistive network. However, this problem can be compensated when the resolution is sufficiently improved. The other disadvantage of low operation speed can be a problem when the illumination condition is dim because of their long exposure time; however, the problem can be minimized when the proposed logarithmic APS is used.

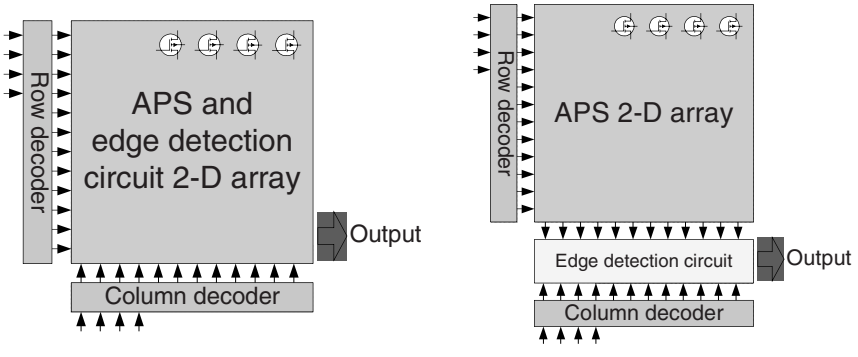


Fig. 5. Structures of a bio-inspired CMOS vision chip. (a) Conventional structure with 2-D resistive network. (b) Resolution-improved structure.

4 Measurement

The bio-inspired vision chip with 160×120 pixels was fabricated by using a 0.35 μm 2P4M standard CMOS technology. The chip size was 5×5 mm^2. The chip contained 144 pads for input/output (I/O), a 2-D logarithmic APS array, two decoders for pixel selection, and a one-dimensional (1-D) edge detection circuit. An optical lens (focal length of 16 mm, f number of 1.4) was mounted in a C-mount format for the projection of an input image onto the chip surface. Figure 6 shows the layout of the fabricated chip.

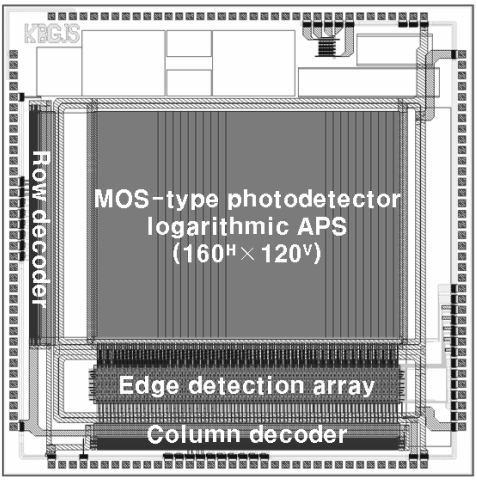
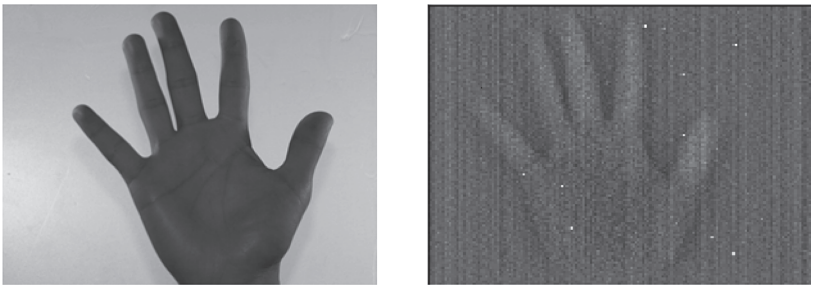


Fig. 6. Layout of the fabricated chip



(a) (b)

Fig. 7. Experimental results. (a) Input image, (b) Output Image.

Figure 7(a) and (b) show an input image and an output image, respectively. The output swing was approximately 100 mV for the second order of contrast difference. Over 300 mV of maximum swing was measured for an edge over 5 decades. The average noise of a final image was approximately 10.6 mV. Compared with previous

results using a logarithmic APS, it is very improved results. The operation speed of the vision chip is also improved compared with chips using a charge-accumulation type APS. For our chip, the required operation time containing noise reduction and edge detection was only 600 micro-seconds. This time may be reduced by optimizing the circuit. In the case of the illumination condition of a thousand lx, a commercial CMOS APS requires at least several milliseconds for charge accumulation, but our chip could send information in real-time. It helps detect and search a region-of-interest (ROI) for real applications. Approximately 25.6 mW of power consumption was investigated.

5 Conclusion

Previously, many silicon retina chips have been introduced. Their parallel signal processing based on a biological retina is proper for neuromorphic systems. However, the photo-sensor based on charge-accumulation limits their functional advantage of continuity. In order to overcome this problem, several silicon retinas based on logarithmic APS have been proposed; however, their results suffered from low SNR and small output swing for real applications.

In this paper, a vision chip using MOS-type photodetector logarithmic APS with low power dissipation and low noise was introduced. By using the logarithmic APS and SCDS, low noise image could be continuously obtained. Higher quality of final output image could be obtained by using PLARC, compared with previous results. SSRC helped reduce noise and power consumption. In addition, the resolution of the proposed vision chip could be largely improved without extra cost-increase by using the pseudo 2-D structure. The proposed vision chip has been fabricated by using a 0.35 μm 2P4M standard CMOS process, and then successfully demonstrated. By applying the proposed vision chip to neuromorphic systems, real-time and robust computation with a compact hardware would be achieved.

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