10 Mixers

I know that I know nothing.
Socrates

As discussed in Sect. 2 and illustrated in Fig. 10.1, mixers convert the high RF frequency to a low IF frequency in receivers and vice versa in transmitters. The corresponding circuits are referred to as down- and up-mixers, respectively. An LO signal provided by a VCO is required for this operation. For capacity reasons and to allow coexistence with other standards, the data has to be transmitted by means of a high RF carrier frequency, whereas in the receiver, low IF frequencies are required for simple baseband processing.

The requirements for down-mixers, e.g. regarding gain and noise, are more challenging than for up-mixers. This is attributed to the fact that the signal to noise ratio in transmitters is high because of the strong signal power being locally available. In the following sections we focus on down-mixers. However, the gained insights can be mapped to up-mixers.

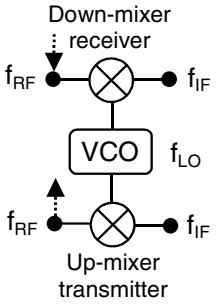


Fig. 10.1. Mixers used for frequency down- and up-conversion in receivers and transmitters

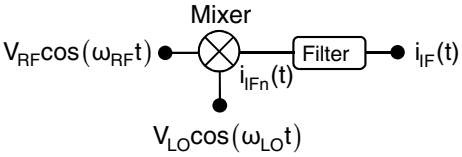


Fig. 10.2. Mixer fed by sinusoidal RF and LO signals yielding the IF signal

10.1 Nonlinearities and Mixing Products

The nonlinearities of a device as a function of a time variant LO signal are instrumental for mixing [Maa03]. Undesired frequency components have to be filtered out. Referring to the schematic depicted in Fig. 10.2, the voltage across any nonlinear device may be represented by

$$v_{IF}(t) = V_{LO}\cos(\omega_{LO}t) + V_{RF}\cos(\omega_{RF}t). \tag{10.1}$$

In this simple model, we assume that the mixer acts as a signal adder. The current characteristics of nonlinear device can by described by a Taylor-series:

$$i_{IF}(t) = c_0 + c_1 v_{IF}(t) + c_2 v_{IF}^2(t) + c_3 v_{IF}^3(t) \ldots + c_n v_{IF}^n(t). \tag{10.2}$$

The constants c_n are obtained by inspection of the individual current versus voltage characteristics of a device. For FETs these properties may be based on a quadratic function, whereas for BJTs, the dependency might rather be exponential. With Eqs. (10.1) and (10.2) we get

$$\begin{aligned} i_{IF}(t) = {} & c_0 + c_1\left[V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t)\right] + \\ & c_2\left[\begin{array}{l} \frac{V_{RF}^2}{2}\left(1+\cos(\omega_{RF}t)\right) + \frac{V_{LO}^2}{2}\left(1+\cos(\omega_{LO}t)\right) + \\ \frac{V_{RF}V_{LO}}{2}\left(\cos(\omega_{LO}t+\omega_{LO}t) + \cos(\omega_{LO}t-\omega_{LO}t)\right) \end{array}\right] + \ldots \end{aligned} \tag{10.3}$$

These mixing components are illustrated in Fig. 10.3 up to the 4th order. The amplitudes of the frequency components tend to become smaller with increased n, since the mixing efficiency strongly decreases towards higher mixing products as found by inspection of the c_n components in Eq. (10.3). Moreover, we can deduce that the $\omega_{RF}-\omega_{LO}$ and $\omega_{RF}+\omega_{LO}$ components have the potential to provide the highest gain compared to other intermodulation products. Thus, these frequency components are frequently used for the down- and up-conversion, respectively. The conversion loss is defined by

$$L_c = \frac{P_{IF}}{P_{RF}}, \tag{10.4}$$

where P_{RF} and P_{IF} denote the RF and IF power. Conversion gain G_c can be reached for active mixers. We have to consider that the LO power is usually much higher than the RF power, because the RF signal is attenuated by propagation in the air, whereas the LO is locally fed. Thus, the $n \cdot f_{RF}$ components are relatively weak, whereas the undesired $n \cdot f_{LO}$ components are strong and have to be filtered. The suppression of undesired components is measured by means of the port to port isolations, which can be important in systems, where we want to avoid compression of circuits following the mixer. Important are high LO to IF and LO to RF isola-

tions since the LO power is very strong. In circuits targeted for low power consuming applications, the conversion efficiency

$$\eta_c = \frac{P_{IF}}{P_{RF} + P_{LO} + P_{dc}} \tag{10.5}$$

is an important measure, which includes also the LO power P_{LO} and the DC power P_{dc}. Similar to amplifiers, we may define the following figure of merit for mixers:

$$\text{FOM} = \frac{f_c[\text{GHz}]}{f_t[\text{GHz}]} \cdot \frac{G_c[\text{dB}]}{\text{NF}[\text{dB}]} \cdot \frac{\text{IIP3}[\text{dBm}]}{P_{dc}[\text{dBm}]} . \tag{10.6}$$

The first term in the equation describes the centre operation frequency f_c with respect to the f_t of the used technology, the second factor considers the conversion gain to noise figure ratio and the third term relates the large signal properties to the consumed DC power. Several modifications of Eq. (10.6) can be found in the literature. Optionally, the representation of the large signal properties by means of P_{1dB} instead of the IIP3 may be reasonable as well. The use of non-logarithmic values may be an option. For wideband mixers, f_c may be substituted by the bandwidth.

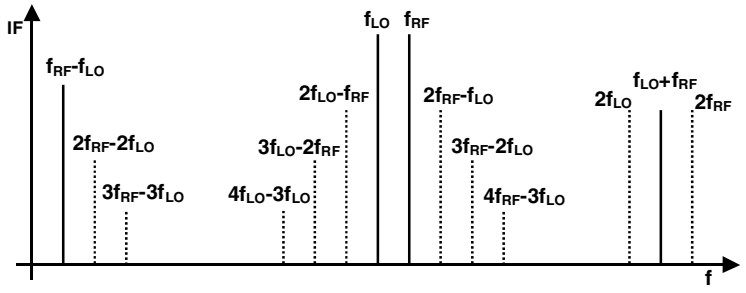


Fig. 10.3. Part of IF mixer spectrum generated by nonlinear mixing of f_{RF} with f_{LO}

Table 10.1. Element variations of 90 nm n-channel SOI MOSFET

Element	Var. as f(V_{gs})	Var. as f(V_{ds})	Nonlinear effect
R_g, R_d, R_s	Small values, negligible dependency		Very weak
R_{gs}	<20%		Weak, path dominated by series C_{gs}
C_{ds}	<10%		Weak since dominated by par. R_{ds}
C_{gd}	30%		Weak miller effect due to mixer bias, dominated by C_{gs}
C_{gs}	30%	25%	Moderate
r_o	6 Ω–2 kΩ		Strong
g_m	0–80 mS		Very strong

w_g=64 µm as function of voltage variations from 0 to 1 V on condition that other voltage is fixed at optimum value between 0 and 1 V

Transistors are frequently used as the nonlinear devices in monolithically integrated mixers. VLSI IC processes feature no optimised mixing diodes as commonly applied in discrete and off-chip implementations. These mixing diodes would require special doping profiles. For cost reasons such doping profiles are rarely available.

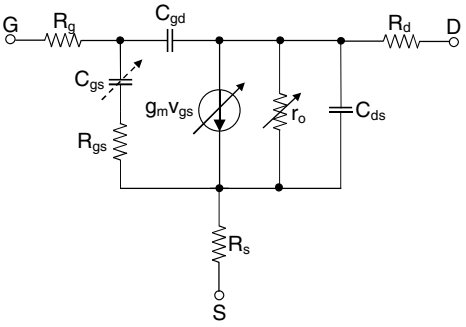


Fig. 10.4. Simplified equivalent circuit of MOSFET and dominant nonlinear elements

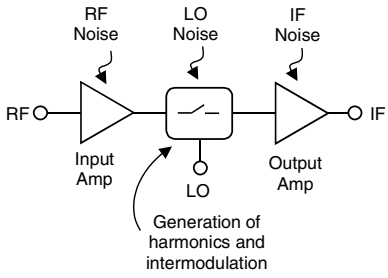


Fig. 10.6. Generic schematic of mixer, nonlinearities are generated by switching

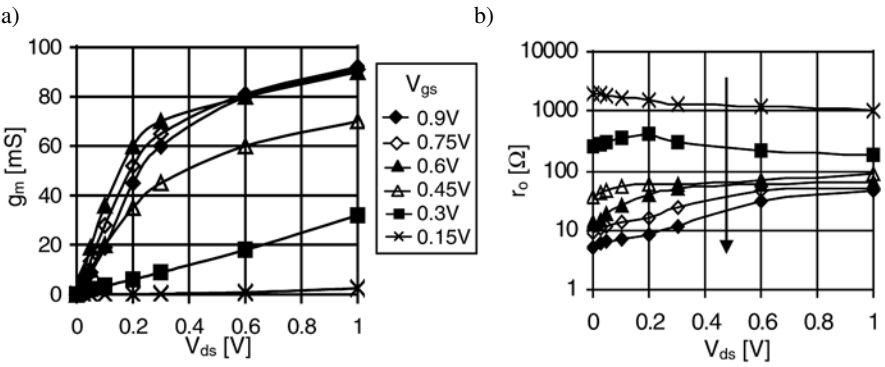


Fig. 10.5a,b. Dominant nonlinearities of 90-nm SOI n-channel FET: **a** transconductance; **b** channel resistance

The nonlinear characteristics of FETs can be a function of V_{gs} and or V_{ds}. In Fig. 10.4, the simplified equivalent circuit of a FET is shown indicating the major nonlinearities. To gain first insights concerning the potential for mixing, the relative variations of the equivalent circuit elements for 90-nm n-channel SOI MOSFET are measured and listed in Table 10.1. As expected, no nonlinearities are associated with the contact resistances R_g, R_d and R_s. Weak changes of less than 30% are observed for the elements R_{gs}, C_{ds}, C_{gd} and C_{gs}. The highest nonlinear properties are expected for g_m dominating the current source properties of the device followed by the output impedance r_o. Figure 10.5 illustrates the characteristics of the latter two parameters. According to Table 5.5, $r_o = r_{ds} \,||\, R_{ds}$. In the triode

or resistive region, where $V_{ds}<V_{ds,sat}$, r_o is determined by R_{ds}, which can become quite low at high V_{gs}.

The optimum choice of the type of nonlinearity depends on the application. The g_m properties allow higher conversion gain, whereas the r_o characteristics yield higher linearity with respect to unwanted frequency components. The final choice depends on the desired tradeoff between frequency bandwidth, required LO power, DC power and the requirements in terms of gain/loss, linearity and output power.

10.2 Noise

According to Sect. 4.3.5, the system noise figure of receivers is mainly determined by the noise figure of the LNA located in front of the mixer. Given that the LNA has a high gain, the contribution of the mixer noise on the system noise figure is weak. Consequently, mixer noise is usually not critical as long as the noise is not exorbitantly high.

The analysis of mixer noise requires nonlinear noise modelling, which is complex [Maa93, Hul93]. Since the theories have to be approximated heavily to give analytical results, it is not a surprise that the agreement between theories and practice is limited. Many conclusions based on the analysis are contradicted by experimental results of other researchers. Thus, from didactic point of view, no noise modelling is treated in this book. However, the designer should keep the insights concerning linear noise in mind. Since the nonlinear noise is based on the conversion of linear noise sources, the minimisation of linear noise sources helps to lower the nonlinear mixer noise. Corresponding design strategies involve the proper choice of the transistors, the bias, the RF input matching and the avoidance of resistive parasitics. The generic schematics depicted in Fig. 10.6 may help to understand the noise sources qualitatively. In a thought experiment, we may split the mixer circuit into three parts: an RF input amplifier, the section where the nonlinearity is generated, and an IF amplifier. Sure, in practice all three parts may merge. Given that the gain of the virtual RF amplifier is high, the noise is determined by the input stage. The linearity of the active mixers may be determined by the IF stage, which has to handle the gain of the preceding stages. By the way, the noise estimation of resistive mixer is easy. In good approximation, the noise equals the resistive loss.

For details concerning mixer noise, the interested and scientifically motivated reader is referred to literature: FET gate-pumped transconductance mixers [Tie83], MOS Gilbert cell [Ter99, Hey04], SiGe Gilbert cell [Joh05], and distributed Gilbert cell mixer [Saf05].

Compared to the theoretical analysis, practical measurements can be accomplished relatively easy. As discussed in Sect. 15.4.6, both the single side band (SSB) and double side band (DSB) noise figures are used for the characterisation.

10.3 Topologies

An overview of the most important approaches used for mixers is sketched in Fig. 10.7. Either active or passive topologies can be employed [Maa03, Rob04, Maa98]. As mentioned beforehand, active topologies mainly apply nonlinear transconductances and channel resistances. The differential pair and Gilbert cell mixers are based on nonlinearities associated with hard switching. Passive mixers mainly exploit the nonlinearities of resistances and reactive elements at zero DC channel voltage yielding excellent large signal properties at zero DC power. Drawback of passive approaches is their loss, which has to be compensated by amplifiers drawing DC power.

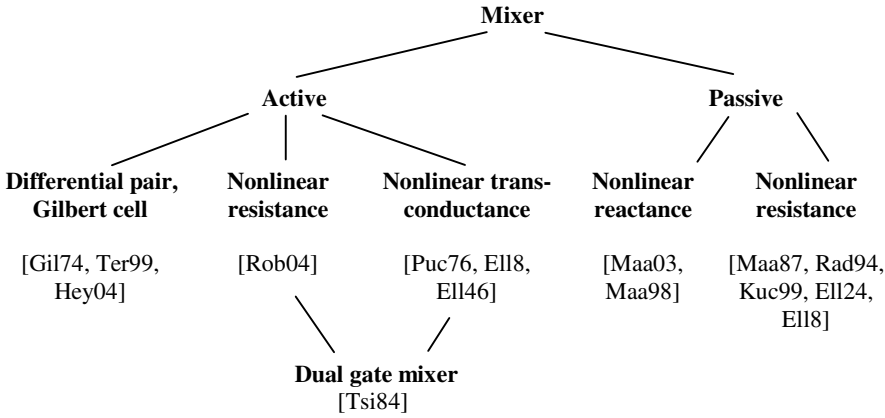


Fig. 10.7. Overview of mixer topologies and corresponding nonlinearities

10.3.1 Transconductance-Pumped Mixers

The simplified equivalent circuit of a g_m-type down-mixer FET is shown in Fig. 10.8. As outlined in Table 10.2, either the gate or the drain voltage can be pumped by the LO signal leading to a time-variant function of g_m, which generates the nonlinearities required for mixing.

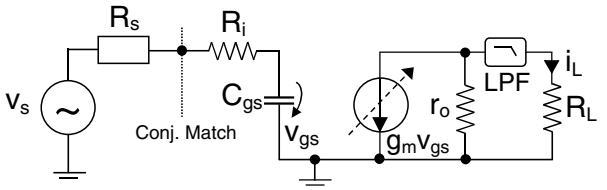
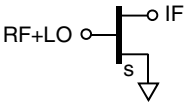
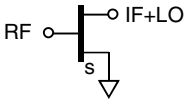
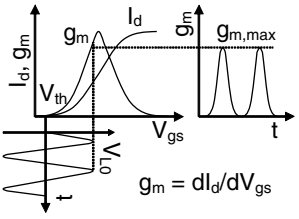
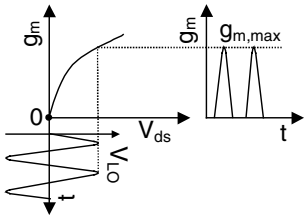


Fig. 10.8. Simplified equivalent circuit of transconductance FET down-mixer, $g_m=f(V_{gs}, V_{ds})$: nonlinear transconductance, R_i: gate resistance $f(R_g, R_{gs})$, r_o: drain source impedance, C_{gs}: gate source capacitance, R_s: source impedance (could also be complex), R_L: load, compare [Ell14] © IEEE 2004

Drain pumped down-mixers have been demonstrated in practice [Dar96, Bur76, Ell14] and analysed theoretically [Beg79]. They have a remarkable advantage compared to the gate pumped approach. The RF and the LO frequency, which are close together, are injected at different ports simplifying the filtering and improving the LO to RF and RF to LO isolation. The isolation is limited by the C_{gd} of the transistor. Biased at the transition between the linear and saturation region, the transistor provides the most pronounced level of nonlinearities. Aggressively scaled CMOS FETs have the advantage that they have very small drain source saturation voltage $V_{ds,sat}$ of below 0.2 V. Thus, no V_{ds} bias voltage is necessarily required since the applied LO power is sufficient to drive the device from zero V_{ds} to $V_{ds,sat}$.

Table 10.2. Overview of transconductance pumped mixers

	Gate pumped	**Drain pumped**	
Circuit schematics			
Functional principle			
V_{ds} bias	> $V_{ds,\,sat}$	$V_{ds,sat}$	0 V possible if $V_{ds,sat}$ small
V_{gs} bias	V_{th}	$V_{gs}>V_{th}$	
Non-linearity	$g_m=f(V_{gs})$	$g_m=f(V_{ds})$	
Reference	[Kwo93, Orz03, Puc76, Ell46]	[Dar96, Bur76, Beg79]	[Ell14]

The gate pumped mixer operates in the saturation region with V_{gs} biased close to the threshold voltage V_{th}, where maximum non-linear variations of g_m are achieved [Puc76, Kwo93, Orz03].

For both the gate- and drain-pumped mixer, the LO signal leads to a time variant g_m, which may be approximated by a cosine function with 50% duty cycle. In this context, compare the g_m waveforms according to Table 10.2. Only the positive half-wave of the cosine exists since $g_m(t)$ equals zero for $V_{gs}\leq V_{th}$ and $V_{ds}\leq 0$, respectively, assuming n-channel devices. The conversion gain mainly depends on the fundamental component of $g_m(t)$. Following the derivations of [Maa03], the fundamental component can be calculated by Fourier series [Bro91] yielding

$$g_{m1}(t) = \frac{1}{2} g_{m,max} \cos(\omega_{LO} t) \tag{10.7}$$

where $g_{m,max}$ represents the peak value of $g_m(t)$. The RF input port of the mixer is fed with the RF voltage

$$v_{s,RF}(t) = V_{s,RF} \cos(\omega_{RF} t)\,, \tag{10.8}$$

where V_{sRF} denotes the RF input amplitude. For maximum power transfer we demand conjugate matching at the node between the RF input and the mixer circuit. According to Fig. 10.8, at the gate node, we can find the following identity concerning the gate currents:

$$v_{gs,RF}(t) \cdot \omega_{RF} C_{gs} = \frac{v_{s,RF}(t)}{2R_i}, \tag{10.9}$$

where R_i is a function of R_{gs} and R_g. The overall load current including the RF, LO and mixing frequencies is given by

$$i_d(t) = -g_m(t) \cdot v_{gs,RF}(t) \cdot \frac{r_o}{r_o + R_L}\,. \tag{10.10}$$

With Eqs. (10.7)–(10.10), the trigonometric theorem

$$\cos(\omega_{LO} t) \cdot \cos(\omega_{RF} t) = \frac{1}{2}\cos\left[(\omega_{RF} - \omega_{LO})\,t\right] + \frac{1}{2}\cos\left[(\omega_{RF} + \omega_{LO})\,t\right], \tag{10.11}$$

and assuming ideal filtering of all frequency components except the IF frequency $\omega_{IF} = \omega_{RF} - \omega_{LO}$, we obtain an IF drain current of

$$i_{L,IF}(t) = -\frac{g_{m,max} V_{s,RF} \cos(\omega_{IF} t)}{8\omega_{RF} C_{gs} R_i} \cdot \frac{r_o}{r_o + R_L}\,. \tag{10.12}$$

With Eqs. (10.11) and (10.12), the IF load power yields

$$P_{L,IF} = \frac{1}{2}\left|i_{L,IF}\right|^2 R_L = \frac{g_{m,max}^2 V_{s,RF}^2}{128\pi^2 \omega_{RF}^2 C_{gs}^2} \cdot \frac{R_L r_o^2}{R_i^2 (r_o + R_L)^2}\,. \tag{10.13}$$

Assuming conjugate input matching, the available RF input power can be calculated by

$$P_{s,RF} = \frac{V_{s,RF}^2}{8R_i}\,. \tag{10.14}$$

Finally, with Eqs. (10.13) and (10.14) we can compute a conversion gain of

$$G_c = \frac{P_{L,IF}}{P_{s,RF}} = \underbrace{\frac{g_{m,max}^2}{16\omega_{RF}^2 C_{gs}^2}}_{k_1} \cdot \underbrace{\frac{R_L r_o^2}{R_i \left(r_o + R_L\right)^2}}_{k_2} = k_1 \cdot k_2 \,, \tag{10.15}$$

where the factor $\frac{g_{m,max}^2}{C_{gs}^2}$ is bounded by the maximum ω_t of the applied transistor.

Equation (10.15) gives first fruitful insights for optimisation. To achieve high conversion gain or low loss, an optimum bias point and LO power has to be applied providing maximum $g_{m,max}$. As expected, the conversion gain decreases with frequency. The first term k_1 is independent on the transistor gate width w_g because both $g_{m,max}$ and C_{gs} are proportional to w_g. The second term k_2 indicates the existence of a maximum with respect to w_g. Since r_o and R_i depend on w_g, an optimum w_g as a function of R_L, r_o and R_i can be found. As long as $R_L < r_o$, the gain can be enhanced by increasing R_L.

10.3.1.1 CMOS Drain Pumped Transconductance Mixer at 30–40 GHz

As an example, a passive drain pumped transconductance mixer topology with zero DC power consumption is presented, which is well suited for short channel FET technologies [Ell14]. The circuit is implemented in IBM 90 nm VSLI SOI CMOS technology.

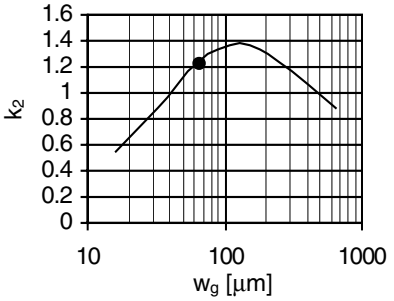


Fig. 10.9. Calculated characteristics of second term of Eq. (10.15) vs gate width at V_{gs}=0.4 V, V_{ds}=0.7 V and R_L=50 Ω, compare [Ell14] © IEEE 2004

Low loss is achieved by reusing the LO power to drive the device RF-wise into the active region despite the fact that the DC drain source voltage is zero. An n-channel FET with a w_g of 64 µm is used. As indicated in Fig. 10.9 and in accordance with Eq. (10.15), this size is well suited to reach a high conversion gain at 50 Ω terminations, since the coefficient k_2 is close to its maximum. The maximum k_2 is reached at twice the transistor width. However, large transistors increase the

feedback capacitance C_{gd} thereby degrading the LO to RF isolation. Furthermore, the chosen w_g allows relatively simple impedance matching and filtering at the specified RF, LO and IF centre frequencies of 35 GHz, 32.5 GHz and 2.5 GHz, respectively.

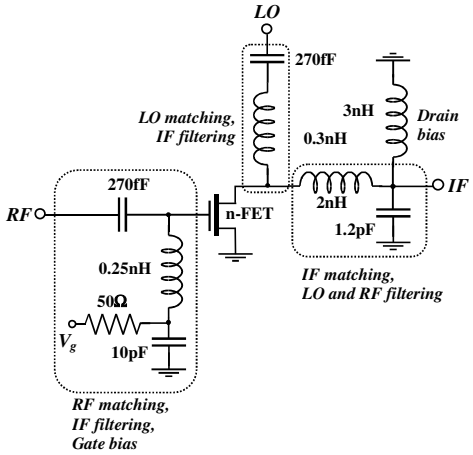


Fig. 10.10. Simplified circuit schematics of passive drain pumped transconductance mixer, compare [Ell14] © IEEE 2004

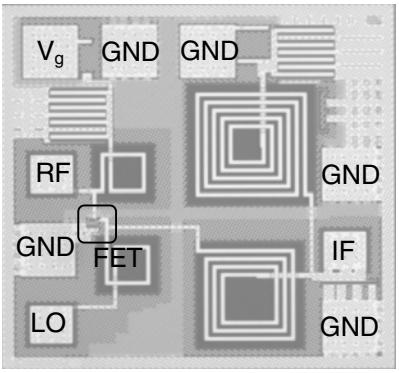


Fig. 10.11. Photograph of mixer MMIC with overall chip size of 0.5×0.47 mm^2, compare [Ell14] © IEEE 2004

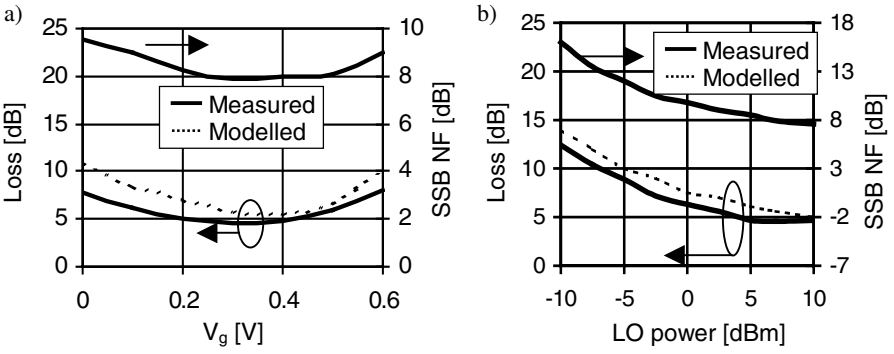


Fig. 10.12a,b. Conversion loss and single side band noise figure (SSB NF), f_{RF}=35 GHz, f_{LO}=32.5 GHz, f_{IF}=2.5 GHz, V_{ds}=0 V: **a** vs V_g, LO power=7.5 dBm; **b** vs LO power, V_g=0.3 V, compare [Ell14] © IEEE 2004

The characteristics of g_m vs V_{ds} and V_{gs} of the FET are shown in Fig. 10.5a. For V_{gs} smaller than 0.9 V, $V_{ds,sat}$ is around 0.2 V. Thus, even with zero V_{ds}, only small LO power is required to drive the transistor into the transition between linear and saturation region, where the highest level of nonlinearity is generated. The plot indicates that for low V_g, this nonlinear transition is reached with minimum LO power. However, this decreases the maximum value of g_m and increases the

conversion loss as shown in Eq. (10.15). Thus, V_g is a design tradeoff between minimum LO power and conversion gain. As demonstrated later, measurements and simulations reveal an optimum V_g of approximately 0.4 V.

The simplified circuit schematics of the mixer and a photograph of the IC are shown in Figs. 10.10 and 10.11. To decrease losses and to maximise the conversion efficiency of the mixer, the number of lossy passive elements is kept as low as possible. Where feasible, the LC filter elements are reused for impedance matching, bias feeding and DC blocking. At the RF port, a highpass filter is applied for suppression of the IF frequency, RF impedance matching, DC blocking and feeding of the gate bias. The lowpass filter at the IF port allows IF impedance matching and filtering of the LO and RF frequencies. At the LO port, a bandpass filter is used for the filtering of the IF frequency, LO matching and DC blocking. A grounded bias choke inductance defines a V_{ds} DC voltage of zero.

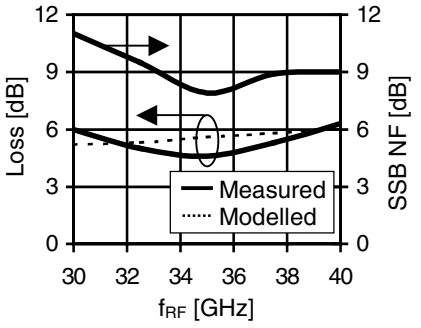


Fig. 10.13. Conversion loss and SSB NF vs RF frequency, LO power=7.5 dBm, f_{IF}=2.5 GHz, V_g=0.3 V, V_{ds}=0 V, compare [Ell14] © IEEE 2004

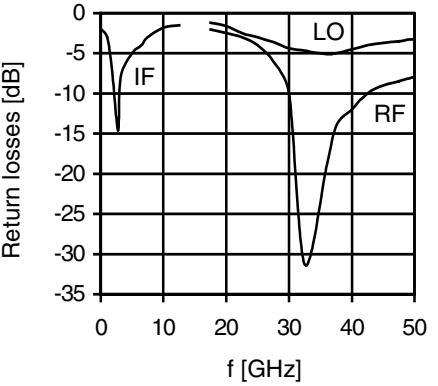


Fig. 10.14. Return losses at V_g=0.3 V and V_{ds}=0.2 V representing an average large signal point, compare [Ell14] © IEEE 2004

In Fig. 10.12, the conversion loss and the SSB NF vs V_g and LO power are depicted. The lowest loss and SSB NF are measured at V_g=0.3 V. At an RF frequency of 35 GHz, an LO frequency of 32.5 GHz, an IF frequency of 2.5 GHz and an LO power of 7.5 dBm, a conversion loss of 4.6 dB and a SSB NF of 7.9 dB are measured. The increase of the conversion loss and the SSB NF with decreased LO power is relatively weak. At an LO power of only 0 dBm, the conversion loss of 6.3 dB and the SSB NF of 9.7 dB are still low enough for low power consuming WLAN applications. The properties vs frequency are shown in Figs. 10.13 and 10.14. The measured IIP3 vs LO power is plotted in Fig. 10.15. The IIP3 rises with increased LO power since the maximum signal swing increases. At an LO power of 0 dBm and 7.5 dBm, the IIP3 is -2 dBm and 2 dBm, respectively. The 1 dB input compression points is –6 dBm at an LO power of 7.5 dBm. In Table 10.3, the minimum port isolations are listed.

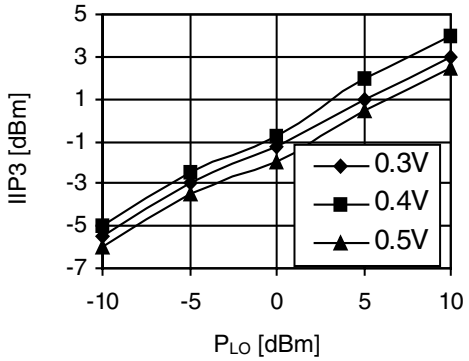


Fig. 10.15. Measured IIP3 at V_{ds}=0 V for different V_g, compare [Ell14] © IEEE 2004

Table 10.3. Measured minimum port isolations

LO to IF	RF to IF	LO to RF	IF to RF
45 dB	48 dB	11 dB	37 dB

LO power: 0–10 dBm

10.3.2 Gate-Pumped Resistive Mixer

People who only see the positive aspect of a development are called technicians.
Werner Mitsch, German aphorist

Resistive mixers are based on the variation of the channel conductance determined by R_{ds} vs the gate voltage, which in turn is a function of the LO power. Due to the fact that passive resistive mixers do not have to handle a significant DC current, the maximum possible input level of resistive mixers can be larger than for the active counterparts. Consequently, high linearity is achievable for resistive mixers. Because of their passive and resistive nature, resistive mixers have a relatively high conversion loss. Several resistive mixers have been reported in literature [Maa87, Sch98, Zir01, Ver00]. Theoretical aspects have been addressed in the rigorous work presented in [Sal71].

Resistive mixers can be implemented in different circuit configurations. Due to their low complexity, those shown in Fig. 10.16 are well suited for monolithic integration. The overall mixer loss may be described by

$$L_{overall} \approx L_{RF-filter} \cdot L_{IF-filter} \cdot L_{switch} \cdot L_{conv}\,, \tag{10.16}$$

with the insertion loss of the RF and IF filters $L_{RF\text{-}filter}$ and $L_{IF\text{-}filter}$, the insertion loss caused by the non-ideal on- and off-resistance of the FET L_{switch}, and the conversion loss due to the nonlinear mixing process L_{conv}.

The nonlinear resistance can be realised by a resistive (cold) FET, which can either be connected in series or shunt configuration. In ideal case, the nonlinear FET acts as a switch with an on-resistance Z_{on} of zero and an off-resistance Z_{off} of ∞. Note that switching is always associated with strong nonlinearities. Suppose ideal switching transitions, where an infinite number of harmonics and intermodu-

lation products are generated due to the square-wave multiplied with any input signal.

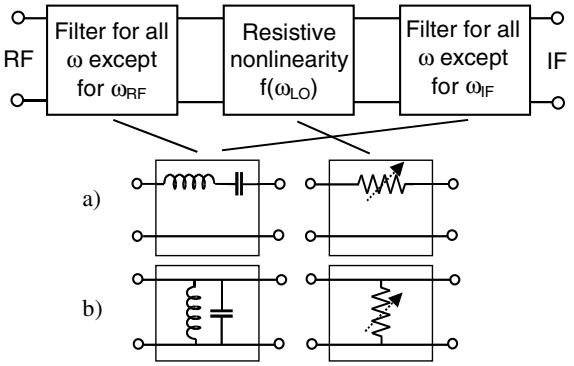


Fig. 10.16a,b. Resistive mixers, nonlinear resistance can be realised in: **a** series or; **b** shunt configuration, filters can be implemented as series bandpass (**a**) or shunted bandpass (**b**), compare [Ell8] © IEEE 2005

The simplified equivalent circuit of a resistive FET, the corresponding values of the equivalent circuit elements in on- and off-mode, and the channel resistance of a transistor with w_g=64 µm are shown in Figs. 13.3 and 13.4. Depending on the impedance conditions of the environment, the nonideal characteristics of Z_{off} or Z_{on} can dominate the losses. Thus, an optimum w_g exists as demonstrated later. Following [Sal71, Lin01], the loss associated with the non-ideal on- and off-resistances may be estimated by

$$L_{switch} = 1 + 2\left[1 + \sqrt{1 + \left(\frac{1}{\delta}\right)^2}\right] \tag{10.17}$$

with

$$\delta = \left|\frac{Z_{on}}{Z_{off}}\right|. \tag{10.18}$$

The best conversion efficiency at given LO power is achieved at a DC bias corresponding with an average value between Z_{on} and Z_{off}. By considering a sinusoidal LO signal with sufficient magnitude to drive the channel resistance from an on- to off-state, we observe the time variant characteristics of R_{ds} as illustrated in Fig. 10.17.

With the assumption that the LO power is much higher than the RF power, the nonlinear R_{ds} can be expanded into a Fourier series:

$$R_{ds}(t) = R_{ds0} + 2\sum_{n=1}^{\infty} R_{dsn} \cos(n\omega_{LO}t) \tag{10.19}$$

with R_{ds0} as the fundamental and R_{dsn} the n^{th} Fourier coefficient of R_{ds}. If we neglect the parasitics of the FET and the filters and if we assume ideal filtering of all frequencies except the desired RF and IF frequencies, the theoretical conversion loss can be calculated by [Sal71]

$$L_{conv} = \frac{\text{available input power}}{\text{output power}} = \frac{1+\sqrt{1-\varepsilon^2}}{1-\sqrt{1-\varepsilon^2}}. \tag{10.20}$$

Assuming a rectangular shape of R_{ds} with duty cycle Θ as outlined in Fig. 10.17 yields

$$\varepsilon = \frac{R_{ds1}}{R_{ds0}} = \frac{\sin(\Theta \cdot \pi)}{\Theta \cdot \pi}. \tag{10.21}$$

This identity can be found in conversion tables of Fourier series [Bro91]. Due to the passive nature of the device, and depending on the shape and the duty cycle Θ, the factor ε ranges from unity to zero. In theory, this results in a loss of zero and ∞, respectively. Unfortunately, an ε of unity can never be reached since the optimum source resistance R_{source} and output resistance R_{out} of the mixer related by [Bar67, Bäc99]

$$R_{source} = R_{out} = \sqrt{R_{ds0}^2 - R_{ds1}^2} \tag{10.22}$$

would approach zero. Consequently, in practice, no impedance matching would be possible.

Filters are required to minimise the signal energy converted to unwanted frequencies. These filters can be implemented as series or shunted bandpass filters, in ideal case providing an open or a short, respectively, for all frequencies except the desired RF or IF frequency. Compared to series bandpass filters, the shunted bandpass filters have two significant advantages. Both the capacitor and the inductor are shunted at one port. Thus, a significant part of the substrate losses are short-circuited, thereby yielding a higher quality factor. Furthermore, due to the shunted inductance, the input and output of the resistive FET are DC grounded. Hence, a DC drain source voltage of zero is provided to keep the device within the resistive region. As a benefit, no additional area consuming and lossy bias elements are needed. Consequently, bandpass filters in shunt configuration are favourable. The filters can be designed by $\omega_{RF} = \frac{1}{\sqrt{L_{RF}C_{RF}}}$ and $\omega_{IF} = \frac{1}{\sqrt{L_{IF}C_{IF}}}$.

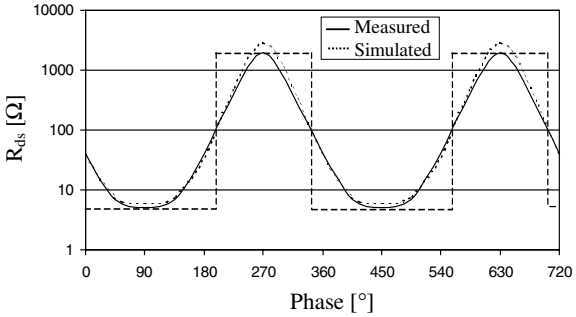


Fig. 10.17. Nonlinear characteristics of channel resistance according to Fig. 10.5b when driven by sufficiently high LO signal, V_g=0.45 V, compare [Ell8] © IEEE 2005

For many system applications, differential mixers are advantageous. Figure 10.18 depicts the topology of a differential resistive mixer. The double balanced structure consists of four passive FETs. In the simplified schematic, the impedance matching, bias and filter networks are not included. For details concerning such mixers, the reader is referred to the literature [Lee04, Cir05]. A loss and SSB NF of around 7 dB have been demonstrated [Pih01].

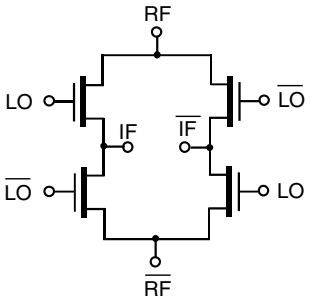


Fig. 10.18. Simplified schematic of double balanced resistive mixer

10.3.2.1 Gate-Pumped CMOS Resistive Mixer at 26.5–30 GHz

In Figs. 10.19 and 10.20, the simplified circuit schematic and chip photograph of a gate-pumped resistive CMOS mixer are shown, which has been implemented in IBM 90-nm SOI technology [Ell8]. The circuit is optimised for RF and IF centre frequencies of 28 GHz and 2.5 GHz, respectively. Figure 10.21 depicts the simulated characteristics of the filters. The RF filter has a loss $L_{RF\text{-}filter}$ of 1.1 dB at the RF frequency and a suppression of the IF frequency of 18 dB. A loss $L_{IF\text{-}filter}$ of 2.5 dB at the IF frequency and an IF to RF and LO isolation of higher than 22 dB are simulated for the IF filter.

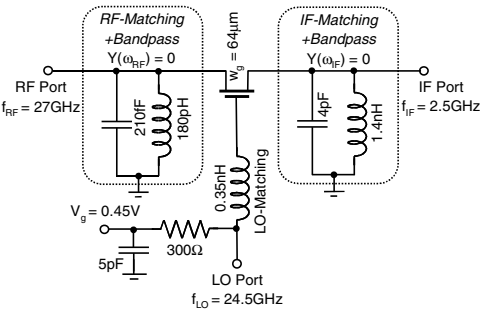


Fig. 10.19. Simplified circuit schematic of resistive mixer, compare [Ell8] © IEEE 2005

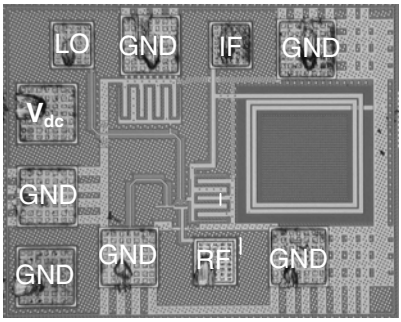


Fig. 10.20. Photograph of mixer with chip size of 0.4 × 0.3 mm^2, compare [Ell8] © IEEE 2005

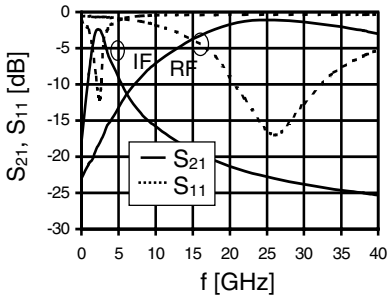


Fig. 10.21. Simulated S-parameters of filters including parasitics, compare [Ell8] © IEEE 2005

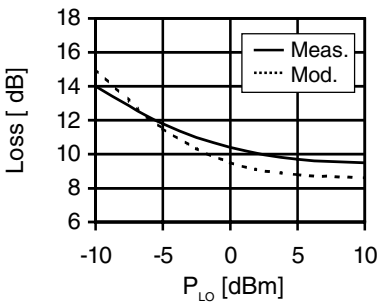


Fig. 10.22. Conversion loss vs LO power at RF frequency of 27 GHz, IF frequency of 2.5 GHz and V_g=0.45 V, compare [Ell8] © IEEE 2005

By using Eqs. (10.17), (10.18), (13.1) and (13.2), and the values of the FET according to Fig. 13.4a, we can estimate a loss of L_{switch}≈0.5 dB at 27 GHz. Due to the small l_g and the low associated parasitics, this value is relatively low, even at such high frequencies. As illustrated in Fig. 10.17, we can extract a duty cycle of θ=35%. Thus, from Eqs. (10.20) and (10.21), a conversion loss of 5.9 dB can be calculated. From Eq. (10.16) we can now estimate the theoretical overall mixer loss amounting to

$$L_{overall}\,[\mathrm{dB}] \approx 1.1\ \mathrm{dB} + 2.5\ \mathrm{dB} + 0.5\ \mathrm{dB} + 5.9\ \mathrm{dB} = 10\ \mathrm{dB}. \qquad (10.23)$$

We can conclude that the nonlinear mixing has the highest contribution to the overall loss, followed by the insertion loss of the IF filter. For a wide LO power range, minimum loss is achieved for a DC voltage of approximately 0.45 V. Hence this bias is fed.

In Fig. 10.22, the conversion loss is plotted vs LO power. The minimum measured loss is 9.7 dB at an LO power of 10 dB, which is close to the theoretical value of 10 dB obtained from the analytical calculations. The loss raises only slightly with decreased LO power. At a low LO power of 0 dB, a conversion loss of 10.3 dB is measured making the circuit also well suited for low power applications. Usually, resistive mixers require high LO power to achieve low loss. The measured 3 dB RF frequency bandwidth ranges approximately from 26.5 to 30 GHz. In Fig. 10.23, the return losses are shown at the small signal DC operation point. The measured SSB NF and IIP3 are plotted in Fig. 10.24. As expected from resistive mixers, the SSB NF is close to the value obtained for the conversion loss. A minimum noise figure of approximately 11 dB is measured at 5 dBm LO power. Up to 10 dBm, the IIP3 increases with LO power. At 0 dBm and 10 dBm LO power, high values of 12.7 dBm and 20 dBm, respectively, are measured. The port isolations are summarised in Table 10.4. Due to the suppression of the filters relatively high port isolations are achieved.

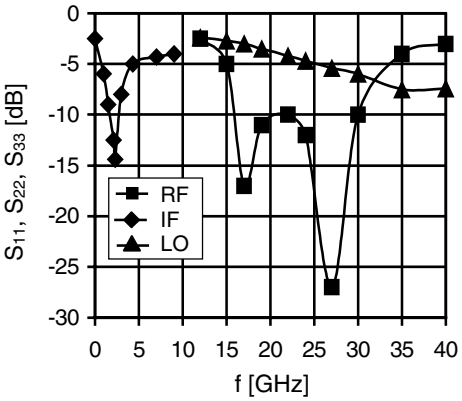


Fig. 10.23. Return losses in small signal operation point at bias of 0.45 V, compare [Ell8] © IEEE 2005

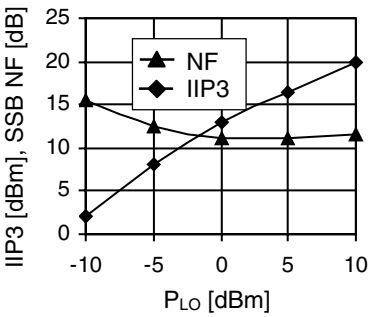


Fig. 10.24. Measured input third intercept point and single side band noise figure at bias of 0.45 V, f_{RF}=27 GHz and f_{IF}= 2.5 GHz, compare [Ell8] © IEEE 2005

Table 10.4. Port isolations

	LO to IF	**LO to RF**	**RF to IF**	**IF to RF**
Measured	22 dB	24 dB	33 dB	25 dB
LS model	30 dB	20 dB	26 dB	17 dB

f_{RF}=27 GHz and f_{IF}=2.5 GHz, 5 dBm LO power, 0.45 V bias

10.3.3 Differential Pair and Gilbert-Cell Mixer

The mixers presented in this section are those most frequently used in commercial integrated systems. Among the significant advantages are the differential LO and IF paths, high gain and large bandwidth. In Fig. 10.25, the simplest configuration based on a differential pair is shown. By means of an RF tranconductance stage, the RF input voltage is converted into an RF current, which is commutatively switched by the upper two transistors. We assume ideal switches with duty cycle of 50% and square-wave characteristics with magnitude of 1 and –1. Consequently, the current through the RF stage is multiplied with the function [Bef03, Bro91]

$$h(t) = \frac{4}{\pi} \cdot \sum_{n=0}^{\infty} \frac{(-1)^n}{2n+1} \cdot \sin\left[(2n+1)\,\omega_{LO} t\right]. \tag{10.24}$$

By Fourier analysis, the conversion transconductance of the desired $\omega_{IF} = \omega_{RF} - \omega_{LO}$ component can be calculated yielding

$$g_{m1} = \frac{2}{\pi} \cdot g_m \,. \tag{10.25}$$

The magnitude of the associated conversion voltage gain can be approximated by the well-known relation of

$$a_{v1} = g_{m1} \cdot Z_L \,. \tag{10.26}$$

From the latter equations we can deduce the following design issues:

- The voltage gain and the associated conversion gain can be raised by increasing of g_m, which is a function of the applied bias and transistor width.
- We can increase the conversion gain also by making Z_L large. As for amplifiers, the maximum gain is bounded by stability constraints. High values of Z_L increase the RC constant at the output leading to a limitation of the maximum operation frequency and bandwidth. Consequently, the optimum value of Z_L has to be traded off for maximum gain on one hand, and maximum operation frequency and stability on the other hand. Since Z_L determines the signal swing in the IV curves, Z_L impacts also the linearity. By the way, how can we get a high Z_L? One solution is the to use a parallel LC network with $\omega_{IF} = \frac{1}{\sqrt{LC}}$. Neglecting resistive losses, this LC network provides an impedance of ∞. In this context, the reader is referred to Sect. 11.5.3, where a similar load is used for a cross-coupled oscillator. One disadvantage might be the large size of the inductors. An alternative solution is to use a compact parallel RC load [Bef03]. However, it is clear that the latter load provides lower RF conversion gain than the LC approach.

- Harmonics and intermodulation products are generated by switching. The mentioned LC filter is suited to suppress undesired frequencies at the output.
- The LO power has to be high enough to allow switching with a rectangular-like function. Symmetrical switching is advantageous regarding the shape of the RF signal and the associated properties in terms of linearity, noise and conversion gain.

Compared to the single balanced differential pair, the Gilbert cell illustrated in Fig. 10.26 offers one advantage. It is a doubled balanced topology [Gil74]. LO-wise the outputs of the two single-balanced mixers are connected inversely parallel, whereas IF-wise the outputs are in parallel. Consequently, at the output, the LO signal is cancelled, whereas the IF amplitude is doubled. Thus, the doubled balanced mixer provides a high level of LO to IF isolation, which can be important in systems. We may consider the potential to saturate following circuits such as the IF amplifiers or the analogue to digital converters by means of the high LO power. Disadvantages of double balanced mixers are the high power consumption. The drawback of double supply current is made up for double output power. However, we have to consider the voltage headroom required for the additional current source. All signal ports of the Gilbert cell mixer are fully differential, which is not the case for the single balanced topology. This may not necessarily be an advantage since the RF input provided by the LNA may anyway be single ended.

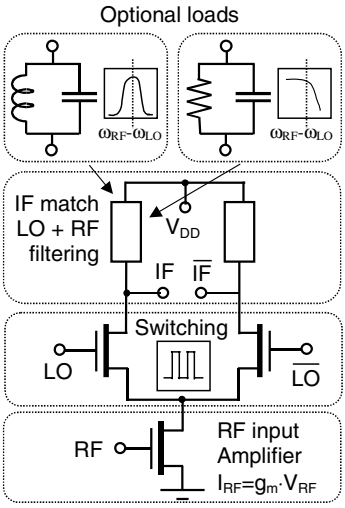


Fig. 10.25. Differential pair (single balanced)

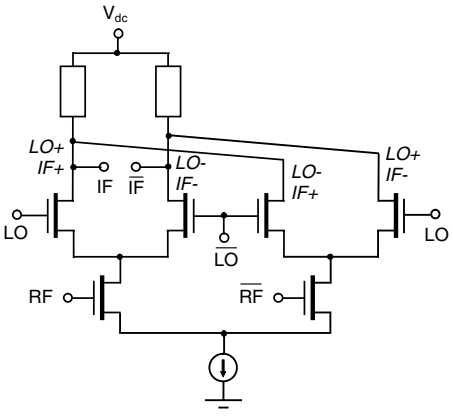


Fig. 10.26. Gilbert cell (double balanced)

10.3.3.1 CMOS Differential Pair Mixer Covering 27–33 GHz

A 27–33-GHz CMOS differential down-mixer is treated now [Ell10], which uses the same CMOS SOI technology as the mixers presented in the preceding sections. The circuit schematic and the chip photograph are shown in Figs. 10.27 and 10.28. An LC bandpass filter is applied as load and for impedance matching. The gates of the FETs are biased via high-ohmic resistors allowing the operation with single supply voltage. The corresponding gate and drain supply voltages of all FETs are approximately $V_{dd}/2$. This bias corresponds to class-A operation, where the RF buffer and the switching FETs have good gain properties. Furthermore, the FET can be symmetrically switched by a sinusoidal LO voltage. With an average g_m of 80 mS and a load resistance Z_L of 50 Ω, we can estimate an upper limit of the conversion gain of around 6 dB. With a loss of the IF filter of approximately 2.5 dB and losses due to the nonideal RF input matching in the range of 2 dB, we can predict an upper conversion gain of 1.5 dB. Due to the nonideal characteristics of the FETs at these high frequencies, in practice, the achievable conversion gain will be lower. The nonideal characteristics are mainly caused by the non-zero on-resistance and the non-infinitely off-resistance of the switch FETs, and the non-zero channel conductance of the RF buffer FET.

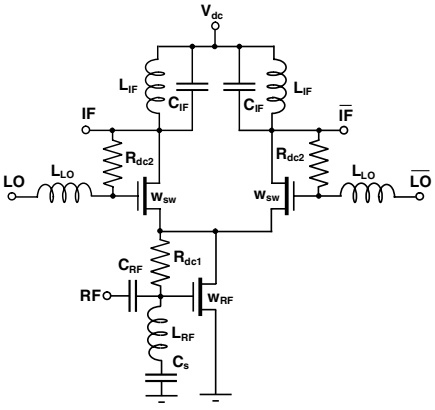


Fig. 10.27. Simplified schematic, w_{RF}= 128 µm, w_{sw}=64 µm, C_{RF}=100 fF, L_{RF}= 140 fH, C_s=2 pF, R_{dc1}=R_{dc2}=4 kΩ, L_{LO}= 400 fH, L_{IF}=1.2 nH, C_{IF}=4 pF, compare [Ell10] © IEE 2004

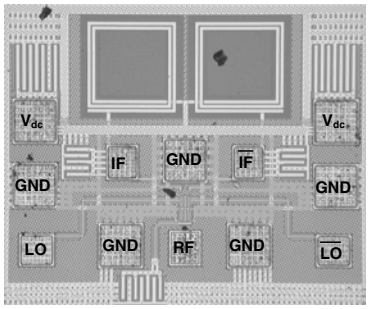


Fig. 10.28. Photograph of mixer with chip size of 0.5 × 0.4 mm^2, compare [Ell10] © IEE 2004

To simplify measurements, the circuit has been designed for 50-Ω terminations. Much higher load impedances could be applied in systems. This would yield significantly higher gain as indicated in Eq. (10.26). The circuit is operated with RF, IF and LO frequencies of 30 GHz, 2.5 GHz and 27.5 GHz, respectively, and biased with a supply voltage of 1.2 V, a corresponding supply current of 17 mA and an LO power of 5 dBm. The return losses are depicted in Fig. 10.29. The lowest loss and SSB NF of 2.5 dB and 13 dB are measured at 29 GHz and 28 GHz, respectively. Within a broad frequency range from 26 to 34 GHz, the loss and noise

figure increase is less than 3 dB. The loss and SSB NF vs LO power are illustrated in Fig. 10.30. The lowest loss is measured at an LO power of 2.5 dBm. Up to 10 dBm LO power, the SSB NF decreases with LO power. As shown in Fig. 10.31, up to 10 dBm LO power, the IIP3 increases with LO power. At 5 dB LO power and 1.2 V supply voltage, the IIP3 is 0.5 dBm. The port isolations are listed in Table 10.5.

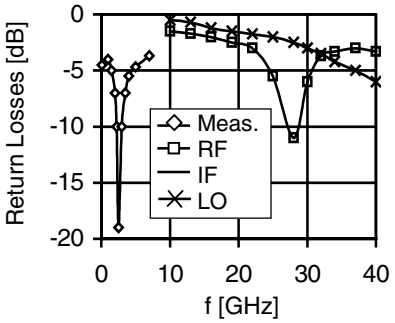


Fig. 10.29. Small signal return losses at V_{dc}=1.2 V and I_{dc}=17 mA, compare [Ell10] © IEE 2004

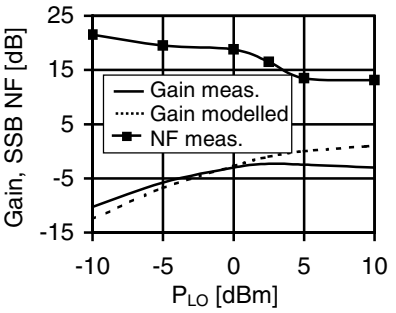


Fig. 10.30. Conversion loss and measured SSB noise figure vs RF frequency with fixed IF frequency of 2.5 GHz at 5 dBm LO power, V_{dc}=1.2 V and I_{dc}=17 mA, compare [Ell10] © IEE 2004

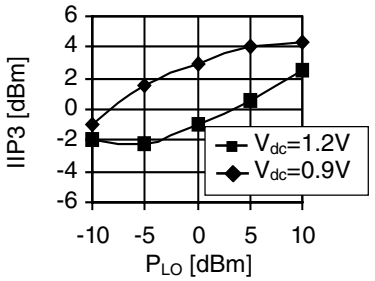


Fig. 10.31. Measured third order intercept point at input vs LO power, V_{dc}=1.2 V, I_{dc}=17 mA, f_{RF}=30 GHz, f_{IF}=2.5 GHz, compare [Ell10] © IEE 2004

Table 10.5. Port isolation

Isolation	LO to IF	LO to RF	RF to IF	IF to RF
Meas.	8 dB	12 dB	20 dB	30 dB
Sim.	17 dB	18 dB	19.5 dB	37 dB

LO power: 2.5 dBm

10.3.4 Comparison of Mixer Approaches

In Table 10.6 we find a qualitative comparison of the mixer approaches treated in the preceding sections. It is clear that passive mixers are not capable of providing gain. To compensate for the losses, the saved DC power can be used for an amplifier located in front of the mixer yielding a low system noise figure. Especially on silicon-based technologies having poor substrate isolation, the differential topologies are superior due to their high immunity against noise and pick-up of unwanted signals via the substrate, and the high gain.

Table 10.6. Qualitative comparison of mixer approaches

	Drain-pumped transconductance	**Gate-pumped transconductance**	**Gate-pumped resistive**	**Differential gate-pumped resistive**	**Differential pair**	**Gilbert-cell**
Conversion gain	Moderate	High	Low	Low	Very high	Very high
Linearity	Moderate	Low	High/very high	Very high	Moderate	Moderate/high
Noise	Low	Very low	Moderate	Moderate	High	High/very high
LO to IF suppression	Moderate (down-mixer) Low (up-mixer)	Low (down-mixer) Moderate (up-mixer)	Low	Low	Moderate	Very high
Power consumption	Low/zero	Moderate/low	Zero	Zero	High	Very high
Chip area	Moderate/large (inductors)	Moderate/large (inductors)	Moderate/large (inductors)	Moderate/large (inductors)	Small (RC load) Moderate/large (LC load)	Small/moderate (RC load) Large (LC load)
System integration	May be limited since single-ended	May be limited since single-ended	May be limited since single-ended	Good/very good	Good (LO, IF differential)	Very good

10.3.5 Mixer Performances

The key performances of several state-of-the-art down-mixer topologies are listed in Table 10.7.

Table 10.7. Mixer performances

	Principle	f_{RF}/f_{IF} [GHz]	G_c [dB]	SSB NF [dB]	IIP3 [mW]	P_{LO} [mW]	P_{dc} [V×mA]	Ref.
Active Mixers								
200-nm InP HEMT	Gate pumped g_m	95/ 1	0.9	n.a.	n.a.	1.6	n.a.	[Kwo93]
100-nm InP HEMT		64.5/ 16	1	n.a.	n.a.	0.7	n.a.	[Orz03]
0.5-µm SiGe HBT	Gilbert cell	24/ 0.1	≈10[a]	n.a.	n.a.	≈1	15 × 3.6	[Sön03]
180-nm CMOS	Cascode	10/ 0.2	16	n.a.	n.a.	n.a.	n.a.	[Mad01]
180-nm CMOS	Diff. pair	24/ 4.9	13[b]	17.5	n.a.	n.a.	1.5 × 27	[Gua04]
90-nm SOI CMOS	Diff. pair	30/ 2.5	–2.5	13	1	3	1.2 × 17	Section 10.3.3.1 [Ell10]
Passive Mixers								
0.5-µm GaAs MESFET	Gate pumped resistive	1.9/ 0.11	–7	8	6.3	3.2	0	[Kuc99]
0.5-µm GaAs MESFET		5.2/ 0.95	–5.5	6.5	200	10		[Ell24]
130-nm GaAs HEMT		25.7/ 0.2	–7.2	n.a.	n.a.	10		[Ver00]
90-nm SOI CMOS		27/ 2.5	–9.7	11	100	10		Section 10.3.2.1 [Ell8]
140-nm InP PHEMT		60/ n.a.	–7.7	n.a.	n.a.	3.2		[Zir01]
130-nm GaAs HEMT		77/ 0.03	–10	n.a.	n.a.	1		[Sch98]
Schottky diode	8th harmonic	38/ 1.2	–23	n.a	n.a.	100		[Zha01]
90-nm SOI CMOS	Drain pumped g_m	35/ 2.5	–4.6	7.9	1.5	5		Section 10.3.1.1 [Ell4]

[a]Inclusive buffer [b]High-ohmic input

10.4 Tutorials

1. Why do we need mixers? Do we need frequency conversion for UWB systems?
2. What are the major design constraints for mixers? Compare the requirements for down- and up-mixers.
3. Under which conditions is the noise of mixers important?
4. What is the difference of harmonics and intermodulation products?
5. How can we mathematically describe the nonlinear characteristics (e.g. current) of a device?
6. Show analytically that the mixing product of two frequencies can give permutations of frequencies. What is the important requirement?
7. What about the amplitudes of higher harmonics? Why do they decrease with increasing order?
8. Draw the equivalent circuit of a FET. What are the most non-linear elements? Why?
9. Explain the functional principle of gate and drain pumped transconductance mixers. How can we maximise the conversion gain? What are the limitations in terms of maximum operation frequency? Which one would be better suited in terms of LO to IF/RF isolation for a down- and up-mixer?
10. What are the pros and cons concerning active transconductances and passive resistances?
11. Explain the functional principle of a differential pair and Gilbert cell mixer. How can we optimise the conversion gain? Review the tradeoffs for the loads with respect to gain, highest operation frequency, bandwidth, power consumption, stability and circuit size.
12. Which device has stronger g_m nonlinearities – the BJT or the FET? Which one should provide higher conversion gain at low and high frequencies?
13. Could we design frequency multipliers and dividers with mixers, e.g. using a differential pair?
14. Review the typical performances of state-of-the-art mixers.

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