5

Electronic Dust and e-Grains

H. Reichl and M. J. Wolf

"Small is beautiful"

5.1 Introduction

With microelectronics as the technology and Ambient Intelligence as the application driver, the changes to all areas of our professional and private lives will be increasingly far-reaching. Today, visions of the future are all founded on a common theme: seamless communication based on the Internet and mobile multifunctional terminal devices. As is apparent with mobile phones, the trend is moving towards smaller, more complex, autonomous systems. These systems are emerging as universal information and communication terminals, characterized by extreme miniaturization and the implementation of a wide range of services. This trend will inevitably be carried forward into the future. In the process, present-day system integration requires the production of ever-more complex systems, comprising an increasing number of active and passive components while reducing production costs.

In order to reduce the size of a system, it is necessary to develop new integration technologies, which also use the third dimension for system integration, and, secondly, to develop an alternative to replace the conventional method of system integration through rigid connections. This represents the framework for a new concept of system integration, based on so-called "electronic grains" or "e-Grains" or "Smart Dust." e-Grains are highly miniaturized sensor nodes. They are tiny, autonomous, functional units, and are distinctive, not only through their ability to communicate with each other, but also because they are freely programmable and to a certain degree modular. At the same time, these units are universal and partly specialized, for example, through the integration of selective sensors.

In terms of hardware, technology, and software design, system integration based on the innovative e-Grain concept represents an entirely new challenge and requires a synergy of individual technologies at an exceptionally early stage. And naturally, through the differing nature of the approaches used to find a system solution, it also holds a particular techno-scientific appeal, while simultaneously yielding extremely high innovative potential.

This technology poses particular challenges with regard to the desirable sizes (a few cubic millimeters), the need to achieve continuous operation through an integrated or external wireless power supply, and the necessity of allowing multiple e-Grains to communicate. The system is characterized by a large number of individual interconnected e-Grains. The e-Grain vision therefore represents a new approach to system integration that will help to develop complex, flexible, and cost-efficient integrated systems with black-start capability, based on ultra-small sub-components. Due to the high density required for integration, the realization of e-Grains necessarily involves stacking thin functional films, which are then bonded together. To do this, a new 3D bonding technique based on polymer films is under consideration. The development of highly integrated 3D wiring calls for a vertical-integration technology that allows interconnections to be fabricated and precisely aligned on ultra-thin substrates below 50 µm. The production of ultra-thin functional films as well as their integration to form a complete wafer-level (WL) system is therefore a key technology. In addition to reducing the size, the miniaturization of passive components is also fundamentally important for the complete system.

The e-Grain system requires that the tiny electronic units be capable of autonomously meeting their own energy requirements over a certain period of time or during their entire operating life. This necessitates energy storage devices with high power density compatible with the system in terms of dimensions and production technology.

Another important issue of the e-Grain system is wireless linking of individual e-Grain cells. Microwave front end technology will therefore assume a key position as a connecting link between data-processing electronics and the transmission channel. In view of the low range of 1–10 m and the already oversubscribed utilization of frequencies in the range below 10 GHz, which restricts the flexibility required by the e-Grain system, transmission will lie in the millimeter wavelength range (10–60 GHz).

Communication between a large number of tiny, highly integrated e-Grains presents a particular challenge in the design and implementation of this communication system. One of the important parameters for communication between a number of e-Grains is the available energy capacity which is greatly limited by the small volume.

Special attention is also given to the way in which two individual e-Grains communicate, address assignment within a self-organized network, a flexible semantics-based grouping of messages within an e-Grain network as well as interfaces to applications and management. The creation of a self-organized ad-hoc network that can comprise a large arbitrary number of e-Grains requires a suitable operating-system environment that provides the necessary administration service. In its entirety, this form of ad-hoc network can be seen as the configurable system, whereby the networked components representing the configurable resources. The actual operating system provides the necessary administration services to monitor and control this type of system. This also includes the programming of individual e-Grains.

In addition, the operating system offers a µ-network interface through which the applications themselves can access the network components. For linking the e-Grain µ-network to other networks (LAN, Internet), the operating system provides gateways with the corresponding address and protocol conversion functions.

5.2 Basic Construction of Self-Sufficient Wireless Sensor Nodes – e-Grains

Figure 5.1 shows the principle architecture of a wireless sensor node such as an e-Grain. It is divided into an analog part (sensors, amplifiers, and AD-converter) in digital signal processing, a wireless interface, and a power supply. The functions of the different elements are described in Fig. 5.1.

- The *sensors* are the basic components of the e-Grains. Depending on the sensor requirements the preferred technology for realization is MEMS, with a mandatory prerequisite of ultra-low power.
- The *low power analog interface* is in charge of interfacing the analog physical world seen by the sensors to the digital world of the microcontroller. The main constraint on this function is the minimization of the internal components to reduce the power consumption, while being compatible with noise levels adapted to the resolution of the sensors, the necessary bandwidth, and the dynamic range.
- The *microcontroller* is in charge of interfacing with almost all the functions of the e-Grains, particularly for sequencing all the operations, while controlling the power dissipation to reduce it to the lowest possible level. In some applications its functionality is extended to data compression

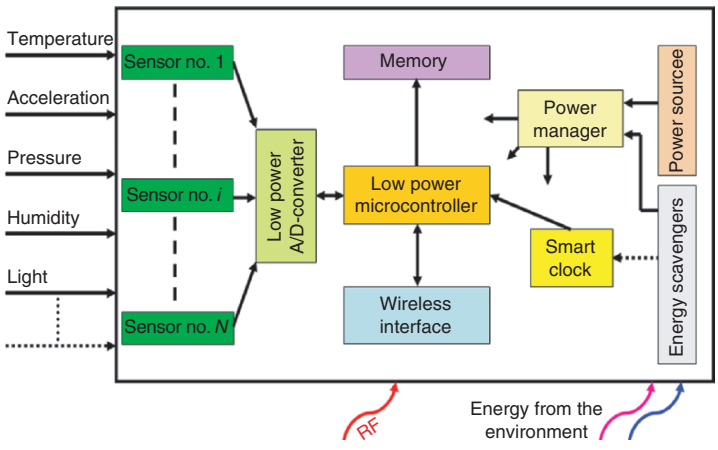

Fig. 5.1. Principle architecture of self-sufficient wireless sensor nodes, e.g., e-Grains

operations, self-organizing procedure with other e-Grains for data transmissions and relay, calibration operations, or other specific operations (such as localizing other e-Grains).
- The *wireless interface* is in charge of allowing the best possible link budget for communication, using different techniques, from specific antenna schemes to dynamic impedance matching. This interface is bi-directional: uploading programs and getting data back from the sensors. The main challenge here is the optimal compromise among the highest transmission efficiency, the lowest power dissipation, and the reduced dimensions acceptable in a given domain.
- The *events storage memory* is a generic memory with specific properties of very low power consumption for a given memory space, data/state remanence, possibly dynamic programmability, and dynamic sharing between data and programs. In the simplest case, it can be a standard flash memory.
- The *smart clock* is a specific function useful for different cases. It can be used as an "awakener" of the microcontroller in the case of ultra-low power specific applications such as transient event monitoring where, most of the time, there is nothing (no event) to be detected, but from time to time specific short time events occur, for which a high resolution is necessary to track the data to be monitored. Alternatively, it can be used as a self rate-switchable clock (for power saving objectives) or a smart clock for localization purposes.
- The *micropower source* is the basic local energy source of any e-Grain. In the simplest case, it can be a micro-battery or a supercapacitor. In more elaborate versions, it can also be a micro-fuel cell. Its main characteristic is that its lifetime is necessarily limited in time, contrary to the energy scavenger described below:
- The *energy scavenger* is a function designed to get energy from the environment: either from the real natural physical flows of energy (optical flux, EM, thermal flux, etc.) or from artificial sources, such as in the situation of remote powering, where a source of power is directed towards the e-Grains from an external location.
- The *power management* can be realized by a smart circuit able to handle the power management issues linked to the multiplicity of energy sources. This will be achieved by analyzing the available energy densities at different points of time, deciding on the procedure for maximizing the collected energy, switching in time between the different energy sources, while storing this energy, e.g., in micro-batteries.

The future e-Grain is a 3D arrangement of functional sub-modules (layers), each of which is a heterogeneous functional layer with embedded components as illustrated in Fig. 5.2.

The minimal physical size of an e-Grain is determined by three main factors: the size of the constituent integrated circuits, the power storage and

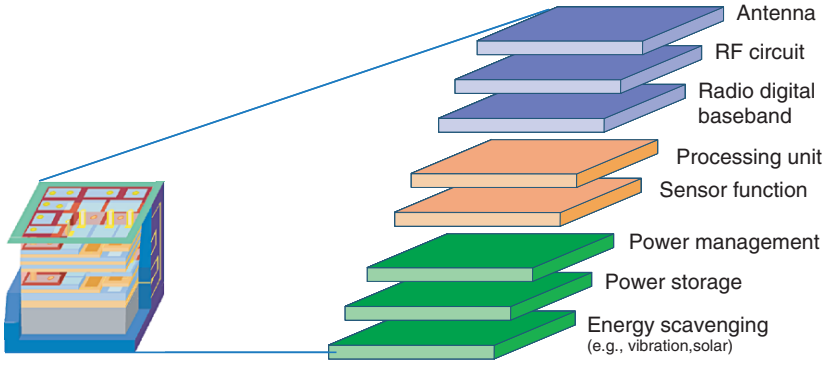

Fig. 5.2. Schematic of an e-Grain structure based on heterogeneous functional layers

harvesting subsystem, and the size of the antenna required for power-efficient communication. The scaling roadmap (ITRS) of integrated circuit technologies enables the realization of complex circuits in rather small sizes. The main size limitations for e-Grains are therefore the power system and the antenna size (e-Grain, online).

5.3 System Design

After consideration of the functional units, it is required to specify the architecture by designing the circuitry and looking for bottlenecks of the complete system. Behavior models of the whole system regarding costs, energy, and size help to choose materials, components, and technological processes (Niedermayer et al. 2004). The selection of materials and technologies is also influenced by environmental conditions. Ambient parameters such as force magnitudes, temperature maxima, and humidity result in a very different focus of the system design. Additional design restrictions follow from the process flow. Thus, the position of several components is not arbitrarily due to effects such as field coupling and shielding, if the functional layers are folded or stacked afterwards. According to the design rules, the layout is generated by defining the component positions and routing their interconnections; see Fig. 5.3.

The interdependencies between different functional units have to be considered in the case of higher component densities. For instance, the transmission frequency has to be defined for designing the communication hardware. A sole consideration of the communication circuitry would only include parameters such as antenna efficiency, antenna directivity, RF-losses, polarization, and mismatch. Resulting in a changed structure of transmission data or a modification of the data rate, other modules influence the hardware optimization of the communication unit. For instance, technological improvements of an applied sensor could allow an accelerated data acquisition. In this case a faster

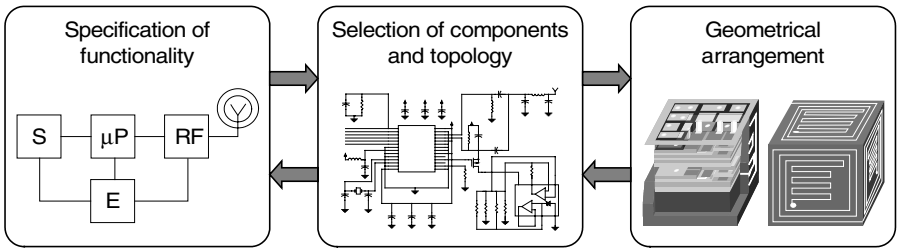

Fig. 5.3. Abstraction levels of system design

architecture with shorter duty cycles would be recommended. Thus, the optimal transmission frequency regarding power consumption will move to higher values. The suitable solution for the whole system, however, also has to reflect environmental conditions such as absorptions, reflections, noise, and RF coverage.

Depending on the reliability requirements, monitoring of some internal and external conditions guarantees safer functioning in security sensitive cases. Therefore, appropriate algorithms calculate the probability of a malfunction. As a result, an observation and evaluation of operating voltage gradients, temperature variations, and vibrations can significantly improve failure predictions. A very compact layout with dense interconnections results from the system design. The debugging of highly integrated prototypes can become very challenging and requires system verification at different levels of the design process.

An integrated treatment of physical couplings is especially important for small systems with tightly positioned components. Apart from the realization of prototypes and their characterization by measurements, the whole system or adequate subsystems have to be verified in a computerized model (Mentor Graphics 2001). Distributed microsystems are often heterogeneous systems and possess both spatially distributed and concentrated elements. Properties resulting from different physical domains have to be simulated to describe the behavior of the whole system. As a consequence, the modeling and simulation of these devices is more complex. Due to the limited computation time for simulations, details which are of less significance for the system behavior often have to be neglected during model generation.

Besides the verification of the analog, digital, and mixed-signal circuitry, the parasitics have to be considered for the components, package elements, and interconnections. This includes a quantification of reflections, cross talk, and radiation. Furthermore parasitic charging of insulation layers can substantially influence the system behavior.

Small distances between several components are often critical regarding heat spreading, conductance, convection, and radiation. Thus, the heating of a microprocessor can cause a thermal drift in an adjacent sensor. These thermal effects can be reduced by solutions such as thermal vias, an efficient

energy management, or a sensor data processing with drift awareness. To achieve the latter, macromodels of the sensors are helpful, which describe the coupled thermo-mechanical and electrical behavior. Often, for the electrical behavior white (or glass) box models are used, which are transparent and represent the "physics," while for the thermal behavior black box models are preferred, which describe the I/O behavior "merely" mathematically.

Diverse computations from other domains such as acoustics or fluidics may also be required depending on the application. Mechanical simulations addressing shock and stress are often relevant for reliability estimates of packaging elements like solder bumps. Some verification examinations can result in coupled simulations of different domains. This is required, for instance, for a characterization of forces generated by electrostatic actuators.

Highly integrated systems certainly need to be tested by measurement but this meets with two main problems. The first arises from the high degree of complexity, the second one stems from the extreme miniaturization, which makes interfacing to standard measurement equipment difficult. For example, even the capacitance of an RF probe may cause erroneous results.

It would thus be desirable to perform the verification of the complete system by virtual prototyping, in which the entire design is represented in computer memory and verified in the virtual world before being implemented in hardware. Software testing is not, however, immune to problems arising from complexity either, as has already been pointed out.

The more precisely the effects can be characterized, the more correctly the counter measures can be dimensioned without high design overheads. Therefore, efficient system verification allows increased component densities and smaller energy supplies due to optimized power consumption. Those energy savings can be achieved by means such as reducing timing slack or lowering voltage levels. Additionally, the increased effort for system verification can result in cheaper products by permitting higher component tolerances.

The errors, detected during the verification process, can necessitate different efforts. At best, only small changes have to be made in the layout. More serious errors require a replacement or addition of components. In the worst case, the design must be restarted at the concept level, demanding a completely different architecture. Therefore, prototyping can require several iterations to discover and fix problems. Furthermore, a problem solution can introduce new errors. If the verified prototypes meet the application needs, it is often necessary to additionally adapt to the requirements of high volume manufacturing.

5.4 System Integration Technologies

Several companies and research institutes all over the world are currently working on the development of 3D system integration. Besides the approaches which are based on silicon technologies (SoC) like fabrication of multiple

device layers using recrystallization or epitaxial growth, the large spectrum of technological concepts can be classified in the following categories: stacking of organic substrates, integration of flexible functional layers, embedded components in organic substrates, and WL integration by stacking of chips or wafers.

5.4.1 Stacking of Organic Substrates

Based on organic substrates (e.g., FR4) and existing assembly and interconnection technologies (e.g., chip on board), COB Fraunhofer IZM has developed a 3D stacked configuration (Grosser 2004; Wolf et al. 2005). Single components (SMDs, quartz), integrated circuits as bare die, and micropackages available on the market were used for this approach.

The basic construction for the sensor module is shown in Fig. 5.4. All required functions and components are integrated in the package within a size of 1 cm^3.

The advantage of this modular concept is that each sub-module can be tested separately. By exchanging sub-modules different applications can be reached, new components can be implemented, and the production yield can be increased as well. The configuration of the individual sub-modules is shown in Fig. 5.5.

Figure 5.6 illustrates a 3D visualization of the printed circuit board (PCB) sensor node (1 cm^3). An FR4 frame acts as a vertical interconnection between the individual sub-modules, e.g., sensors and microprocessors.

Figure 5.7 shows the single sub-modules (microcontroller, RF unit, sensor unit, clock). Solder joints interconnect the sub-modules via a frame. A cross section of the sensor node and the vertical solder interconnects is shown in Fig. 5.8.

Figure 5.9 shows a sensor node (PCB technology), which is able to measure the temperature of the environment. A number of these systems can be

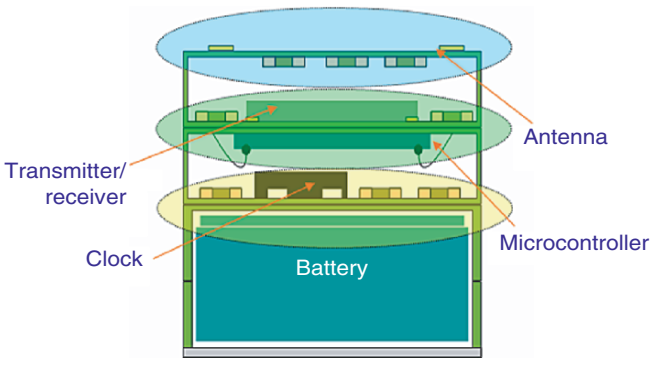

Fig. 5.4. Layered structure of a wireless sensor node in stacked PCB technology

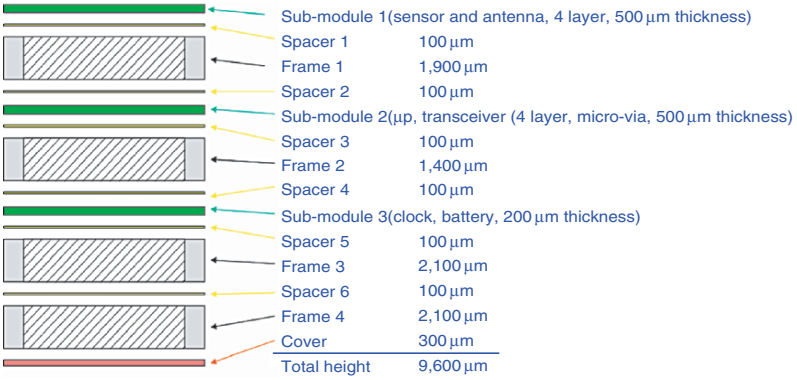

Fig. 5.5. Sub-module specification and arrangement for the PCB-sensor node (Kallmayer et al. 2005)

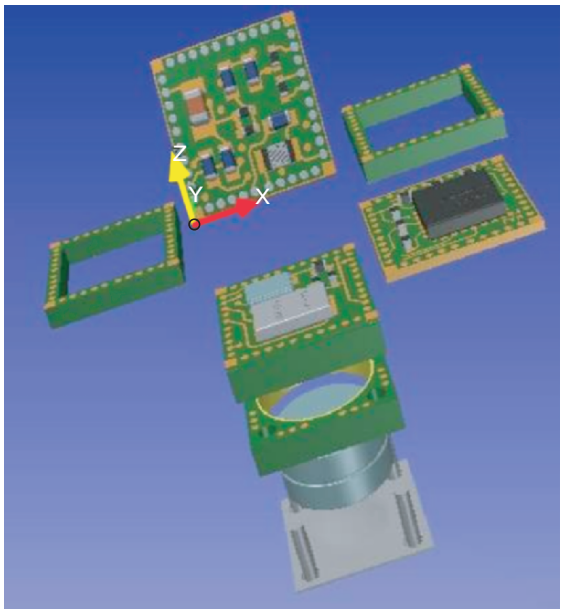

Fig. 5.6. 3D visualization of the functional sub-modules of the sensor module

combined and wireless linked for specific applications (e.g., logistic,environment, process control, etc.). The technical parameters of the PCB-sensor node are:

- Operating range: $> 1\,\mathrm{m}$
- Operating frequency: $2.4\,\mathrm{GHz}$
- Repetition rate: $1/\mathrm{s}$
- Power supply: two batteries ($2 \times 1.5\,\mathrm{V}$)
- Operating time: $> 500\,\mathrm{h}$

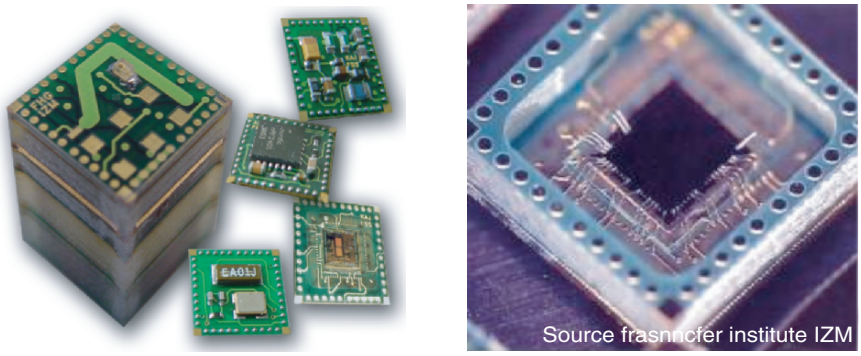

Fig. 5.7. Assembled functional sub-modules and details of microprocessor unit

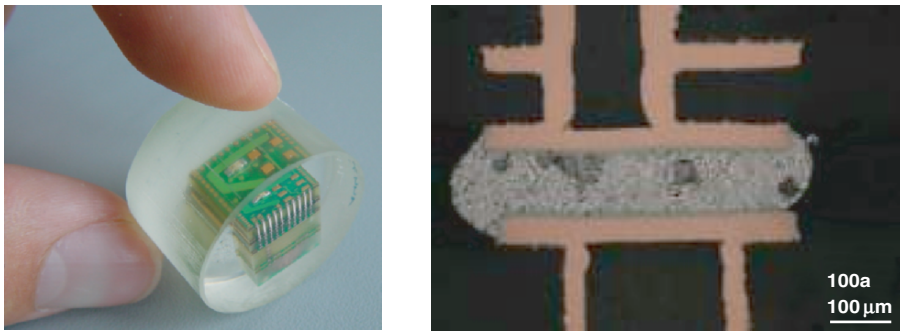

Fig. 5.8. Solder interconnection between the individual functional unit and the frame for 3D assembly

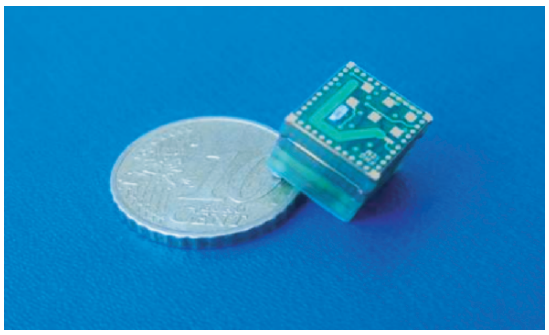

Fig. 5.9. Wireless temperature sensor node in stacked printed circuit board technology (size: 1 cm^3)

5.4.2 Integration of Flexible Functional Layers

The integration of chip components on flexible substrates offers the possibility to create high dense sensor nodes by folding of the flexible substrate. Figure 5.10 shows a schematic of a folded sensor node. An essential advantage of this technology is that the sensor node can be tested before folding. To reduce the system height and the footprint of the node flip-chip interconnects are preferred.

As long as ICs with standard thicknesses between 250 and 600 µm are used, conventional flip-chip technologies with contact heights of approximately 50–100 µm may be applied, forming reliable interconnects on various organic or inorganic, rigid, or flexible substrates.

A reduction of the contact height towards ultra-thin flip-chip interconnects gains in importance in connection with thin chips and substrates. Figure 5.11 shows the disproportion between the thicknesses of the structural elements of an assembly consisting of a thin IC (50 µm), bonded on a thin substrate (50 µm) with conventional flip-chip technology. In consequence, the reduction of the contact heights as well as the thicknesses of chip and substrate to 10 µm holds an impressive potential for a further reduction of the total module thicknesses to approximately 100 or 30 µm, respectively. This makes ultra-thin flip-chip interconnects a substantial contribution to meeting the requirements of future highly integrated and miniaturized modules that may consist of several, stacked or folded, ultra-thin active and passive layers.

By using solder technology the thicknesses of the UBM, the solder bumps and the substrate metallization can be reduced. The standard electroless nickel UBM for high reliability has a thickness between 5 and 10 µm but only a minimum thickness of 1 µm is necessary to have a closed and void free nickel layer (Nieland et al. 2000). Technologically, it is possible to reduce the Ni layer to almost the thickness of the last chip passivation layer.

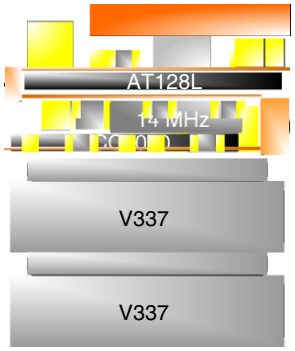

Fig. 5.10. Schematic of a sensor node with a folded flexible substrate, antenna, and battery (Kallmayer et al. 2005)

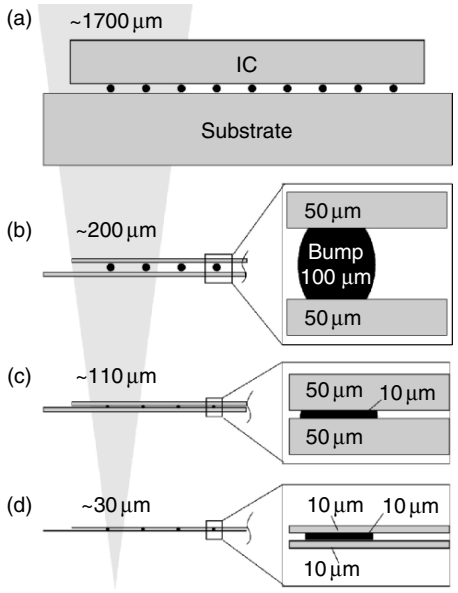

Fig. 5.11. Miniaturization potential of ultra-thin flip-chip interconnects (Kallmayer et al. 2005)

For the application of very small solder volumes and bumping of ICs with pitches $< 150\,\mu$m conventional printing methods are not suited. Electroplating is one choice, but the just lately developed "immersion solder bumping" (ISB) is a step ahead under low-cost aspects. This maskless process uses the wettability of the UBM by a liquid solder alloy through which the entire wafer is moved. The solder cap height is typically in the range of a few micrometers; see Fig. 5.12.

Regarding adhesive bonding technologies, NCA and ACA will be within closer consideration, as they are the most promising technologies. UBM and substrate metallization can be reduced even more than in the case of soldering as adhesive bonding does not lead to dissolution of the metal layers. For both, NCA and ACA, leaving out bumps completely is an option for further reduction of contact height. Some ACA applications today are making use of nickel bumps. In this case the contact height is determined by the nickel bump, the substrate metallization, and the size of the trapped particles, commonly ranging from 3 to 15 µm. With these possible ACA and NCA contact configurations, investigation of the ageing behavior for both technologies gains much importance.

An impressive step for further miniaturization of any 3D-chip- or multichip-assembly can be taken by the use of thin chips. Today, wafers can be thinned from 600 µm standard thickness to approximately 10 µm. In these thickness ranges silicon shows great mechanical flexibility comparable with that of polymeric foils.

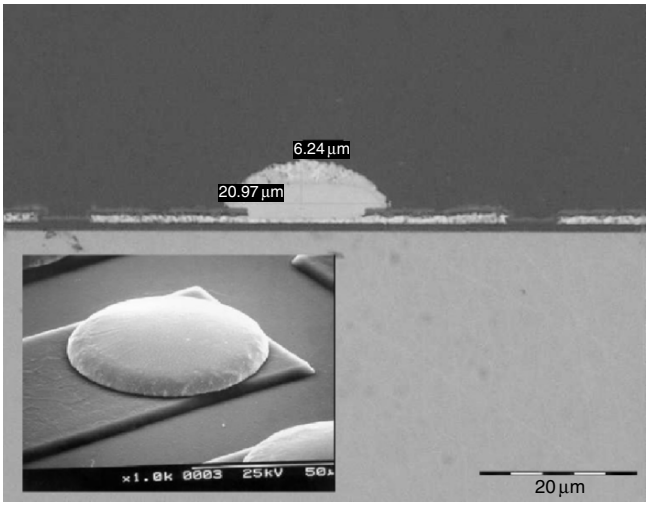

Fig. 5.12. SEM picture of a cross section of an immersion solder bump

Figure 5.13 shows SEM pictures of cross sections of thin soldered and ultra-thin ACA bonded flip-chip test assemblies (Pahl et al. 2002). The realization of extremely space saving system–level integration requires technologies allowing 3D packaging while taking into account the space required for passive components. The minimization of the area needed for passive components such as coils, resistors, capacitors, and filters is an important factor for volume reduction of such wireless sensor systems as well.

The application of thin flexible circuit interposers stacked by solder bump connections is a possibility to combine high density routing with passive device integration and to realize a 3D approach by bending, folding, or stacking (Wolf et al. 2005).

The thin flexible circuit interposer units are based on a temporary release layer, a polyimide dielectric with a built-up high density thin film copper wiring as well as passive element integration at wafer level; see Fig. 5.14. After removing the units from the carrier wafer by applying a temporary release layer a stacking process can be realized by using standard assembly equipments like a flip-chip bonder; see Fig. 5.15.

Besides conductor lines and passive elements such as resistors, capacitors, coils and filters, active chips thinned down to 20 µm can also be integrated into the polymer layers.

The advantages of WL processing of polyimide-based flexible interposers can be formulated as follows:

- Realization of ultra-thin ($\approx$ 50 µm) high density stackable flexible substrates with via chains.
- Application of the conventional thin film technology, e.g., spin-on of photo-definable dielectrics (polymer) and photoresist, sputtering of metal seed

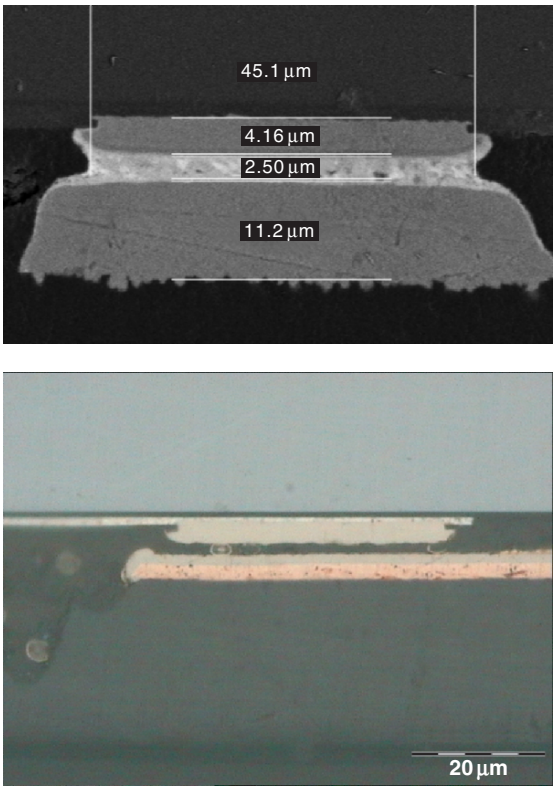

Fig. 5.13. SEM pictures of thin soldered contact (upper) and ultra-thin ACA contact, ∼ 3 µm Ni, ∼ 3 µm deformed particle, ∼ 3 µm Cu/Au (lower)

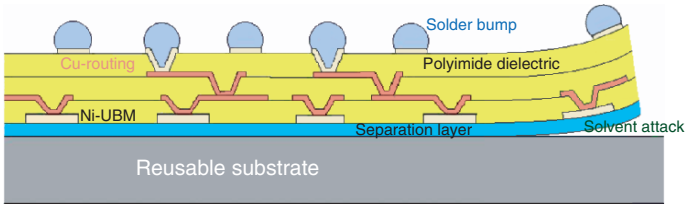

Fig. 5.14. Principle of thin film flexible interposer

layers and resistor layers, electroplating of routing metal (e.g., Cu, Ni, Au) and solder alloy (e.g., AuSn, SnAg, CuSn).
– Small dimensions of conductor lines and vias (high density).
– Arbitrary shape, foldable, stackable for 3D integration.
– Integration of passive elements (R, C, L) and active devices (ICs).
– Metal routing completely encapsulated.
– Excellent chemical and high temperature stability.

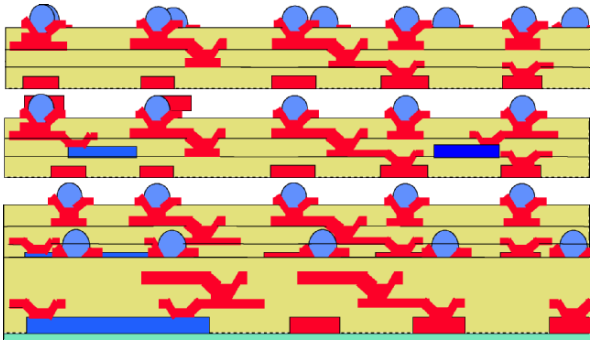

Fig. 5.15. Stacking of flexible interposer with embedded devices

The realization of integrated passive elements into the flexible interposer can be achieved by adapting the thin film process.

Resistors

Most resistor requirements can be met with thin films having a sheet resistance R_s of 100 ohms sq^{-1}, which can be achieved by an approximately 20 nm thin NiCr layer. Low resistor values can be realized by straight lines, while higher values have to be laid out as meanders.

Inductors

The only way to realize inductors in a thin film build-up of only two routing layers is the planar coil approach. A good magnetic field coupling is reached by a conductor, which is arranged into a spiral form in one metal layer. A second metal layer is necessary to route the inner coil contact to the outside of the coil. This layer can also be used for additional windings so that a larger inductance value can be realized within the same area. The characteristic values, e.g., inductance, quality factor, resonance frequency, are influenced by the material and design parameters like number of turns, diameter of coil window, line pitch/space, etc.

Capacitors

In a thin film build-up with two routing layers integrated capacitors can be realized by simple parallel plate structures. For the parallel plate type the interlayer polymer serves as the dielectric material. The characteristic values like capacitance, quality factor as well as their resonant frequency depend on the electrode area A, the interlayer polymer thickness as well as the electrode form and the dielectric constant ε_r which is around 3.3 for polyamide.

Filters

Based on the single components (R, L, C) more complex passive structures like matching or resistor networks, oscillators or filters can be implemented (Zoschke et al. 2005). The necessary interconnections between the elements can be realized as high density conductor lines as well as transmission lines for high frequency application. As one example Fig. 5.16 shows an LC low pass filter using Cu and polyimide ($\varepsilon_r = 3.3$). The filter was designed in Tschebyscheff style of third order to have cut off frequencies of 2.45 and 5 GHz. Microstrip transmission lines were used for elements interconnection. The coils have an inductance of 5.8 nH, the capacitor has a capacitance of 1 pF.

Figure 5.17 shows the measured attenuation behavior of this filter structure up to a frequency of 8 GHz. At 2.45 GHz a clear bend in insertion loss can be observed. The structure has a total size of 3.3 mm × 1.95 mm (Zoschke et al. 2004).

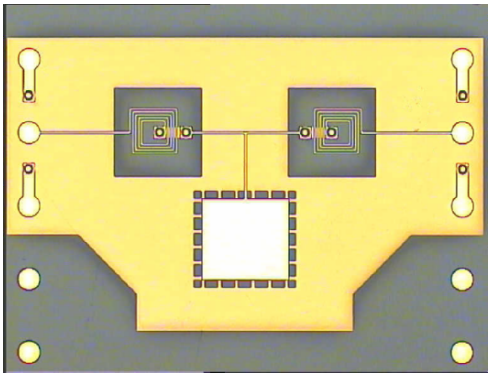

Fig. 5.16. Attenuation of thin film low pass filter

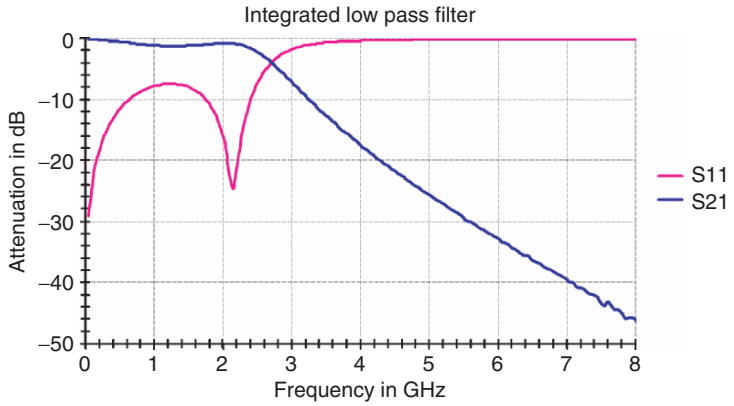

Fig. 5.17. Integrated low pass filter with two inductors and one capacitor

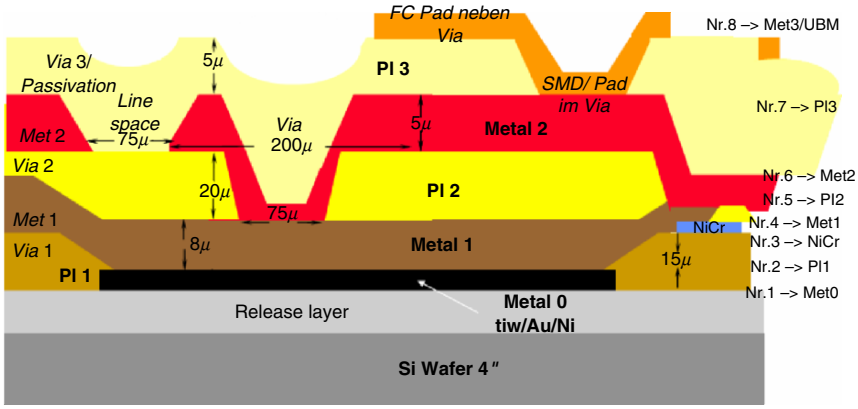

Fig. 5.18. Schematic cross section of the flex interposer

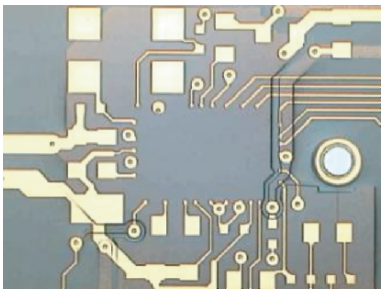

Fig. 5.19. Detail of RF circuit pads

Based on the release process for a functional layer a thin film interposer for a wireless sensor node was realized at Fraunhofer IZM. A schematic cross section is shown in Fig. 5.18.

Figure 5.19 shows a detail of the IO pads of the receiver component, which will later be flip-chip assembled.

The interposer consists of four metal layers (Cu) and three polymer layers (PI) with an overall thickness of 35 µm and a size of 9.8 mm × 31.2 mm; see Fig. 5.20 (Wolf et al. 2005).

The substrate with the assembled components as shown in Fig. 5.20 will be folded, and connected to the antenna and batteries. The overall size of the module including antenna is around 1 cm^3 from which the electronic components take up approximately 20% of the volume.

Modified configurations such as stacked devices instead of folding the flex interposer are implemented. Figures 5.21 and 5.22 show examples of assembled stacks of flex substrates. The stacks were aligned and soldered using a flip-chip bonding tool. The stack units were designed for the assembly of thin flip-chips on top of them.

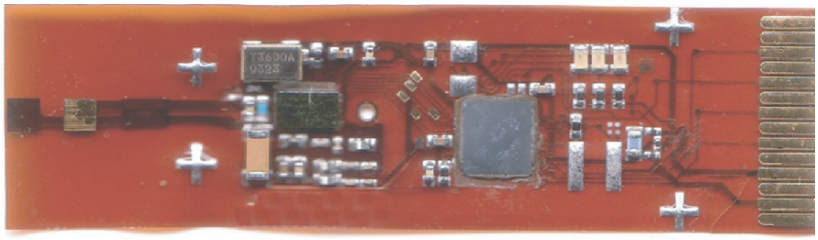

Fig. 5.20. Flex polymer interposer assembled with all electronic components for a wireless sensor node (868 MHz) (Fraunhofer IZM) (Wolf et al. 2005)

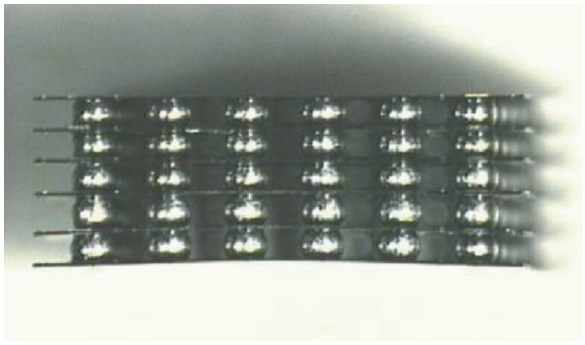

Fig. 5.21. Stack of six flexible substrates with solder ball interconnects, total thickness approximately 1.3 mm

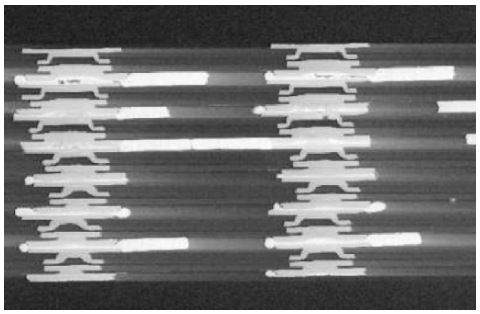

Fig. 5.22. Stack of eight flexible substrates with thin solder interconnects, total thickness approximately 0.53 mm

5.5 Embedded Components in Organic Substrates

A number of approaches concerning the integration of components have lately been presented. One of the first was the integration of power devices, shown by General Electric (Filion et al. 1994). The Technical University of Berlin later presented an embedding of chips into ceramic substrates for a signal processing application. Recently Intel introduced its bumpless build-up layer (BBUL) as packaging technology for their future microprocessors (Waris et al. 2001). At Helsinki University of Technology the so-called integrated module board (IMB) technology has been developed, which embeds chips into holes in an organic substrate core (Braunisch et al. 2002; Tuominen and Palm 2002).

At Fraunhofer IZM and the Technical University of Berlin the chip in polymer (CIP) technology is under development (Ostmann et al. 2002a, b). Its main feature is the embedding of very thin chips (50 µm thickness or less) into built-up layers of PCBs, without sacrificing any space in the core substrate. The embedded chips can be combined with integrated passive components; see Fig. 5.23.

A substantial advantage of the CIP approach is the embedding of components, using mainly processes and equipment from advanced PCB manufacturing. The realization of the process is illustrated by the cross section in Fig. 5.24.

Before introducing such a technology into production, a number of challenges have to be mastered. An acceptable yield has to be obtained. Since no subsequent repair of an embedded component is possible the use of known good dice is essential. Furthermore, via formation and metallization process must be highly reliable. The reliability of the CIP package concept still has to be proven. CIP is basically a compound of materials with quite different Young's moduli and thermal expansion coefficients, which might give reason for cracking and delimitation. This requires a detailed understanding by modeling and possibly an adaptation of technological parameters. The RF characteristics have to fulfill requirements of future applications, i.e., several GHz of bandwidth. This requires the use of polymers with low dielectric losses and

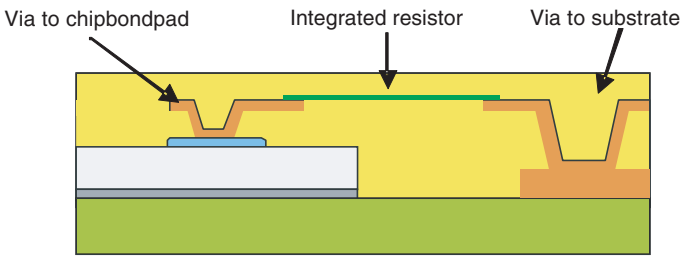

Fig. 5.23. Principle of the chip in polymer structure with embedded chip and integrated resistor

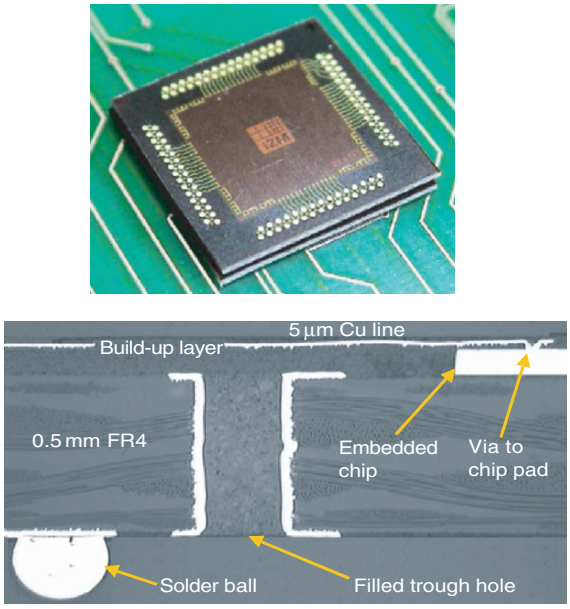

Fig. 5.24. Chip stack and cross section of a stackable package in CIP technology

low dielectric constant as well as very low tolerances for conductor geometries. A power management concept for components with high power dissipation has to be developed. Since no convection cooling of embedded active chips is possible, materials with low thermal resistance have to be used. Integrated resistors have to achieve sufficiently low tolerances, especially in order to be suited for RF circuits. This requires a processing technology with high geometrical resolution and tight control of deposition parameters. Finally, a new production flow has to be established in which chip assembly and testing will be part of substrate manufacturing.

However, CIP technology is a promising approach to obtain 3D assemblies using board integration technologies to meet the target in terms of low cost. Only technologies with the potential to be applied for high volume production are suitable for microelectronic modules integrated in everyday objects and products, and thereby the prerequisite for ubiquitous computing and Ambient Intelligence.

5.6 Wafer-Level Integration by Chip or Wafer Stacking

Most of the currently available industrial 3D stacking approaches of chips or packages only interconnect the layers on the perimeter of the devices. Due to the required high 3D interconnectivity in e-Grains, real 3D interconnections have to be realized within the bulk of the e-Grains.

The 3D inter-chip via (ICV) technology allows a very high density vertical inter-chip wiring. Especially vertical system integration technologies with freely selectable ICVs have a strong demand for 3D system design methods enabling the high performance of extremely miniaturized 3D systems. Manufacturing technologies that largely rely on wafer fabrication processes show a comparatively favorable cost structure. On the other hand wafer yield and chip area issues may be an argument against wafer stacking concepts. In consequence, the so-called chip-to-wafer technologies mainly based on WL processes and utilizing only known good dice will be of advantage. In Fig. 5.25 wafer-to-wafer and chip-to-wafer concepts for vertical system integration are shown in principle.

Vertical system integration in general is based on thinning, adjusted bonding, and vertical metallization of completely processed device substrates by ICVs placed at arbitrary locations. For wafer stacking approaches, the step raster on the device wafers must be identical. This is easily fulfilled for 3D integration of devices of the same kind (e.g., memories) but in the general case of different device areas, the handicap of processing with identical step raster would result in active silicon loss and in consequence increase the fabrication cost per die. In most cases this restriction is even more serious than the yield loss by stacking a non-functional die to a good die. For chip-to-wafer stacking approaches the starting materials are completely processed wafers

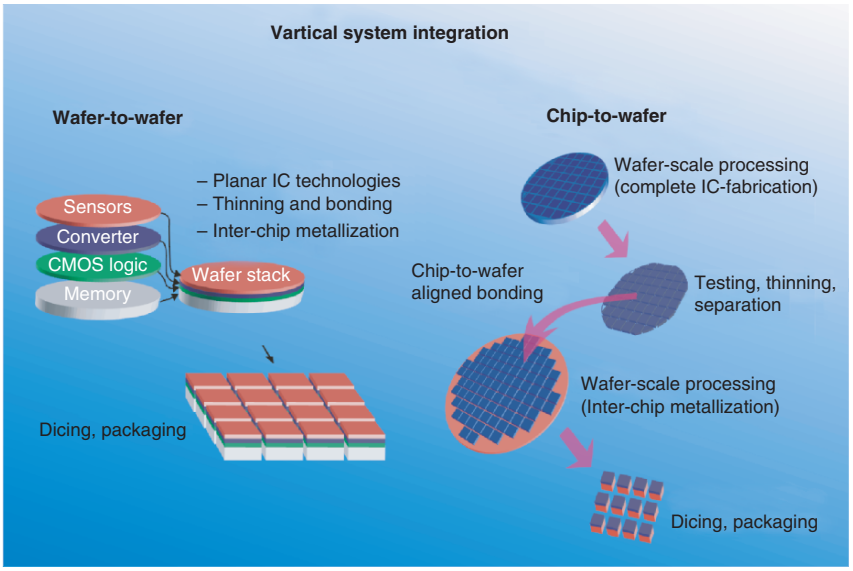

Fig. 5.25. Vertical system integration; wafer-to-wafer versus chip-to-wafer stacking concept for fabrication of vertical integrated systems

too. After WL testing, thinning, and separation, known good dice of the top wafer are aligned bonded to the known good dice of a bottom wafer. This process step represents the only one at chip-level within the total vertical system integration sequence. The subsequent processing for vertical metallization is on wafer-scale again. In consequence the development of a new vertical system integration technology with no need for additional process steps on stack level is in progress. The so-called ICV-SLID concept (Ramm et al. 2003, 2004) is based on the bonding of top chips to a bottom wafer by very thin Cu/Sn pads, which provide both the electrical and the mechanical interconnect. The new approach combines the advantages of the well-established ICV process and the solid–liquid-inter-diffusion technique, which is already successfully applied for face-to-face die stacking. The ICV-SLID concept is a non-flip concept. The top surface of the chip to be added is the top surface after stacking it to the substrate. The ICVs are fully processed – etched and metallized – prior to the thinning sequence, with the advantage that the later stacking of the separated known good dice to the bottom device wafer is the final step of the 3D integration process flow. As a fully modular concept, it allows the formation of multiple device stacks. Figure 5.26 shows the schematic cross section of a vertically integrated circuit fabricated in accordance with the ICV-SLID concept, also indicating the stacking of a next level chip.

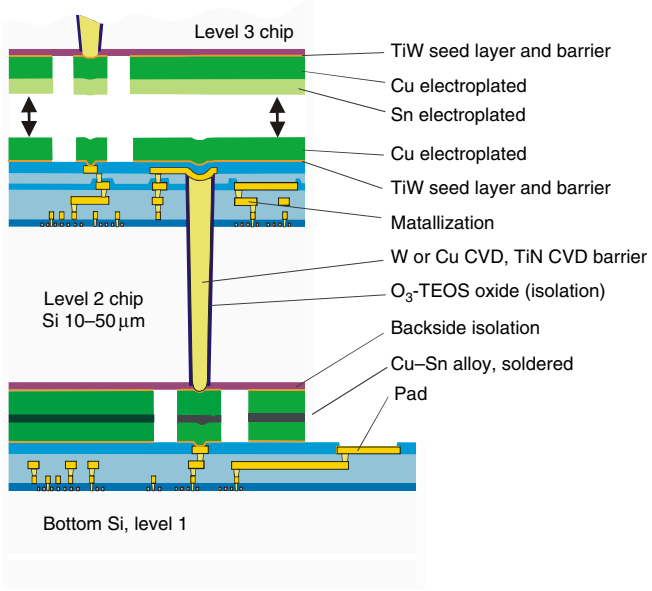

Fig. 5.26. ICV-SLID technology: schematic for the formation of multiple device stacks

For RF-application, low capacitance RF-vias have to be realized. Vias with diameters from 50 to 100 µm are generally required for this application. Metallization can be partially realized in the via hole, filling the hole with dielectrics in a subsequent step.

5.7 Autonomous Energy Supply for e-Grains

Effective power supply of autonomous electronic systems and sensor nodes is a major challenge and a limiting factor for the performance. In general two power supply methods exist: storing the needed amount of energy on the node or scavenging available ambient power at the node.

As the system size decreases, designing a sufficient energy supply is becoming increasingly difficult. Therefore, the power supply is usually the largest and most expensive component of the emerging wireless sensor nodes currently proposed and designed. Furthermore, the power supply (e.g., a battery) is also the limiting factor on the lifetime of the system. If wireless sensor networks are to become ubiquitous, replacing batteries in every device is simply too expensive. Using replaceable batteries in a system smaller than $1\,\mathrm{cm}^3$ may also be difficult.

The most important metrics for power supply technologies are power and energy density as well as lifetime for energy storage devices and power density for harvesting devices. The volumetric energy density of coin type primary batteries like alkaline (0.2–0.3 $\mathrm{W\,h\,cm^{-3}}$), silver oxide (0.3–0.4 $\mathrm{W\,h\,cm^{-3}}$), and lithium (0.4 $\mathrm{W\ h\ cm^{-3}}$) batteries does not differ much from the energy density values of the active materials since packaging contributes much to the volume of small batteries. Zinc–air batteries have the highest energy density (1–1.2 $\mathrm{W\,h\,cm^{-3}}$) of commercially available primary batteries, but the lifetime is limited to few months, which makes them unsuitable for most autonomous systems.

Rechargeable batteries like NiMH- or Li-batteries are used to store energy, which is supplied for example from solar cells. Power density of most coin type secondary batteries is small, but recently some systems have been developed which show good high current behavior. In comparison to Li-button cells Li-polymer batteries have a much higher power density because of the layered thin structure of electrodes and electrolyte, but they are currently not available at sizes below approximately $1\,\mathrm{cm}^3$.

Power harvesting of the environment to continuously fill the electrical storage device of the system can be achieved in different ways and strongly depends on the environmental conditions at the location of the device. Some examples of energy conversion methods are summarized in Table 5.1.

Practical applications are at present more or less limited to solar cells. Standard lighting condition, that means the incident light at midday on a sunny day, yields $100\,\mathrm{mW\,cm^{-2}}$. But in indoor conditions this value is easily reduced by a factor of 20. Single crystal silicon solar cells exhibit efficiencies of 15–20%.

Table 5.1. Examples of realized micropower energy conversion modules for the use of ambient energy to power autonomous systems

energy	conversion module	power density
light radiation	photovoltaic modules	$0.01 - 20\,\mathrm{mW\,cm^{-2}}$ (Hahn 2002)
thermal energy	thermoelectric devices	$10 - 100\,\mu\mathrm{W\,cm^{-3}}$ (Böttner 2002)
mechanical energy: vibrations, air flow, pressure variations, movements of humans, etc.	piezoelectric generators, rotary electromagnetic engines	$100{-}1,000\,\mu\mathrm{W\,cm^{-3}}$ (Roundy et al. 2003)
chemical energy	bio-fuel cells	$175\,\mu\mathrm{W\,cm^{-2}}$ (O'Neill and Woodward 2000, Palmore palmore2000)

5.8 Wafer-Level Integration of Lithium-Polymer Batteries

For systems which receive their power from ambient energy as shown in Table 5.1 or from fuel cells a temporary energy storage is needed in most cases, since time and quantity of the supplied power do not correspond with the instantaneous power demand of the device. The electrical energy can be stored in a secondary battery or in a capacitor. Ultra-capacitors represent a compromise between batteries and standard capacitors. Their energy density is about one order of magnitude higher than standard capacitors and about one to two orders of magnitude lower than rechargeable batteries.

Lithium-polymer batteries have the highest energy density of all commercially available secondary batteries. They are in widespread use in portable electronics with capacities between 100 and approximately 1,000 Ah. Due to the layered structure of thin foils, their power density is quite high. They can easily be adapted to the dimension of the device and are flexible in size. Miniaturization of these batteries down to sizes below approximately $1\,\mathrm{cm}^3$ leads to a reduction of energy density, since the fraction of the battery package increases at the expense of active material.

Figure 5.27 shows the energy density of small Li-polymer batteries as function of battery thickness. There is a significant reduction of energy density at thicknesses below 1 mm because the thickness of the packaging foil becomes dominant.

High energy density of small (mm) size batteries can only be maintained, if the volume fraction of the battery package is reduced. Neither the coin type metallic casing nor the Al-polymer foil package is suited for e-Grain batteries. Small geometrical dimensions, minor discharge as well as a long lifetime, are

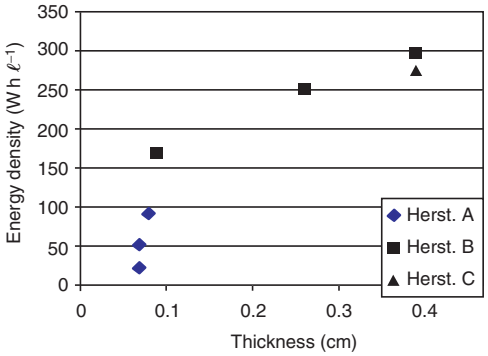

Fig. 5.27. Energy density of small lithium-polymer batteries as function of battery thickness

additional specifications for secondary batteries used in miniaturized electronic systems. Furthermore, a fast charge rate and cost saving production technology are desirable.

The packaging foil and the sealed seam used for battery encapsulation make it difficult to reduce the battery size of conventional Li-batteries. To achieve high energy density for small size batteries new encapsulation techniques are necessary. A new encapsulation technology based on parylene was investigated at Fraunhofer IZM. Parylene deposition followed by a final metallization allows the production of secondary Li-batteries with a maximum relationship of active material to the encapsulation material. A cross-sectional view and a picture of the WL Li-battery are shown in Figs. 5.28 and 5.29. The moisture vapor transmission of parylene is better than most polymers while the gas permeation of O_2 and N_2 is comparable to epoxies. Since most of the battery is covered with thin film metal, only a small area of some square micrometer of parylene at the current feed through are effective for gas permeation and a nearly hermetic package can be realized.

A high number of batteries can be produced and encapsulated at the same time using WL technology. The arbitrary footprint of the battery allows the best utilization of the available space in small electronic systems like e-Grains. The thickness of a single battery assembly is reduced because the encapsulation layer is very thin. A satisfactory way to boost the deliverable capacity while avoiding a raise of the internal resistance is by creating a battery stack.

5.9 Micro-fuel Cell Integration

As improvements in battery technology have so far been limited to energy density increases of only a few percent per annum, over the past few years many R&D activities have concentrated on alternative forms of miniature power supply. One of the most promising candidates is micro-fuel cell (FC) based on polymer electrolyte membranes (PEM). Compared to batteries the

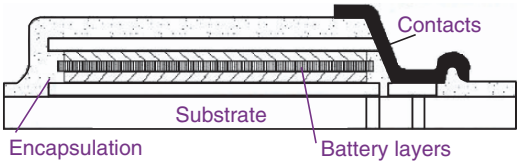

Fig. 5.28. Cross-sectional view of a WL Li-battery

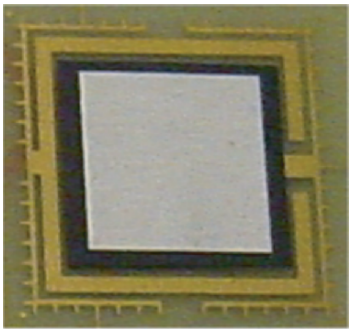

Fig. 5.29. Prototype of a WL Li-battery

environmental impact of fuel cells is much lower (Hahn and Müller 2000). Table 5.2 gives an energy density comparison of fuel cells and batteries, showing the potential of this technology.

Fuel cells operate on the same principle as batteries, converting energy electrochemically, but are "open" systems where the reactor size and configuration determine the energy and power output. Since a single fuel cell has an operation voltage of approximately 0.5 V, a multitude of cells are needed which are typically assembled in stack configuration.

A fuel cell stack can be subdivided into three constituent component groups: the membrane electrode assemblies (MEAs) which fulfill the electrochemical function of the fuel cell, the bipolar plates (commonly consisting of graphite and carbon-filled polymers) which supply the MEAs with hydrogen and oxygen, provide cooling and conductive electronic paths, and the gas diffusion layers (GDL) which are inserted between MEAs and bipolar plates to distribute the reactants uniformly. Fuel cells of the air-breathing type use ambient air as an oxidant. PEM fuel cells operate with hydrogen. At the moment there is no hydrogen storage available which is suitable for miniature applications. For direct methanol fuel cells (DMFC) a better storage opportunity exists in the form of methanol cartridges.

At Fraunhofer IZM technologies for WL fabrication of planar PEM fuel cells between 1 mm^2 and approximately 1 cm^2 have been developed (Schmitz et al. 2003; Wagner et al. 2003). The investigations focused on patterning technologies for the fabrication of microflow fields, design studies for integrated

Table 5.2. Comparison of PEM micro-fuel cell with $NaBH_4$ hydrogen generator and Li-polymer secondary battery in $1\,cm^3$ size; 0.5 mm housing thickness was assumed

	micro-fuel cell with $NaBH_4$ hydrogen generation	wafer-level Li-polymer battery
$1\,cm \times 1\,cm \times 200\,\mu m$		
voltage	(0.5 V) 1.5 V (at 40 mW)	4.1–3 V
power	40 mW	5–20 mW
energy	–	3.5 mW h
$1\,cm \times 1\,cm \times 1\,cm$		
voltage	(0.5 V) 1.5–7.5 V	4.1–3 V
power	$40 - 200\,mW$[a]	150–600 mW
energy	500 mW h	150 mW h

[a] Micro-fuel cells on five sides of the cube.

flow fields, material compatibility for fuel cells, patterning of membrane electrodes, serial interconnection of single cells in a planar arrangement, laminating, and assembling processes. Although wafer technologies were applied, foil materials were used which allow low-cost fabrication in future production.

Prototypes of self-breathing PEM fuel cells with a size of $1 \times 1\,cm^2$ and 200 µm thickness were fabricated. V/I curves were measured at a variety of ambient conditions. Fuel cells with 40 mA output current at 1.5 V ($= 120\,mW\,cm^{-2}$, 25°C, 50% RH) have been successfully demonstrated. Cell performance was validated under varying ambient conditions. Stable long-term operation at $80\,mW\,cm^{-2}$ was achieved. The total performance of the micro-fuel cells is in the same range of current and power density as the best conventional planar PEM fuel cells (Wagner et al. 2005). At the same time this technology offers a high degree of miniaturization and the capability for mass production which is a clear success of the micropatterning approach. Figure 5.30 shows a micro-fuel cell based on foil technology.

Since storage of gaseous hydrogen is not practical in small size applications activities are focused on developing a micro-chemical reactor that produces hydrogen on demand from $NaBH_4$ and water, and yields an energy density of $800\,W\,h\,l^{-1}$. A possible integration of fuel cells and storage container into a $1\,cm^3$ e-Grain is schematically illustrated in Fig. 5.31.

Power supply for wireless sensor nodes like e-Grains is a real challenge. Storing the energy needed for long operation periods of the e-Grain is conflicting with the aim of miniaturization. Size reductions may be achieved, when micro-fuel cells are available with higher energy density compared to primary batteries, which are the well-established sources at the moment. For widespread use and miniaturization of the systems the power harvesting of ambient energy or use of alternative power sources is essential. In this context a small size secondary energy storage is needed which can be easily integrated. A combination of standard Li-polymer battery processing and wafer technologies is considered to reduce battery dimensions to chip size and keep

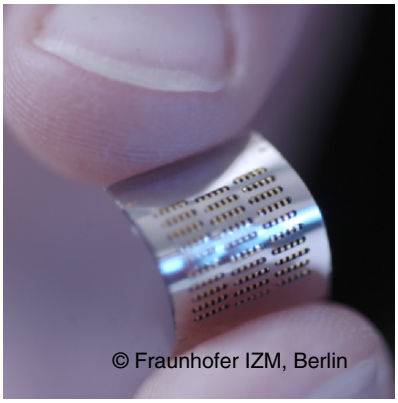

Fig. 5.30. Flexible micro-fuel cell demonstrator: size $1\,\mathrm{cm}^2$, thickness $200\,\mu\mathrm{m}, 80\,\mathrm{mW\,cm}^{-2}$

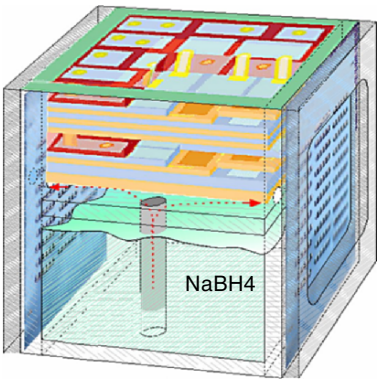

Fig. 5.31. Schematic micro-fuel cell cube, which comprises the electronic part on top, micro-fuel cells at the sides, and a chemical hydride hydrogen generation system

fabrication cost low. A great effort is still needed to realize the WL battery. Table 5.2 gives an overview of energy and power densities obtainable in $1\,\mathrm{cm}^3$ size systems.

5.10 Summary and Outlook

The e-Grain concept attempts to link all types of system integration techniques and represents a full value chain from microelectronics and microsystems. The realization of these future ultra-miniaturized self-sufficient wireless sensor nodes requires heterogeneous technologies on wafer and substrate level, including advanced assembly and interconnection technologies, integration of passive devices, thin circuit device and sensor integration, flexible functional substrate and 3D vertical integration at WL, etc.; see Figs. 5.32 and 5.33.

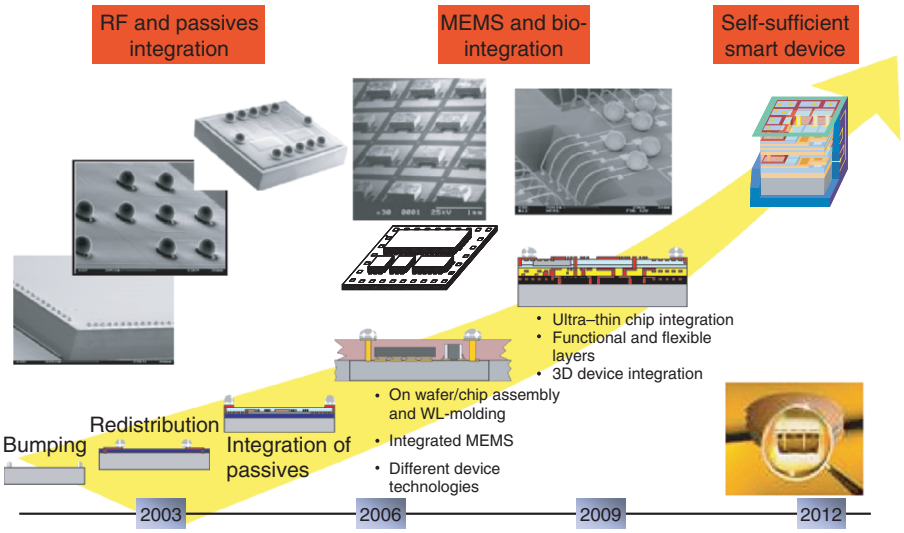

Fig. 5.32. Technology roadmap for WL integration

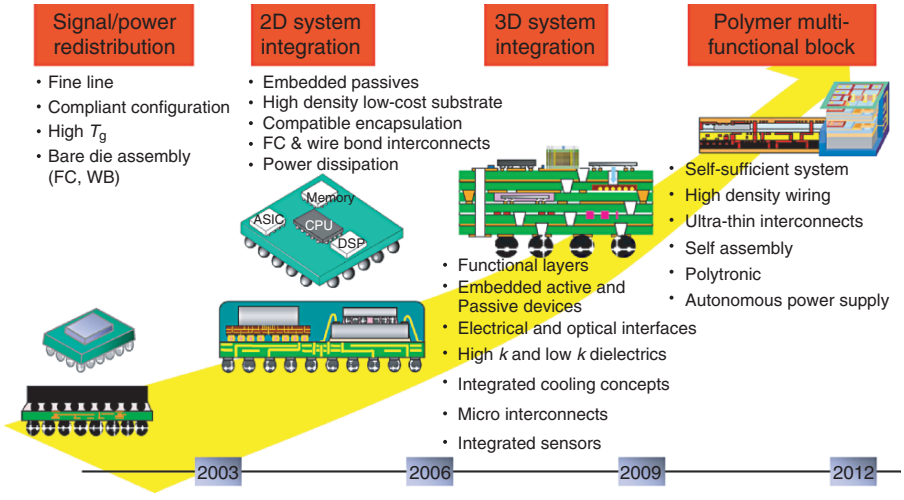

Fig. 5.33. Technology roadmap for substrate level integration

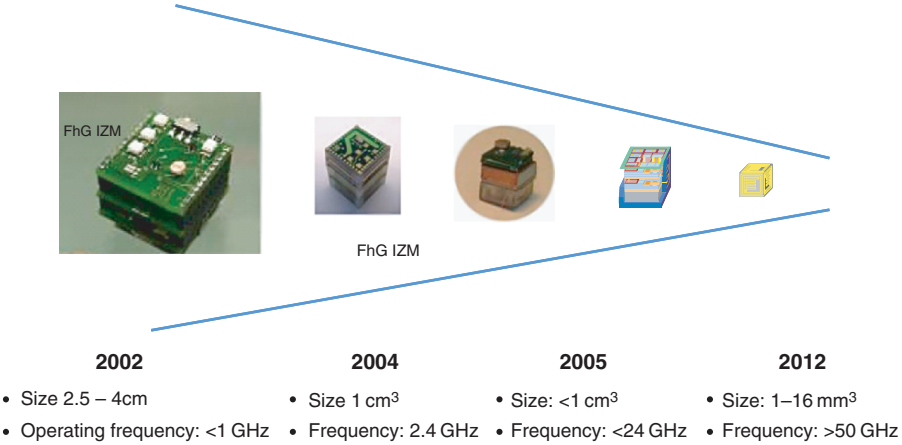

Fig. 5.34. Miniaturization roadmap for self-sufficient wireless sensor nodes (e-Grains)

Contemporary technologies at wafer and substrate level can be used to realize fully functional wireless sensor nodes in a volume of less than $1\,cm^3$. The progress in silicon and integration technologies will result in e-Grains with a size of few cubic millimeters in the next decade; see Fig. 5.34.

Perhaps in just a few years time, a system for an individual specific application will no longer be developed in the currently known way of today. Instead, it will use few grams of universal e-Grains that can be integrated in any human environment and will meet specific information or communication needs through application specific software-based networking. So the future e-Grain may become a "standard component" like microprocessors today.