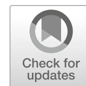
Chapter 2
SiC Single Crystal Growth and Substrate Processing



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2.1 Introduction for SiC Single Crystal Materials

Silicon carbide (SiC) is a IV-IV compound material. In the basic structure unit of SiC, the silicon atoms and carbon atoms are combined together by sp3 covalent bonding, where each carbon atom is surrounded by four silicon atoms and vice versa. The extremely strong Si-C bonds give it unique physical, chemical, and mechanical properties [1], such as high electric breakdown field, high thermal conductivity, and so on. In addition, SiC is well known for its polytypism. The polytypic nature of SiC is that the crystal structure of SiC owns different ordering sequences in one dimensional with the same stoichiometry. And up to now, more than 250 SiC polytypes have been identified [2]. Meanwhile, different SiC polytypes exhibit distinct properties. Currently, the main polytypes of SiC used for device fabrication are 4H-SiC and 6H-SiC. 4H-SiC is an ideal material for power electronic and high-frequency devices, while 6H-SiC is usually employed for optoelectronic device fabrication.

The study about SiC has a quite long history. SiC was first discovered in the process of synthesizing diamond by Berzelius in 1824 [3]. Later, in 1885, Acheson invented a method for SiC preparation in melting furnace. The synthesis process was named as "Acheson process" afterward [4]. In this process, silica and coke are used as the source materials, while salt is employed as additive. The main product of Acheson process is SiC powder, which is mainly used as an abrasive in the processing technologies such as cutting, grinding, and polishing. The by-products in this process are mainly small 6H-SiC plates. In 1905, French scientist Moissan discovered the natural SiC in meteorites, which inspired the intensive interests in

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the potential application of SiC [5]. After that, a series of simple SiC-based devices were fabricated. In 1907, the first SiC light-emitting diode (LED) was made by an engineer named Round [6]. In 1920, SiC-based sensor was applied in the radio receivers. However, at that time, there was no efficient method to synthesize SiC single crystals with high quality. As a result, the development of SiC growth once got stranded. Up to now, many methods have been invented for SiC single crystal growth, including vapor growth and solution growth.

2.1.1 Vapor Growth Method

In 1955, Jan Antony Lely proposed a sublimation technique to prepare SiC single crystals, which opened up a new era of SiC material and devices [7]. This method was name as Lely method later. The schematic diagram of Lely method is shown in Fig. 2.1. The industrial-grade SiC powder was used as source material and placed around the dense graphite crucible wall. The porous graphite was employed to separate the source material and the growth cavity. In the crucible, the temperature around the crucible wall was higher than in the center of the crucible. As a result, the growth was driven by the temperature gradient in the crucible. At first, the source material sublimated at high temperature (about 2500 °C); thus gas species was produced. After that, the vapors penetrated into the porous graphite to grow lamellar crystals on the inner surface. During the growth, argon was used as inert gas, and the pressure in the growth chamber was kept around 1 atm. The gas species randomly nucleated at the inner cavity wall. The defects and micropipe density in

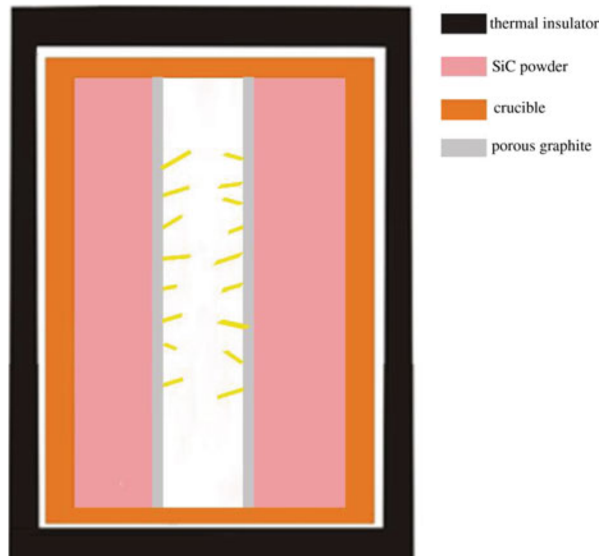


Fig. 2.1 Schematic diagram of Lely method for SiC crystal growth (Provided by Dr. Yan Peng at Shandong University)

the grown crystal are pretty low, which means this method can prepare 6H-SiC single crystals with high quality. However, crystals obtained by this method are in small size and irregular shape. Therefore, the crystals cannot be used for device fabrication. At the same time, due to the random nucleation at the inner cavity wall, 4H and 15R-SiC polytype inclusions often appeared in the grown crystals.

In order to solve the problem of polycrystalline nucleation, Tairov and Tsvetkov modified Lely method by an innovative use of SiC seed in 1978 [8]. The modified Lely method (also called "seed sublimation method" or "physical vapor transport method") was constituted of three steps: (1) sublimation of SiC source material, (2) mass transport of sublimed gas species, and (3) surface reaction and crystallization. The schematic diagram of growth furnace is shown in Fig. 2.2. In this method, SiC powder is put at the bottom of the crucible, and the seed is kept on the lid of the crucible. The distance of source-to-seed is in the range of 30–50 mm. Electromagnetic induction is employed to heat up the crucible in the temperature range of 2100–2400 °C. The graphite felt or porous graphite is used as thermal insulation. During the growth process, high purity argon is flowed as carrier gas, and the pressure in the growth chamber is kept at 20–60 mbar. The SiC powder was decomposed at high temperature, generating Si, Si2C, and SiC2 gas species. The gas species driven by the temperature gradient are transported to the seedand then

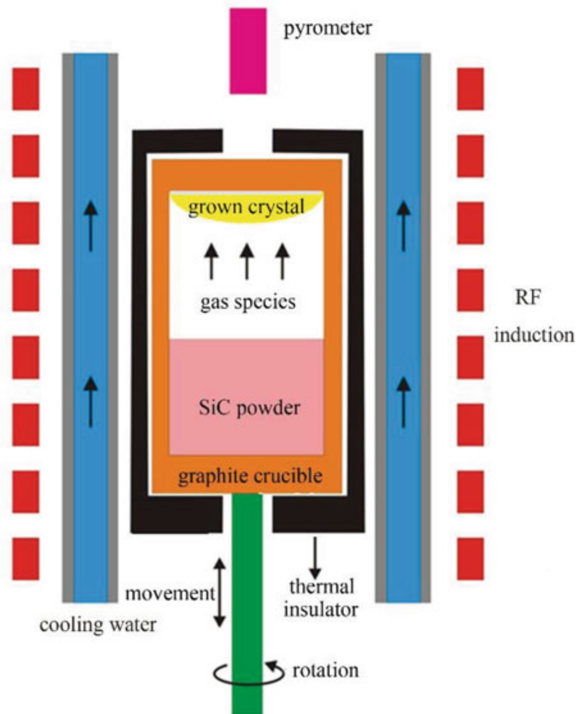
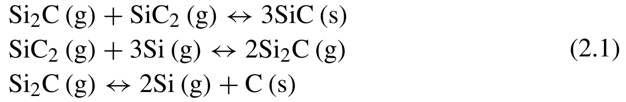


Fig. 2.2 Schematic diagram of a modified Lely method for SiC crystal growth (Provided by Dr. Xianglong Yang at Shandong University)

crystallize on the seed. During the growth, the main reactions were summarized as follows:



$$
\begin{aligned}
&Si_2C\,(g) + SiC_2\,(g) \leftrightarrow 3SiC\,(s)\\
&SiC_2\,(g) + 3Si\,(g) \leftrightarrow 2Si_2C\,(g)\\
&Si_2C\,(g) \leftrightarrow 2Si\,(g) + C\,(s)
\end{aligned}
\tag{2.1}
$$

In this method, the crystal was grown approximately along isotherm lines. As a result, it is crucial to design the thermal field. Though micropipes and dislocations are commonly observed in the crystals grown by this method, the modified Lely method is currently the most mature method for growing bulk SiC single crystals. Using this method, 6H-SiC and 4H-SiC have been commercialized since 1991 and 1994, respectively. Recently, in Cree Research Inc., 4H-SiC single crystals with a diameter of 200 mm were successfully grown [9].

2.1.2 Solution Growth Method

Besides vapor growth, solution is another SiC single crystal growth method. Different from other semiconductor materials (such as Si and GaAs), SiC does not have any liquid phase in normal engineering conditions. According to theoretical analysis, the liquid phase of SiC appears only under high-pressure (>105 bar) and high-temperature (>3200 °C) conditions [10]. The solubility of carbon atoms in melting silicon varies from 0.01 to 19% in the temperature range of 1412–2830 °C. Recent study revealed that the solubility of carbon atoms in melting silicon can be increased by adding transition metal or rare earth metals to silicon solvent [11]. Consequently, it is possible to grow SiC single crystals by solution technique. As shown in Fig. 2.3, high purity graphite crucible is used as both container and

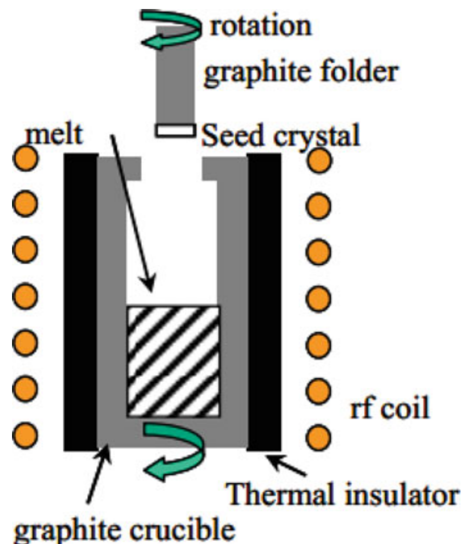


Fig. 2.3 Schematic diagram of a SiC solution growth heated by RF induction

carbon source. High purity Si and metals (such as Ti, Cr) are mixed and put in the crucible at argon atmosphere. SiC seed is mounted on a graphite folder. The typical growth temperature is in the range of 1600–1750 °C. During the growth, the seed is dipped into the ternary solution gradually, while the seed and crucible are rotated in opposite direction. Given that the crystals are grown under near thermal equilibrium condition, there are little micropipes and dislocations in SiC crystals grown by solution method. Therefore, high-quality SiC crystals can be grown by solution method.

2.1.3 High-Temperature Chemical Vapor Deposition (HTCVD) Method

HTCVD is the third method for bulk SiC single crystal growth. High growth rates and long SiC single crystals are expected by this method in comparison with PVT and solution methods. Figure 2.4 is a schematic illustration of a HTCVD SiC growth method [12]. A graphite heater is heated by induction coils and a cylindrical insulator is on the outside of the heater. A seed crystal was fixed on the seed holder. The Si and carbon sources are SiH4 and C3H8, respectively. H2 is used as carrier gas. At high temperature, the source gases were cracked and transformed into the reaction species such as Si, SiC2, Si2C, and C2H2. Then the species were deposited on the seed crystal. HTCVD method has the following advantages: one is the continuous gas source supply. This enables long-term growth which contributes to a long SiC crystal ingot; the other is the accurately controllability of the partial

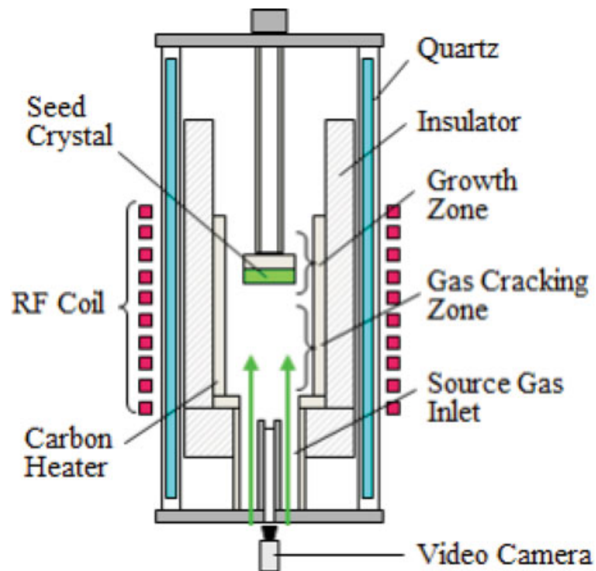


Fig. 2.4 Schematic illustration of the structure of a HTCVD SiC growth method

pressure, the gas flow, and the species ratio of the source gases which make the possibility to grow SiC crystal with Si/C stoichiometry; in addition, high purity semi-insulating SiC crystal can be grown by using high purity gas source.

In summary, SiC bulk single crystals can be grown by PVT, solution, and HTCVD. PVT is a conventional SiC crystal growth method and suitable for mass production. In comparison, the solution and HTCVD are suitable for the high structural quality SiC and the high purity semi-insulating SiC crystal growth, respectively.

2.2 Structure and Physical Properties of SiC

SiC possesses excellent mechanical, thermal, electrical, physical, and chemical properties which make it an ideal semiconductor material for the fabrication of the novel electronic and optoelectronic devices. From a viewpoint of crystallography, SiC is the best known example of polytypism. The variation in occupied sites along the c-axis in a hexagonal close-packed system brings about different crystal structures which were termed as polytypes. Figure 2.5 shows schematically the structures of typical SiC polytypes [13]. There are three possible sites, denoted by A, B, and C. Two layers cannot successively occupy the same site. For example, the next layer on the top of an “A” layer must occupy either “B” or “C” sites. In principle, there are infinite possibilities for the stacking sequence. However, for most materials, only some stacking structures are stable such as the zinc blende or wurtzite structure. For SiC, there are more than 200 polytypes. Polytypes are represented by the number of Si-C bilayers in the unit cell and the crystal system (C for cubic, H for hexagonal, and R for rhombohedral). 3C-SiC is often called β-SiC and other polytypes are termed as α-SiC. The structures of popular SiC polytypes

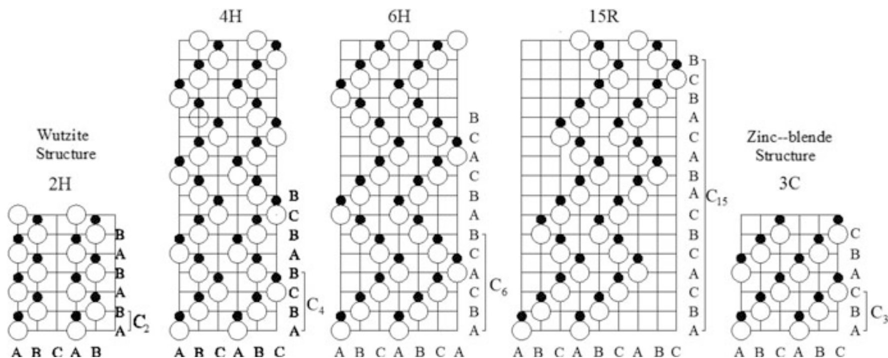


Fig. 2.5 Schematic diagram of SiC structure with different polytypes viewed along [11–20] direction in hexagonal system

Table 2.1 Comparison of basic properties of several semiconductor materials

Property/material	4H-SiC	6H-SiC	Si	GaAs
Thermal conductivity (W/cm K)	4.9	4.9	1.3	0.5
Bandgap (eV)	3.2	3.0	1.12	1.42
Intrinsic material transparent	Yes	Yes	No	No
Available doping	n, p	n, p	n, p	n, p
Saturated electron drift velocity (10^7 m/s)	2.0	2.0	1.0	2.0
Electron mobility (cm^2/Vs)	1000	600	1450	8500
Critical breakdown electrical field (MV/cm)	3	3.2	0.3	0.6
Lattice constant (a)	3.073	3.081	3.84	4.00
Lattice mismatch with GaN (%)	3.8	3.5	−17	−22
Thermal expansion mismatch with GaN (%)	−0.11	−0.12	−0.17	0.11

are 4H, 15R, 6H, and 3C as shown in Fig. 2.5 where open and closed circles donate Si and C atoms, respectively.

Considering the immediate neighbor site of Si-C bilayer stacking, the lattice sites with hexagonal-structured surroundings are termed as "hexagonal sites," and those with cubic-structured surroundings are called as "cubic sites." 4H has one hexagonal and one cubic site and 6H-SiC one hexagonal and two inequivalent cubic sites, while 3C-SiC contains only cubic sites. Hexagonal and cubic sites differ in the location of the second-nearest neighbor leading to different crystal fields. As a consequence, the energy levels of dopants, impurities, and point defects are affected by the lattice site or the hexagonal/cubic ratio. It has been found that the bandgap of SiC polytype increases monotonically with the increase of its hexagonality. The bandgap at room temperature is 2.36 eV for 3C-SiC, 3.26 eV for 4H-SiC, and 3.02 eV for 6H-SiC, respectively.

Compared with the first-generation semiconductor Si and the second-generation semiconductor GaAs, the third-generation semiconductor SiC possesses better physical and chemical properties. Table 2.1 lists the basic properties of several semiconductor materials [14]. From this table, we can see that SiC has higher thermal conductivity, wider bandgap, higher hardness, and higher chemical stability.

The basic properties of SiC material make the electronic devices the follow advantages:

1. The bandgap of SiC is nearly three times as that of Si. Wide bandgap can assure the long-term reliability of device which runs at high temperature. At high temperature, intrinsic carrier excitation will occur, which further causes the device failure. The wider the bandgap, the higher the device limit operating temperature. The limit operating temperature for Si device is lower than 200 °C. In contrast, the limit operation temperature for SiC device exceeds 400 °C.
2. The critical breakdown electrical field of SiC is ten times as that of Si. Thus, SiC can sustain much higher voltages than Si. Devices can be shrunk in size reducing the resistive losses. It reduces system complexity and cost while improving reliability.

3. SiC has a much higher thermal conductivity roughly three times as that of silicon. For SiC device, heat is conducted away much more effectively. It greatly reduces complexity of cooling systems.
4. SiC can carry much higher currents almost five times as that of silicon. It can reduce the area of devices and further reduce the parasitic capacitance.
5. Power devices made from SiC can switch roughly ten times faster than those made from silicon. Therefore, the power conversion circuits operate faster for SiC devices. It means much smaller energy storage capacitors and inductors can be made from SiC.

In addition to the above advantages, SiC is also an ideal substrate for the fabrication of GaN-based optoelectronics and radio frequency devices due to small lattice mismatch with GaN.

Therefore, SiC as the representative of third-generation semiconductor materials has extensive application prospects.

2.3 SiC Single Crystal Growth by PVT Method

From the phase diagram of the Si-C binary system, we know that it is very difficult to obtain stoichiometric SiC liquid phase. It is impossible to employ congruent melt method for SiC single crystal growth. Up to now, the most successful growth method for bulk SiC single crystal is PVT method which consists of the following procedures: (1) sublimation of SiC source, (2) mass transport of sublimed species, and (3) surface reaction and crystallization. Therefore, PVT method was also called as sublimation method.

The principle and growth furnace for the PVT method has been introduced. In order to grow high-quality SiC single crystal, both thermodynamic and kinetic factors must be considered. The process control to maintain optimal thermal and chemical conditions is very important so that an ideal growth interface can be obtained.

Figure 2.6 shows the partial pressures of SiC sublimed species from SiC-C(s) and SiC-Si(l) systems at high temperature [15]. In the gas phase, the dominant species are Si2C, SiC2, and Si which are not stoichiometric SiC.

In the procedure of SiC growing, SiC powder was decomposed at the temperature higher than 2300 °C; the gas phase in sublimation growth is usually Si-rich. This causes the source more and more rich in carbon, i.e., the graphitization of source. In order to avoid the formation of carbon inclusion in SiC single crystal, Si-rich SiC source is often used.

For the PVT growth of SiC, the growth occurred in a nearly closed graphite crucible. We can only measure the temperature at the upper surface of crucible lid or bottom of crucible by using a pyrometer. It is impossible to know the thermal field inside the crucible. Because growth experiment alone is not sufficient to develop a well-controlled PVT growth procedure, modeling and simulation of SiC PVT

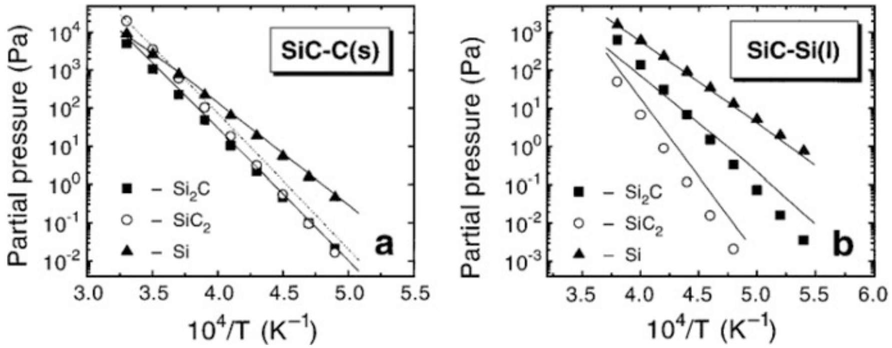


Fig. 2.6 Partial pressures of Si, Si_2C, and SiC_2 vs. temperature calculated for three-phase equilibria: (**a**) SiC-C(s) and (**b**) SiC-Si(l)

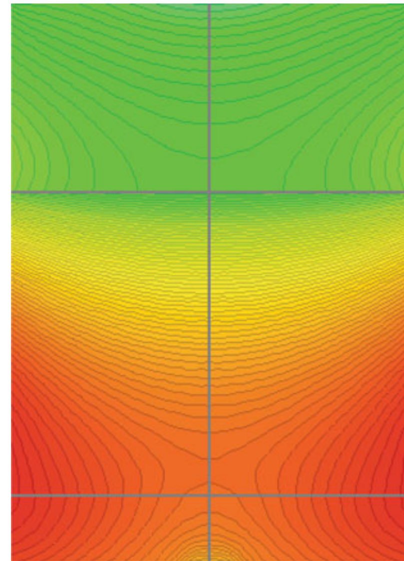


Fig. 2.7 Typical thermal field of SiC PVT growth (Provided by Dr. Yan Peng at Shandong University)

growth are necessary. In the simulation of thermal field, heat transfer by thermal conduction, gas-phase convection, and radiation should be considered. In the heat transfer calculation, the large crystallization energy of SiC must be considered. Heat transfer by radiation is a dominant process at very high temperature in the PVT growth.

Figure 2.7 shows a typical thermal field of SiC PVT growth which was simulated by using a virtual reactor (SiC) software exploited by the semiconductor technology research company. From this figure, the thermal field is described by multiple temperature contour lines. The SiC powder is located in the high-temperature zone of the lower part of the crucible, whereas SiC seed is placed in the low-temperature zone of the crucible lid. At the driving force of temperature gradient, gas species

were transported from the source into the seed, and crystal growth occurred. It has been found that the thermal field was affected by the following parameters such as thickness of insulation shield, shape of crucible, diameter of temperature measurement hole, heating frequency and power, the relative position between crucible and induction coil, etc.

If the influence of mass transport on growth rate is neglected, the shape of SiC growth interface is approximately as same as that of temperature contour lines. For actual crystal growth, a slight convex thermal field is favorable for the thermal stress control and diameter enlargement. Sometimes, to obtain an ideal thermal field, the relative position between crucible and induction coil should be adjusted. Figure 2.8 shows the influence of the relative position between crucible and induction coil on thermal field in which crucible position percent denotes the deviation degree of real crucible position away from standard position.

From Fig. 2.8, we can see that as the crucible move upward corresponding to the increase of crucible position percent, the highest temperature zone shifts toward the crucible bottom. Simultaneously, in the growth cavity, the axial temperature gradient increases, and the radial temperature gradient decreases. Therefore, following the movement of crucible upward, the shape of growth interface will become gradually from convex to plan and vice versa. Figure 2.9 shows a typical as-grown 4H-SiC crystal which has an ideal shape with a slight convex interface.

To predict the growth rate and interface shape, a mass transfer model must be coupled with the heat transfer calculation and the thermodynamic database. In the gas phase, fluid transport is based on the low-pressure kinetic theory of gases. Diffusion coefficients, viscosity, conductivity, and specific heat of species are calculated as a local function of temperature, pressure, and composition. The Stefan flow caused by the phase change of SiC has to be considered. The thermodynamic calculation is performed by minimization of the total free energy of the Si-C-Ar system at high temperature. Calculations indicate that three particular species, Si, Si_2C, and SiC_2, are indeed important to describe sublimation growth [16]. Selder et al. [17] performed the global numerical simulation of heat and mass transfer for SiC bulk crystal growth by PVT. The physical model is based on the two-dimensional solution of the coupled differential equations describing mass conservation, momentum conservation, conjugate heat transfer including surface to surface radiation, multicomponent chemical species mass transfer, and advective flow. The model also includes the Joule volume heat sources induced by the electromagnetic field. Figure 2.10 shows the calculated temperature distribution inside the growth cell and the growing crystal for three different points in time. Due to the existence of radial temperature gradient, the growth front is getting convex. However, the shape of growth front is not only depending on the thermal field at the crystal/gas interface but also influenced by gas species mass transfer especially at the periphery of the growing crystal. As a consequence of two effects, the radial growth rate distribution is smoothed out as the crystal length increases.

Figure 2.11 shows the calculated radial growth rate distributions for the three growth stages. We can see that the growth rate at the crystal center is decreasing with the increase of crystal length, and the radial growth rate distribution is smoothed out

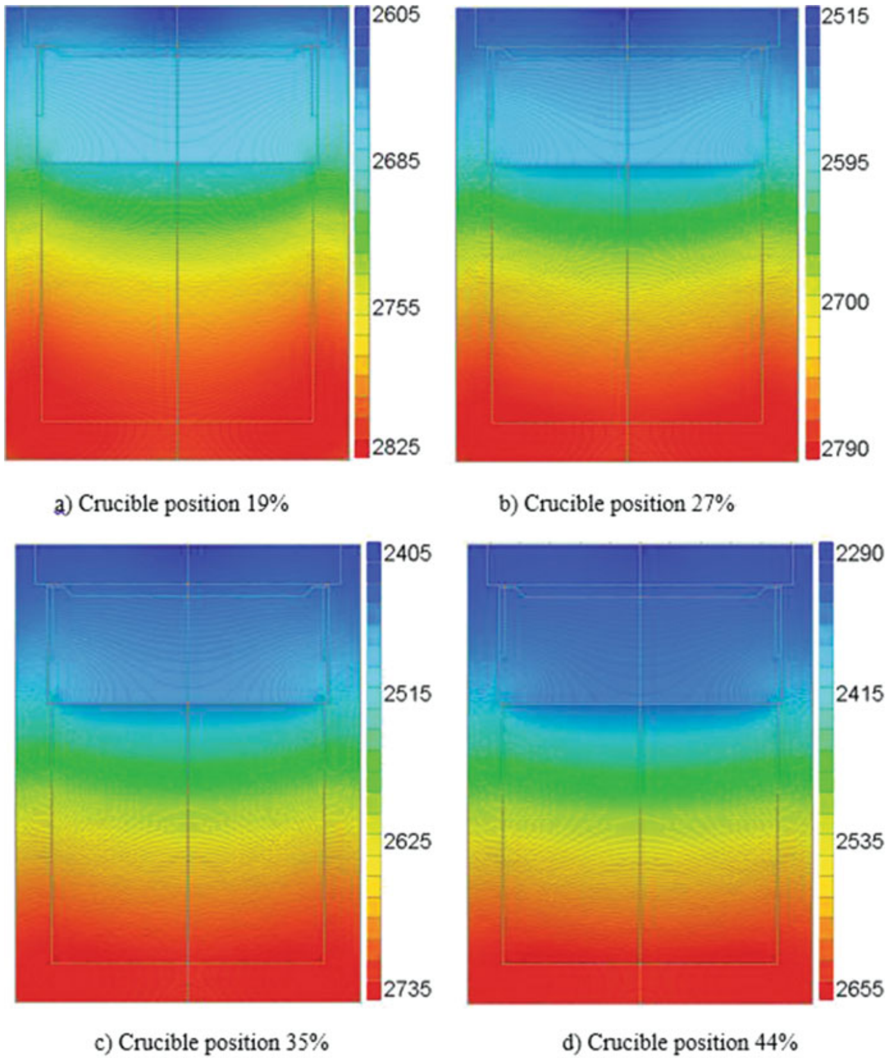


Fig. 2.8 Influence of relative position between crucible and induction coil on the thermal field (Provided by Dr. Peng Y at Shandong University). (**a**–**d**) Correspond to 19% 27%, 35% and 44% crucible position, respectively

with increasing growth time. The above simulation was confirmed by actual SiC single crystal growth experiment.

Figure 2.12 demonstrates a longitudinal cut slice of a SiC crystal. In this figure, dark regions are nitrogen doped, and bright regions correspond to nominally undoped SiC. The positions of the marked and unmarked regions provide the detailed information about the growth front evolution. The crystal growth process is

Fig. 2.9 Photograph of 4 in. 4H-SiC single crystal (Provided by Dr. Peng Y at Shandong University)

in agreement well with the simulations. Especially, the shape of the growth front is similar to the simulation. For both experiment and simulation, the radial growth rate variation is decreasing with the increase of crystal length. By comparing experiment to simulation, it implies that the modeling is successful.

The actual SiC bulk crystal growth via PVT is a complex process in which a number of parameter have to be controlled. The growth rate is a strong function of temperature gradient, source to seed distance, and chamber pressure. The crystal growth procedure includes the following six stages:

1. Low-temperature and high-vacuum stage: At the initial stage, the water and oxygen gas absorbed by graphite parts in growth chamber have to be exhausted, and the chamber pressure is lower than 100 nbar. In the meantime, the crucible was slowly heated to a temperature lower than 1400 °C so that the nitrogen absorbed by graphite material was released and evacuated. If residual oxygen or water exists in the chamber after high vacuum, the crucible and thermal shield materials will be oxidized and damaged.
2. High-temperature and high-pressure stage: In order to control the growth rate so that the nucleation proceeded steadily, the carrier gas Ar was flushed into the chamber, and the pressure in the chamber reached 800 mbar. Because the SiC powder was decomposed into Si, Si_2C, and Si_2C gas species at high temperature, the partial pressures of SiC gas species will be lowered at high background pressure. In this case, the growth rate was controlled at a very low level. It is favorable for SiC nucleation on seed.
3. SiC nucleation stage: At this stage, temperature and pressure were kept stably. SiC was nucleated on seed at a low growth rate. An ideal status is that a large area facet was formed without any structural defects.
4. Pressure decreasing and crystal growth stage: After SiC nucleation was completed, crystal growth rate was fastened by decreasing growth pressure. The growth pressure was decreased from present into a target pressure. Pressure decreasing rate can be expressed as follows:

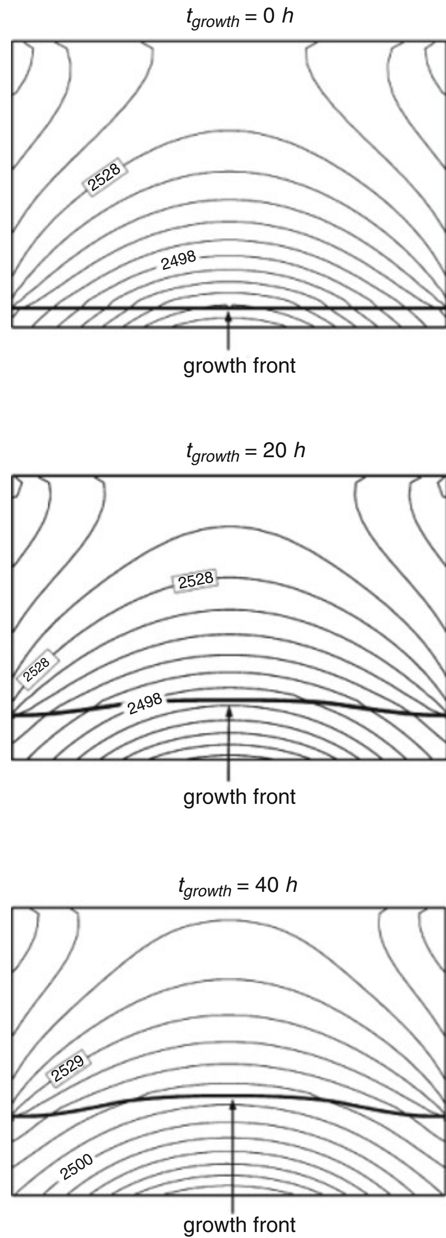


Fig. 2.10 Temperature distribution and growth front for three different points in time during SiC PVT growth. The seed is positioned at the bottom of the individual images. The SiC source is on the top

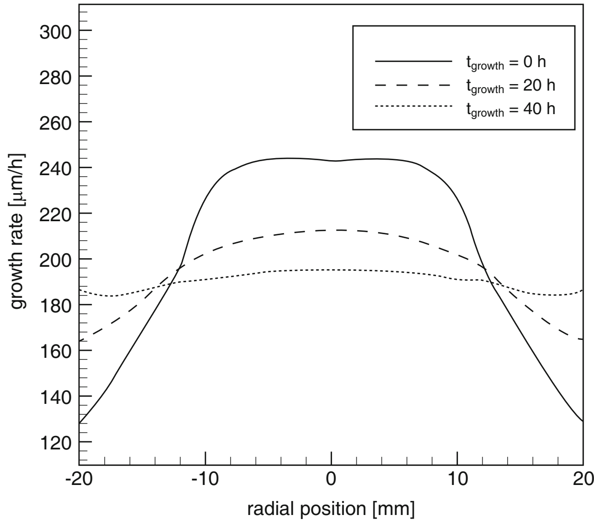


Fig. 2.11 Radial distribution of the calculated growth rate for three different points in time

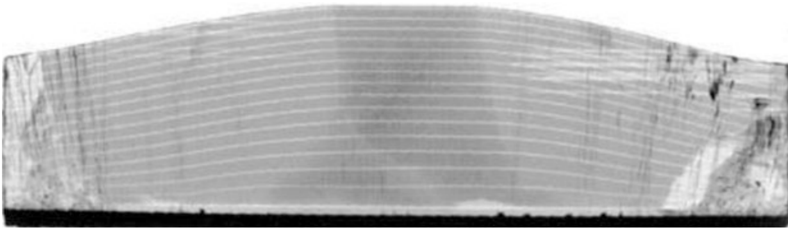


Fig. 2.12 Longitudinal cut slice of a SiC crystal in which the shape of growth front was marked by an interface demarcation technique. Undoped regions exhibit a bright contrast

$$p = p_0 \mathrm{e}^{-t/\tau} \tag{2.2}$$

where p_0 and p donate the present and target pressure, respectively, and τ is constant.

5. Stable crystal growth stage: When the growth pressure reached the target value, the crystal growth proceeded stably at a certain temperature and pressure. The optimal growth rate was proximately 200–300 µm/h.
6. Pressure increasing and cooling stage: When the crystal ingot length was estimated to be 20–30 mm, crystal growth should be terminated by increasing pressure. Then the temperature was lowered slowly into room temperature. The whole growth procedure was ended.

2.4 The Formation and Control of Structural Defects in SiC Single Crystals

SiC single crystals contain various structural defects such as foreign polytypes, micropipes, dislocations, inclusions, point defects, etc. Defects in SiC wafers will deteriorate the device performance and shorten the device lifetime. So defects should be reduced or eliminated.

2.4.1 Micropipe Defects

A micropipe is actually a hollow core associated with a super-screw dislocation. It penetrates through the entire crystal along the c-axis with diameter from tens of nanometers to several micrometers. A SiC device with a micropipe in its active area cannot support significantly high electrical field. Therefore, micropipe is known as a "killer defect" [18]. According to the Frank theory [19], a dislocation whose Burgers vector exceeds a critical value, of the order of magnitude 10 Å, is only in equilibrium with an empty tube at its core. When a micropipe was formed, the elastic strain energy released by the formation of hollow core and surface free energy created by the interior cylindrical surface of hollow core reached a balance. The radius of a hollow core is given by

$$r = \mu b^2 / 8\pi^2 \gamma \tag{2.3}$$

Here γ is the specific surface free energy of the material, and μ the rigidity modulus. The equation has been confirmed by different experiments for micropipes in SiC [20–22].

Figure 2.13 shows an atomic force microscopic (AFM) image of a micropipe in 6H-SiC. At the central region, a circular empty tube can be identified.

Huang et al. [23, 24] have taken the direct image of the super-screw in SiC by back-reflection white-beam synchrotron topography and simulated it by tracing ray method. Based on the dislocation theory, it was considered that the distorted region around a super-screw dislocation core consists of a large number of small crystallites which are orientated by the strain field and diffract X-rays independently according to their local lattice orientations. Under these conditions, calculating the traces of the diffracted X-rays enables one to map the spots where these rays intersect the recording plate, and the contrast intensity of the direct image is then determined by the density distribution of the intersection spots. Figure 2.14 shows the back-reflection synchrotron topograph of a 6c super-screw dislocation in 6H-SiC wafer. Comparison of synchrotron topograph of Fig. 2.6a to the kinematic contrast of Fig. 2.6b for a 6c super-screw dislocation in 6H-SiC wafer indicated that hollow-core micropipes in 6H-SiC the c-axis with Burgers vectors being multiples of the lattice constant *c*.

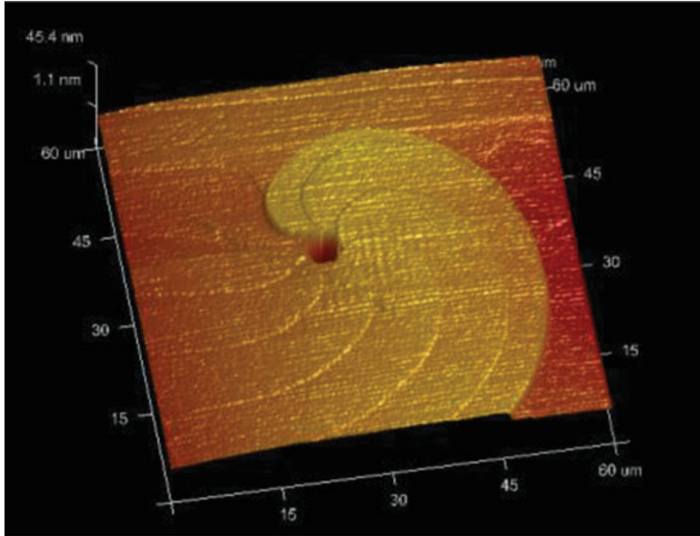


Fig. 2.13 An AFM image of a micropipe in 6H-SiC single crystal (Provided by Dr. Peng Y at Shandong University)

However, it is should be noted that Fig. 2.14a is actually the magnified image of the super-screw dislocation, and the diameter of the circular spot is the function of sample-recording film distance and Burgers vector. Figure 2.15 shows the principle for the contrast formation of a super-screw dislocation. From this figure the formation of the circular contrast feature on the film can be easily understood. From an overall viewpoint, only the different semi-apex angles of the twisted cones determine diffracted X-rays overlap in space and further determine the overall image features of the dislocation on topograph. Obviously, both the magnitude of the Burgers vector and the sample-film distance influence the topographic contrast, especially the diameter of the white-contrast region.

It was found that most of micropipes have the characteristic of mixed dislocations, i.e., their Burgers vectors have both edge and screw contents [23]. Heindl et al. investigated the structures of micropipes in SiC by using AFM and found that micropipes were hollow-core dislocations according to Frank's model but contain dislocations of mixed type [25].

The causes of micropipe generation during PVT growth of SiC include back-side bubble in seed, foreign polytype, inclusion, etc.

Kuhr et al. have observed the formation of micropipes caused by hexagonal void [26]. Figure 2.16a shows a back-reflection topograph of the area above a void, and Fig. 2.16b shows the same area below the void [26]. The area the void will pass through is outlined in white in Fig. 2.16a, and the hexagon of light and dark orientation contrast that occupies the center of Fig. 2.6b represents the trace of the

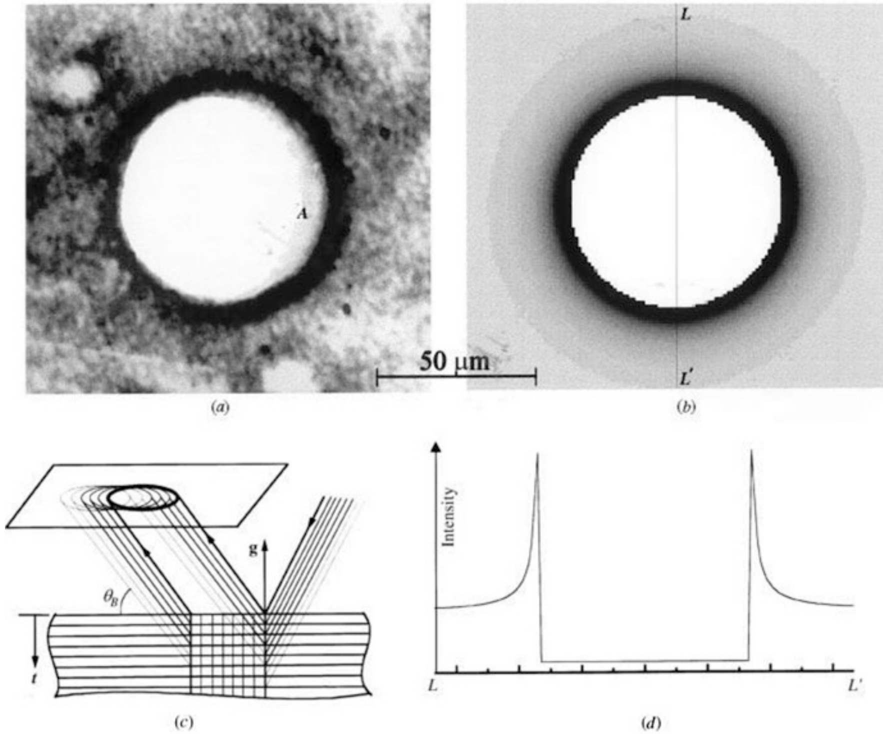


Fig. 2.14 Back-reflection synchrotron topograph of a 6c super-screw dislocation. (**a**) Synchrotron topograph of super-screw dislocation. (**b**) Kinematic contrast of a screw dislocation (Burgers vector magnitude b = 6c = 91.02 Å), simulated by tracing ray method. (**c**) Schematic representation of the displaced diffraction images associated with the deeper layers. (**d**) Radial intensity profile of the simulated image in (**c**)

void's path through the crystal during crystal growth. Large white spots on the left and lower right of the hexagon in both images are micropipes present in both wafers.

Figure 2.17 is a schematic illustration of the void and micropipe formation process. Voids are often formed at the interface between the seed crystal and crucible cap. Evaporation steps at the top of the void and growth steps on the bottom of the void provide strong evidence that SiC transport occurs within the void and that the void moves along the temperature gradient within the growing boule. Dislocations line up along the trace of the void path, and screw dislocations combine to form micropipes at the corners of the void, leaving an area directly beneath the void that is free of screw dislocations. This mechanism for micropipe formation is likely to be dominant in any crystal that contains hexagonal voids. Elimination of hexagonal voids by the use of a back-side evaporation barrier and proper seed mounting techniques was effective to reduce micropipe densities in PVT-grown SiC.

Figure 2.18 is a scanning image of a longitudinal cut 4H-SiC crystal. From this image, we can see that some foreign polytypes including 15R with yellow color and

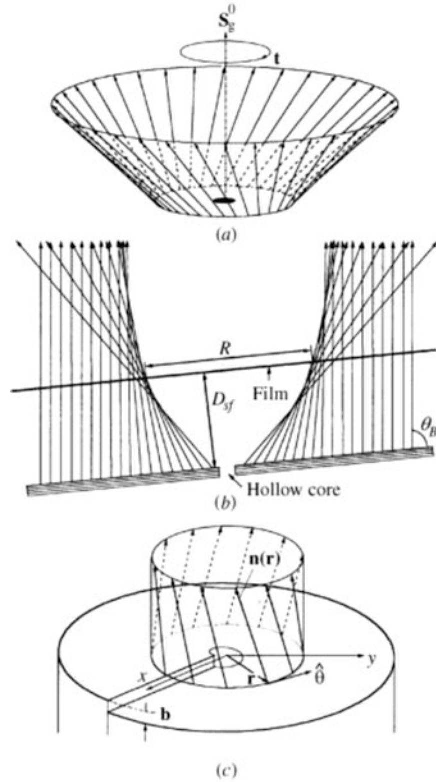


Fig. 2.15 Principle for the contrast formation of a super-screw dislocation in back-reflection synchrotron topograph. (**a**) Schematic drawing of one of the twisted cones. *t* twisting direction. (**b**) Overlap of the twisted cones in space. (**c**) Inclination of coordinate-dependent normal *n* causing the twist of diffracted X-ray

6H with green color appear in 4H-SiC crystal. As soon as the polytype phase transition occurred, a large number of micropipes were formed on the interface between the host polytype and other foreign polytype. Since the foreign polytype causes the serious mismatch in the stacking sequence as the foreign polytype nucleus meets the host polytype, the stacking mismatch and the associated large strains trigger micropipe formation. For 4H-SiC crystal growth, the temperature window for keeping polytype stability is very narrow. Any fluctuation in the temperature profile or pressure in growth cavity may cause unintentional supercooling and deviation of the C/Si ratio at growth front which further lead to the formation of foreign polytypes.

In addition, Si droplets and carbon inclusions in SiC crystals also cause the formation of micropipes.

Glass et al. [27] believed that the excess Si on the growth surface at the initial stage and the accumulation of free C after the source graphitization are the main causes for the formation of micropipes. Figure 2.19 shows an example of (a) a technological issue where a graphite particle has caused a micropipe and (b) a process instability issue where constitutional supercooling has produced Si droplets on the growth surface which have led to micropipe streaming.

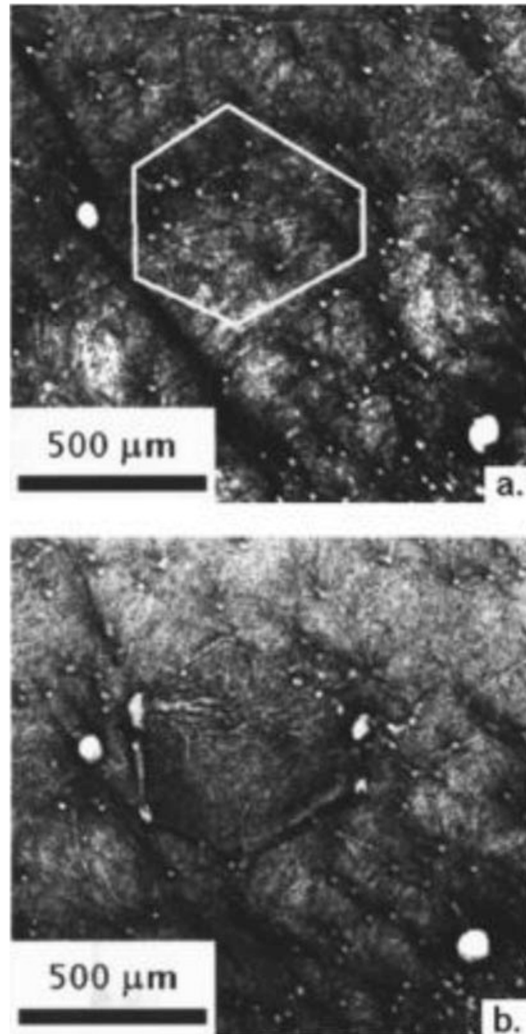


Fig. 2.16 Back-reflection X-ray topographs of the area above a void (**a**) and below a void (**b**) in 6H-SiC. The projected passage of the void has been traced in white. The screw dislocations are visible above the void in (**a**) and are not visible beneath the void in (**b**)

Origins of micropipes in SiC come from two sources. One kind of micropipes was generated from the instability growth conditions or other defects such as seed back-side void, foreign polytype, C or Si inclusion, etc. The others originated from the extension of micropipe in seed, i.e., micropipes have the heredity. For the former case, micropipes were controlled by optimization of the growth conditions such as the seed and the source temperature, the pressure of ambient gas, etc. For the latter case, many efforts have been made in the past decade to reduce or eliminate micropipes in SiC crystals.

To eliminate micropipes in SiC crystals, rhombohedral plane seeds were used to grow SiC crystals [28, 29]. Because the 4H-SiC {0 3−3 8} plane is inclined to the

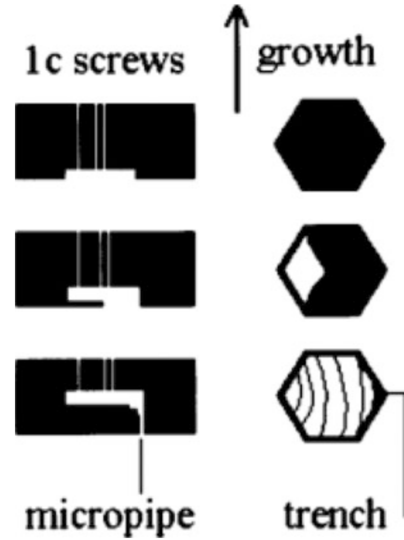


Fig. 2.17 Schematic diagram showing void formation and movement. The void begins as a cavity in the seed attachment layer, growth within the void occurs by lateral attachment and step flow, and the trench closes at the corners of the void, forming micropipes that extend beneath the void

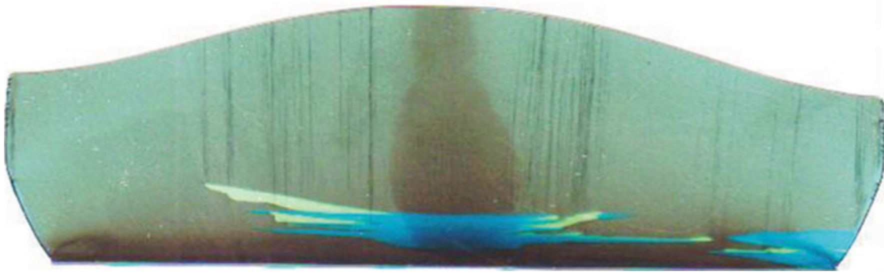


Fig. 2.18 Scanning image of a longitudinal cut 4 in. 4H-SiC crystal (Provided by Dr. Yang X L at Shandong University)

c-plane at 54.7° as shown in Fig. 2.20a and the 4H-SiC {0 3−3 8} plane is semi-equivalent to 3C-SiC {100} as shown in Fig. 2.20b, the 4H-SiC{0 3−3 8} plane has a low surface free energy and can be used as seed plane.

Shiomi et al. [28] found that a micropipe and stacking fault-free region was generated in crystals grown on the 4H-SiC {0 3−3 8} seed, as shown in Fig. 2.21. At the height of H′, there were two regions in the ingot, one was a perfect region without any micropipe and stacking fault (region A) and the other was a stacking fault region (region B). In other words, micropipe and stacking fault-free seed can be obtained by several repeating 4H-SiC crystal growth runs on {0 3−3 8} seed.

Figure 2.22a, b shows the surface morphology of the 4H-SiC {0 3−3 8} wafers after molten KOH etching. Many stripes due to the stacking faults are observed in the wafer from region B. In contrast, region A has high perfection without deep etch pits due to micropipes. It was obvious that the growth on the 4H-SiC {0 3−3 8} seed was suitable to achieve a SiC wafer without micropipes or stacking fault.

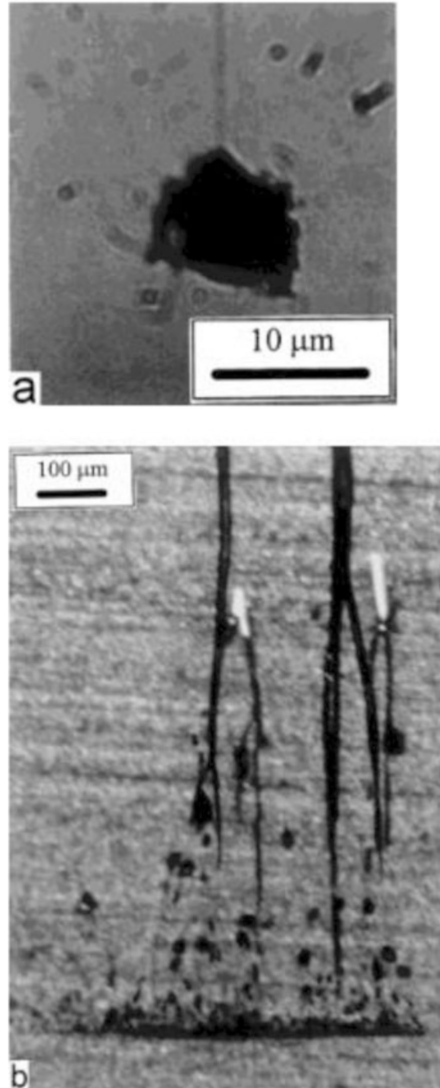


Fig. 2.19 (**a**) Graphite particle with resulting micropipe and (**b**) results of a process instability issue where constitutional supercooling has produced Si droplets on the growth surface leading to micropipe streaming

Li et al. [29] found that {0 1−1 2}, {0 1−1 3}, and {0 1−1 4} planes are the natural appearance faces for 4H-SiC. It implies that each of these planes has a low source free energy and can be used as seed face. By comparing the crystals grown on three seed faces, it was found that the quality of crystals grown on the {0 1−1 4} facet is much better than those of the crystal grown on other facets.

The above experiments confirmed that using non-*c*-face seed for SiC crystal growth is an effective method to eliminate micropipes in case of the existence of micropipes in seed. At present, micropipe-free wafers are commercially available from most suppliers.

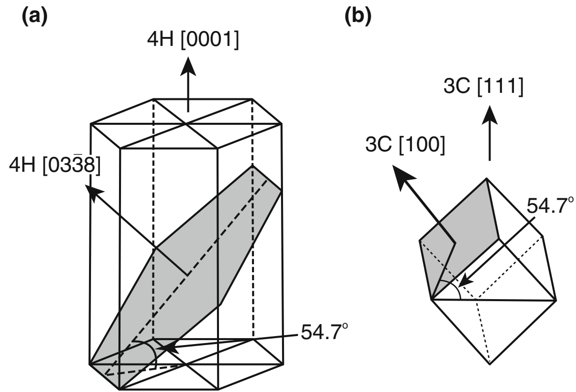


Fig. 2.20 Schematic illustration of unit cell: (**a**) 4H-SiC and (**b**) 3C-SiC

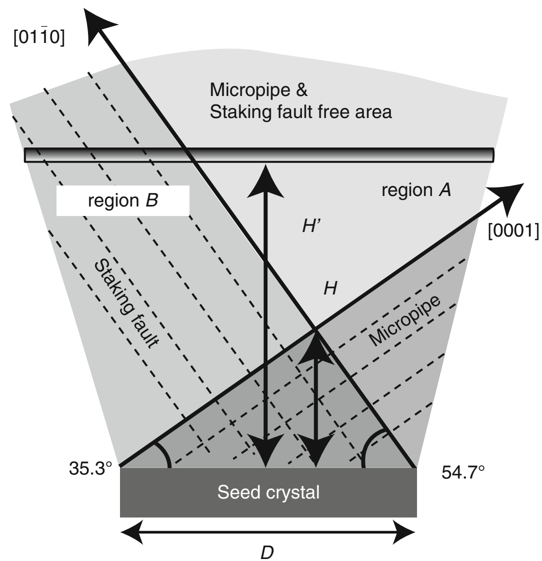


Fig. 2.21 Defect propagation on the 4H-SiC {0 3−3 8} seed

2.4.2 Foreign Polytypes

There are more than 200 polytypes for SiC materials. These polytypes have different characteristics. Because of nearly same stacking fault energy, several different polytypes such as 4H, 6H, and 15R are easily formed simultaneously in a crystal during crystal growth. Figure 2.23 shows a scanning image of a SiC wafer. In this image, we can see that 6H (green), 4H (yellow), and 15R (light yellow) coexist in a wafer. The mixing of the polytypes destabilizes growth and deteriorates the characteristic of SiC as an electronic material. Therefore, it is important to avoid the formation of foreign polytypes and keep the host polytype stability.

In the experiment, it was found that growth parameters such as the growth temperature, pressure in chamber, supersaturation, vapor-phase stoichiometry, impu-

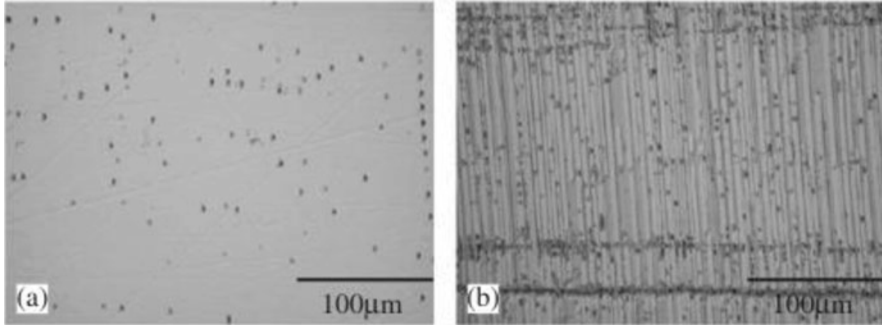


Fig. 2.22 Surface morphology of the 4H-SiC {0 3−3 8} wafer after molten KOH etching: (**a**) the micropipe and stacking fault-free area (region A) and (**b**) the micropipe-free area with stacking fault (region B)

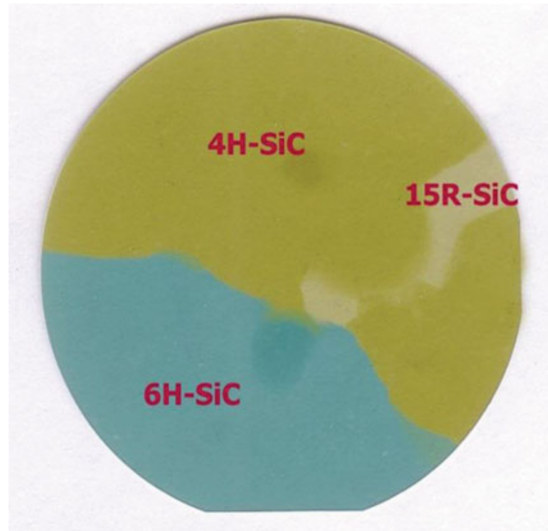


Fig. 2.23 Scanning image of a 4 in. SiC wafer in which 4H, 6H, and 15R polytypes coexist (Provided by Dr. Yang X L at Shandong University)

rities, and polarity of seed surface play important roles to influence the polytype stability. Therefore, the control of polytype is a complicated issue.

Knippenberg [30] reported empirical observation of the relative amount of individual polytype in SiC crystal growth as shown in Fig. 2.24. From this figure, we can see that the 3C is a metastable polytype, and 2H exists only at a low-temperature range. Above 2000 °C, 4H, 6H, and 15R are observed and sublimation growth can be performed. For SiC wafers to be used for electronic devices, 4H is the desired polytype. However, 4H is observed in a narrow temperature window and relative small amount. Thus, 4H-SiC crystal growth is more difficult than 6H.

Based on the classical thermodynamical analysis and crystal growth theory, Shiramomo et al. [31, 32] calculated the free energy of forming a critical nucleus in case of 2D nucleation as shown in Fig. 2.25. It can be expressed as follows:

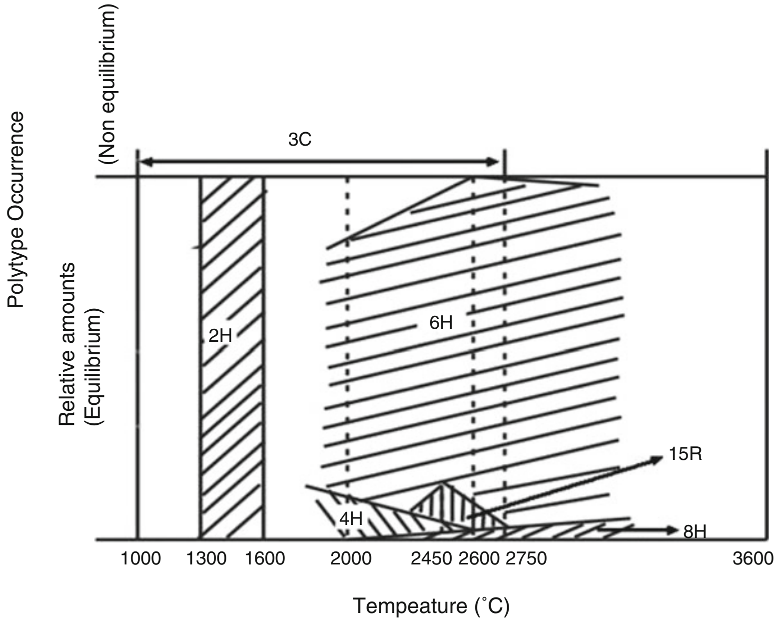
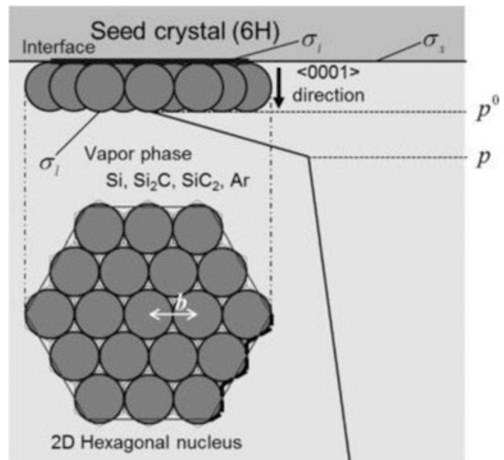


Fig. 2.24 Empirical observation of polytype occurrence in SiC crystal growth

Fig. 2.25 Model of 2D nucleation theory for SiC crystal growth



$$\Delta G_2^* = \frac{b^4 \sigma_l^2}{\Delta\mu - \left(\frac{\sqrt{3}}{2}\right) b^2 \left(\sigma_l + \sigma_i - \sigma_S\right)} \tag{2.4}$$

where b is the first neighbor distance corresponding to the in-plane lattice constant. σ_s, σ_i, and σ_l are the surface energies of the substrate surface, the

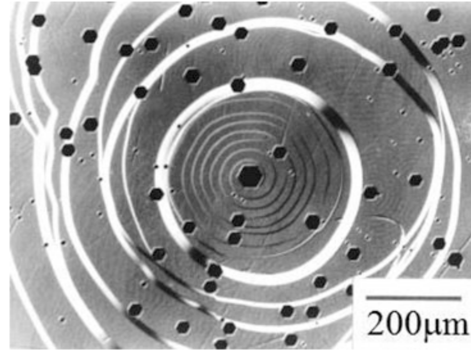


Fig. 2.26 Optical microscopic image of the growing surface of 6H-SiC after the chemical etching

layer/substrate interface, and the layer surface, respectively, as shown in Fig. 2.25. $\Delta\mu$ is the bulk chemical potential change associated with the molecular change from the vapor state to the condensed state.

To clarify which kind of polytype will be favored in the nucleation processes, the nucleation energies of 4H and 6H-SiC as a function of temperature and pressure which are the most easily generated polytypes in the sublimation method are calculated and compared. The calculation results indicated that when *c*-face was used as seed face, 4H-SiC 2D nuclei formation free energy is lower than that of 6H-SiC. This implies that the formation of 4H-SiC is more stable than that of 6H-SiC at nucleation stage in case of *c*-face seed. Additionally, the difference of nucleation energy between 4H-SiC and 6H-SiC decreased as the growth temperature increased and pressure decreased corresponding to increase of supersaturation of carbon species. This means that there is a large probability of the formation of a mixture of 4H and 6H polytypes in case of higher supersaturation, i.e., higher temperature of a seed and lower pressure in the growth chamber. In contrast, 6H-SiC is the most stable polytype for the growth on Si-face seed.

From the kinetic viewpoint, polytype replication through spiral growth around threading screw dislocations plays a critical role for the polytype stability. Figure 2.26 shows the typical surface morphology of a 6H-SiC crystal taken by optical microscope [33]. From this image, we can see that the outcrop of a threading screw dislocation on the surface provides an infinite step source. The spiral step will be kept through the whole growth procedure as long as the growth condition is stably maintained. At the step edges, the stacking information is provided, which ensures the replication of the polytype in the growth procedure.

2.4.3 Dislocations

SiC single crystal ingots and substrates contain a variety of dislocations. The Burgers vector, the extended direction, and the typical density are listed in Table 2.2.

Table 2.2 Main dislocation categories in SiC single crystals

Dislocation	Burgers vector	Extended direction	Typical density (cm^2)
Threading screw dislocation (TSD)	<0 0 0 1>	<0 0 0 1>	10^2–10^4
Threading edge dislocation (TED)	<1 1 −2 0>/3	<0 0 0 1>	10^2–10^4
Basal plane dislocation (BPD)	<1 1 −2 0>/3	In {0 0 0 1} plane	10^2–10^4

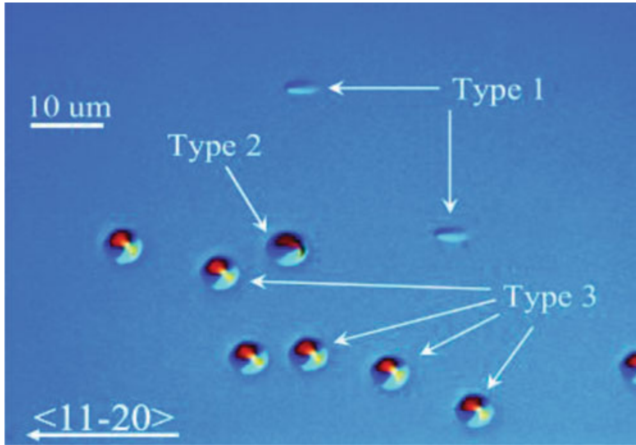


Fig. 2.27 The morphology of pits on SiC surface after oxidation

Figure 2.27 shows the typical surface morphology of SiC crystal after oxidation [34]. The oxidation pits are formed by oxidizing defects. Due to anisotropy of SiC structure, the oxidation rates of SiC are (0 0 0−1) > (1 1−2 0) > (0 0 0 1). Therefore, the oxidation pits were formed by the difference of the oxidation rate. In this figure, three kinds of pits were observed. Type 1, type 2, and type 3 correspond to basal plane dislocation, screw dislocation, and threading edge dislocation. The etch pits formed by molten KOH etching for SiC crystals have similar shapes.

As the device contains TSD, highly localized current may concentrate in the dislocation neighbor resulting in micro-plasmas. As a consequence, TSD causes the reduction of charge carrier lifetime [35]. BPDs are one of the troublesome defects in SiC materials. Stacking faults originating from the BPDs cause the increase of V_F under constant current for bipolar SiC devices, the increase of reverse-biased leakage, and the decrease of forward-biased current for unipolar SiC devices [36]. Diodes with higher TEDs densities have higher leakage current and slightly lower breakdown voltage compared to those without dislocations [37]. Among the three kinds of dislocations, the influence of TED on the performance of SiC device is relatively weak.

Since TED and BPD have the same Burgers vector, they can convert each other. To decrease the effect of dislocation on device performance, the conversions from BPD to TED are often controlled in CVD epitaxial growth by optimizing the growth parameters.

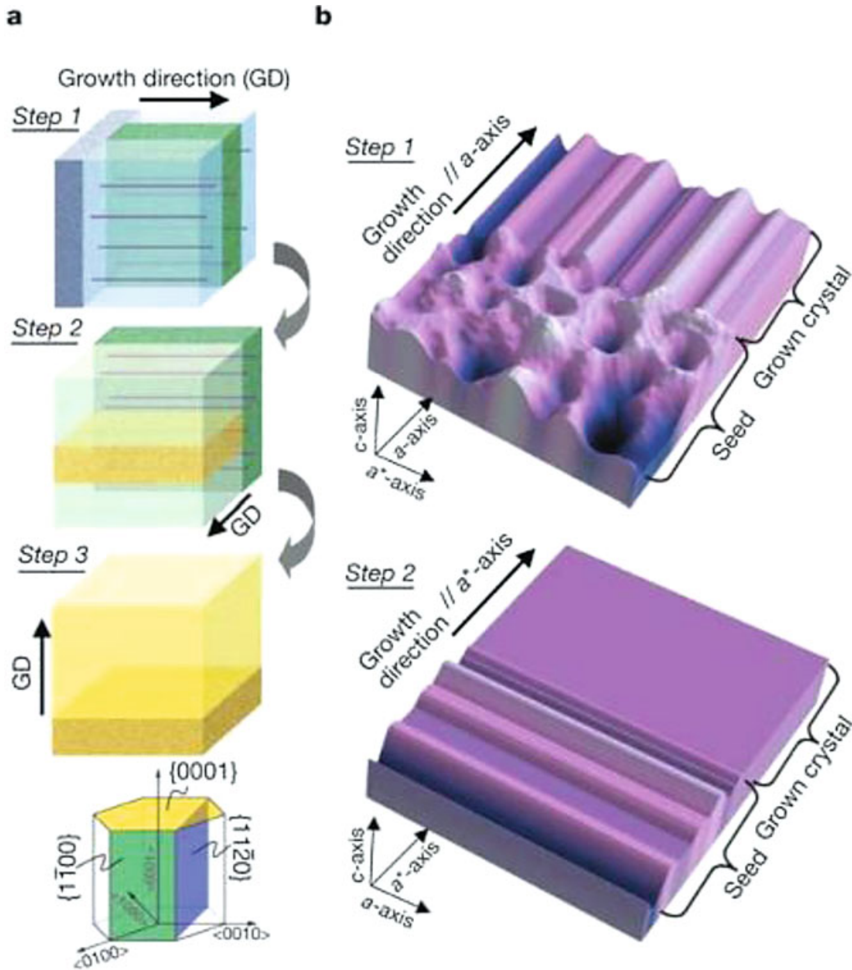


Fig. 2.28 Schematic diagram of the "repeated *a*-face" growth process. The growth sequences are as follows. Step 1: the first *a*-face growth. Step 2: the second *a*-face growth perpendicular to the first *a*-face (the seed was sliced from the first *a*-face growth crystal). Step 3: *c*-face growth with offset angle of several degrees (the seed was sliced from the second *a*-face growth crystal). (**a**) The first and second *a*-faces are {1 1−2 0} and {1−1 0 0}, respectively. (**b**) Top side view, showing {0 0 0 1} lattice plane irregularities of seed and grown crystal in steps 1 and 2. The a*-axis is perpendicular to both the *a*-axis and the *c*-axis

For conventional semiconductor materials such as Si and GaAs, dislocation-free crystals are generally grown from molten sources by means of the "necking" process. But "necking" process is not suitable for SiC crystals grown by PVT because rapid increase of crystal diameter is impossible. To reduce the dislocation density in SiC crystal, "repeated *a*-face" method was proposed by Nakamura et al. for the ultrahigh-quality SiC single crystal growth [38]. Figure 2.28 shows the "repeated *a*-face" growth process.

The process to eliminate dislocations is described as follows. Step 1: *a*-face ({1 1−2 0} or {1−1 0 0}) growth along the *a*-axis (<1 1 −2 0> or <1 −1 0 0>) direction, using a seed sliced from a *c*-face growth ingot. Step N ($N = 2, 3, 4, \ldots$): *a*-face ({1 −1 0 0} or {1 1 −2 0}) growth along the *a*-axis (<1 −1 0 0> or <1 1 −2 0>) direction, using a seed sliced from the *a*-face growth ingot of the previous step (step $N - 1$)—the seed surface orientation is perpendicular to both the previous step's growth and <0 0 0 1> directions. Step $N + 1$: *c*-face growth, using a seed sliced from the *a*-face growth ingot of the previous step (step N)—the seed surface is {0001} face, with several degrees off-axis toward the perpendicular to both the previous step's growth and <0 0 0 1> directions.

The principle for the reduction of the dislocation density is described as follows. In step 1, an *a*-face seed with a high density of dislocations, which are inherited from the crude *c*-axis SiC crystal, was used. In step 2, most of the dislocations are not exposed to the surface of the second seed, because they exit perpendicular to the first *a*-face growth direction, i.e., parallel to the second seed surface. In other words, the second *a*-face growth crystal inherits fewer dislocations.

It was found that the dislocation density could be reduced by increasing the repeating N counts. Etching experiment indicated that averaged etch pit density (EPD) in 4H-SiC decreased exponentially with increase in the repeat count of *a*-face growth. The average EPD and micropipe densities of a 20 mm diameter substrate, taken from the crystal grown on RAF seed with *a*-face growth performed three times, were 75 cm^{-2} and 0 cm^{-2}, respectively. The EPD value is lower by three orders of magnitude than that of conventional-grade SiC substrates.

Finally, the stacking fault was eliminated by the last step *c*-face growth because the stacking faults and partial dislocations are inherited only perpendicular to the *c*-axis. X-ray topographic observation shows that the stacking faults and partial dislocations are eliminated perfectly by the *c*-face growth since the stacking faults and partials lie on the {0 0 0 1} plane.

Figure 2.29 shows the quality assessment for the repeated *a*-face growth crystal by synchrotron topography. From Fig. 2.29a, we can see that crystal quality of the RAF substrate is very homogeneous, and there are very few macroscopic defects and dislocation. The long-range lattice warp is very small with the curvature radius of the lattice of about 800 m. In contrast, the conventional-grade substrate has many macroscopic defects and dislocation networks as shown in Fig. 2.29b.

Therefore, RAF is an effective method to eliminate dislocations and other defects in SiC single crystals.

2.5 Control of Electrical Characters of SiC Crystals Grown by Sublimation Growth

For the fabrication of vertical devices, low-resistivity wafers are needed to minimize the series resistance, while high-resistivity wafers are desired for the fabrication of lateral high-frequency devices, to reduce the parasitic impedance. In SiC

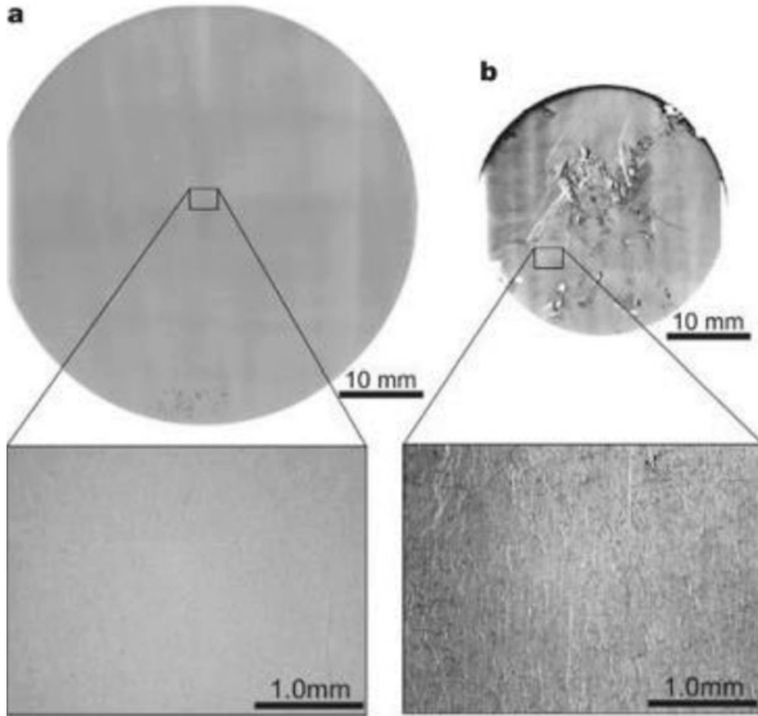


Fig. 2.29 Synchrotron monochromatic beam X-ray topographs. 4H-SiC (0001) 8° off-axis substrate, 2.0 in. in diameter, manufactured by the RAF process (**a**) and a 1.2 in. diameter specimen manufactured by the conventional process (only *c*-face growth (**b**). Averaged EPD and micropipe densities of the RAF growth crystal were about 250 cm^{-2} and 0 cm^{-2}, respectively, and those of crystal grown by the conventional method were about 3×10^4 cm^{-2} and 30 cm^{-2}, respectively. Magnified images are shown below. Dislocation networks are shown in the magnified image of (**b**)

single crystal, N and Al are generally the dopants for n-type and p-type boules, respectively. Semi-insulating characters of SiC crystals were realized by introducing deep levels compensating all shallow donors or acceptors.

2.5.1 n-Type Doping

In the procedure of SiC sublimation growth, nitrogen doping is generally conducted by introducing nitrogen gas into the growth chamber. In this case, carrier gases include Ar and N_2 with a suitable proportion. The nitrogen concentration in grown SiC crystal is approximately proportional to the square root of the nitrogen partial pressure during crystal growth and independent of growth rate. This implies that nitrogen incorporation is determined by the equilibrium between nitrogen in the gas phase and nitrogen adsorbed on the growing surface [39].

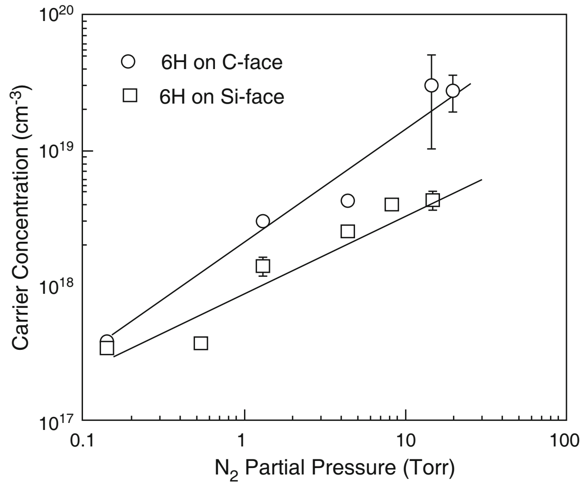


Fig. 2.30 N_2 partial pressure dependence of the carrier concentration in 6H-SiC grown on the (0 0 0 1) Si and the (0 0 0−1) *c*-faces

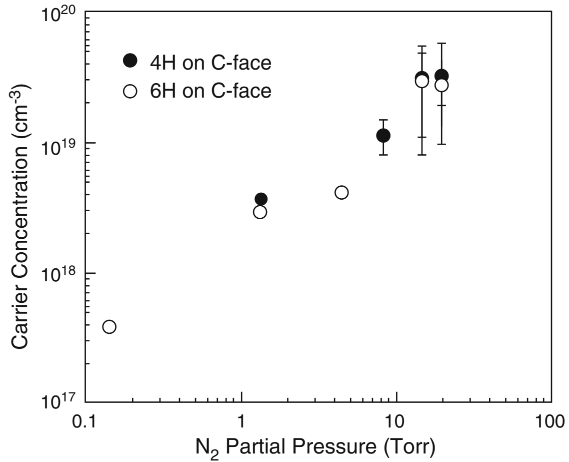


Fig. 2.31 N_2 partial pressure dependence of the carrier concentration in 4H and 6H-SiC grown on the *c*-face

Figure 2.30 shows the N_2 partial pressure dependence of the carrier concentration in 6H-SiC crystals grown on the (0 0 0−1) C and the (0 0 0 1) Si-faces [40]. The carrier concentration increased as the nitrogen partial pressure increased for both crystals. The crystals grown on the *c*-face always had higher carrier concentrations than those grown on the Si-face, and the difference became larger at higher carrier concentrations. The carrier concentration difference originated mainly from the large compensation of the impurity acceptor atoms in the low carrier concentration regime.

Figure 2.31 shows the N_2 partial pressure dependence of the carrier concentration in both 4H and 6H-SiC crystals grown on the *c*-face. Both crystals exhibited the similar concentration variation trend although 6H-SiC has larger nitrogen donor ionization.

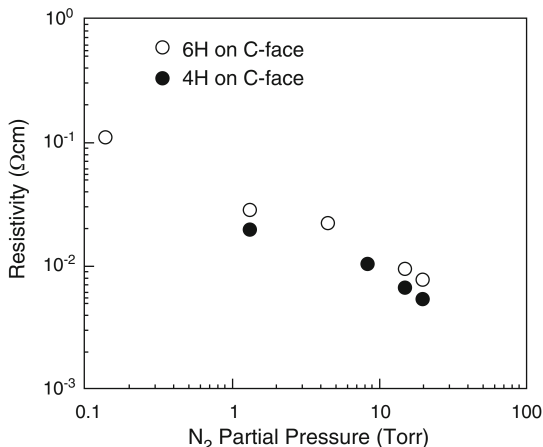


Fig. 2.32 N_2 partial pressure dependence of the resistivities of 4H and 6H-SiC crystals grown on the *c*-face

Figure 2.32 shows the resistivities of the 6H and 4H-SiC crystals as a function of the nitrogen partial pressure. The 4H-SiC crystal always exhibited lower resistivities at the same carrier concentration because of its higher electron mobility. At a nitrogen partial pressure of 20 Torr corresponding to the nitrogen concentration of 10^{20} cm^{-3}, bulk resistivities 7.6×10^{-3} Ω cm for 6H-SiC and 5.3×10^{-3} Ω cm for 4H-SiC were obtained. However, the resistivities of n-type 4H-SiC for the electronic devices were in the range of 0.01–0.03 Ω cm. Therefore, the electron mobility is rather low for 4H-SiC in the above experiment. In n-type SiC wafers, there are several kinds of deep levels or electron traps at a relatively high concentration of 10^{14}–10^{15} [41, 42].

It has been found that stacking faults were formed in highly nitrogen-doped 4H-SiC subjected to an oxidized or annealed in Ar at high temperature [43, 44]. When the nitrogen concentration exceeded 1×10^9 cm^{-3}, the SF occurrence became distinct. Therefore, in order to decrease the resistivity of SiC, it is necessary to grow lightly nitrogen-doped 4H-SiC crystal and decrease the deep level impurity concentrations to very low level.

Recently, Kato et al. have grown low-resistivity n-type 4H-SiC crystals by sublimation using Al-N co-doping technique [45]. Figure 2.33 shows the schematic illustration of the Al-N co-doping 4H-SiC crystal growth. The furnace has two RF coils for heating SiC and Al source, respectively. N and Al doping levels were controlled in the range of 5×10^{18} cm^{-3} to 1×10^{20} cm^{-3} during growth.

It was found that the stacking faults (SFs) were suppressed in the n-type 4H-SiC grown by the co-doping technique. Figure 2.34 shows the etching morphologies of longitudinal cut SiC crystals after molten KOH etching treatment. In Fig. 2.34a, the etched surface shows morphology with line-shaped etch pits caused by a lot of SFs generated due to the high *N* doping of 3×10^{19} cm^{-3}. In contrast, the high N-Al co-doped crystal does not show any sign of SF generation in spite of the high *N* concentration of 8.8×10^{19} cm^{-3} as shown in Fig. 2.34b. Furthermore, the co-

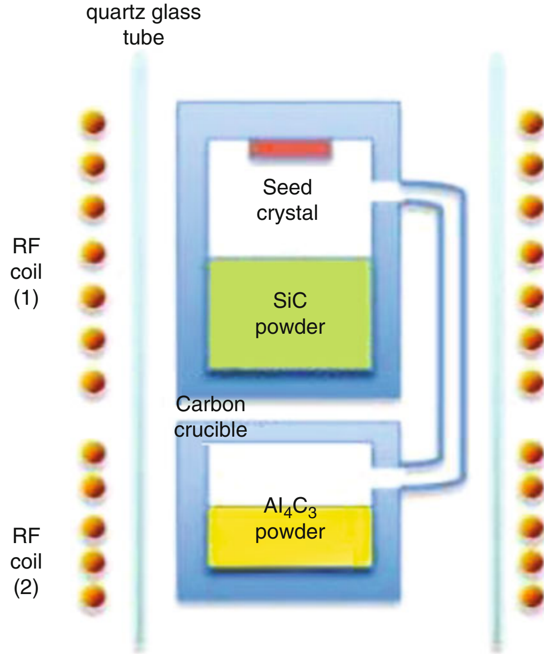


Fig. 2.33 Schematic illustration of Al-N co-doping 4H-SiC crystal growth

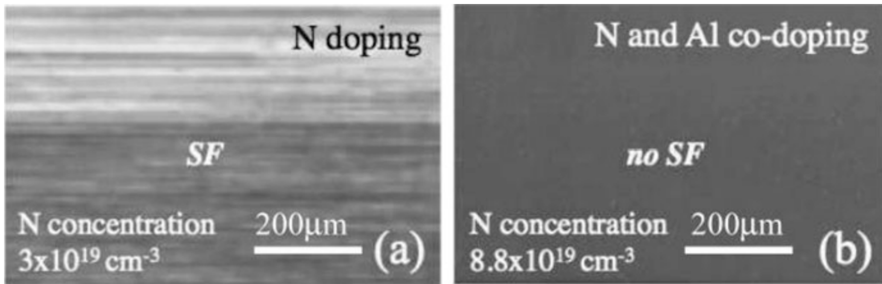


Fig. 2.34 The etching morphologies of longitudinal cut SiC crystals after molten KOH etching treatment. (**a**) Conventional sublimation-grown SiC with *N* concentration of 3×10^{19} cm^{-3}. (**b**) Co-doping-grown SiC with *N* concentration of 8.8×10^{19} cm^{-3} and Al concentration of 4.2×10^{19} cm^{-3}, respectively

doped 4H-SiC crystals show higher activation ratio of donor compared with the conventional nitrogen-doped crystals. When N and Al concentrations for co-doped 4H-SiC are 8.8×10^{19} cm^{-3} and 4.2×10^{19} cm^{-3}, respectively, the resistivity reaches 8.5 mΩ cm.

Therefore, low resistivity for n-type 4H-SiC could be achieved by N-Al co-doping technique. The SFs were suppressed until higher N concentration of 8.8×10^{19} cm^{-3} in the co-doped crystal. At the same time, the co-doped crystals showed higher activation ratio of donor compared with the conventional n-type 4H-SiC crystals.

2.5.2 p-Type Doping

For high-power SiC device application, substrates with low resistivity are required to reduce the unnecessary resistance of the devices. Especially for the fabrication of n-channel IGBTs, showing high performance compared to p-channel IGTs, p-type 4H-SiC substrates with low resistivity are required. Aluminum is often used as p-type dopant in SiC crystal. In general, aluminum doping is realized by adding aluminum or aluminum-containing compound into the SiC source. Aluminum doping is much more difficult than nitrogen doping during SiC crystal growth because severe depletion of the aluminum source occurs in the procedure of crystal growth at high temperature [46]. The Al concentration in crystal is almost proportional to aluminum vapor pressure in the growth chamber.

To realize the effective aluminum doping in 4H-SiC single crystals, Hens et al. have grown p-type SiC by using modified physical vapor transport (M-PVT) technique [47]. Figure 2.35 shows the schematic illustration of M-PVT SiC crystal growth method. In the left configuration of this figure, the Al source is located in the reservoir beneath crucible bottom, and the gas was flowed through the additional pipe only in small amount. If the additional flux is ten times larger than the conventional PVT, crystal growth will be disturbed in the center zone of the seed

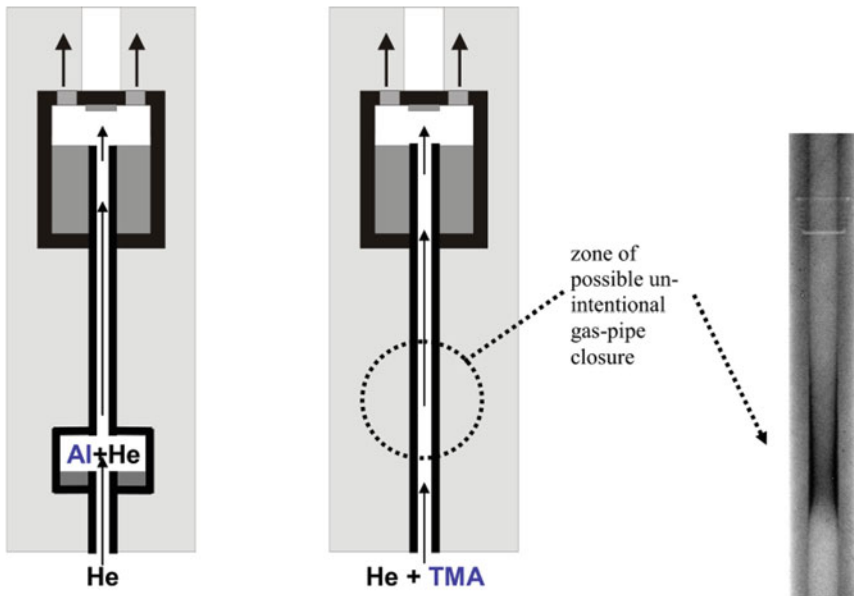


Fig. 2.35 Aluminum p-type doping SiC crystal growth by M-PVT technique. (Left) Regular setup with heated aluminum-containing reservoir. (Center) New setup with TMA source. (Right) X-ray image of gas pipe visible zone of unintentional deposition of carbon/graphite and related aluminum compounds due to decomposition of TMA

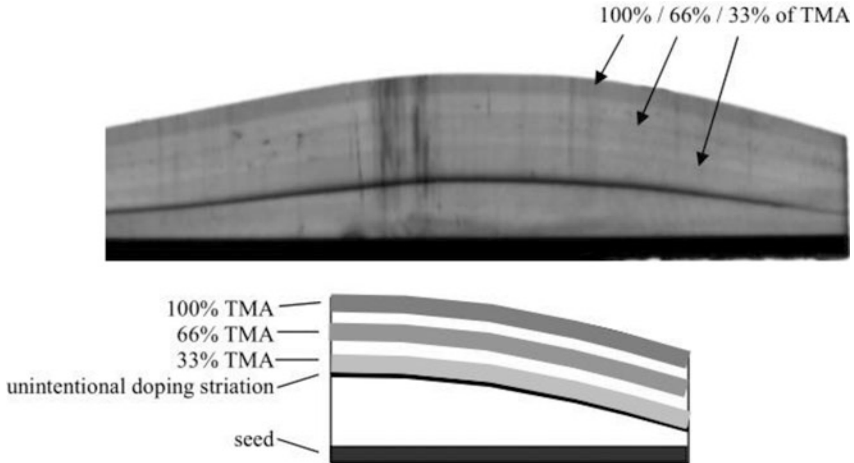


Fig. 2.36 Top: scanning image of longitudinal cut 6H-SiC crystal by M-PVT using TMA as Al source. Al doping concentration is indicated by the gray-level contrast. Bottom: schematic illustration of longitudinal cut of the highlighted doping stripes

crystal. If the additional flux is ten times smaller than the conventional PVT, the pipe will be closed by SiC deposition in the upper pipe zone at the entrance to the growth cell. Therefore, the use of solid Al source has the following disadvantages: (1) the additional pipe is easily blocked by the reverse transport of the SiC vapor species from the hot powder to the colder reservoir. (2) When the additional gas was flowed into the growth cell, it caused the temperature elevating of the central part of the gas room. It further possibly leads to the seed sublimation since the additional gas prevents the Si and C species from depositing on the seed. (3) The Al doping concentration is not easily controlled.

To improve the Al doping homogeneity, M-PVT p-type SiC crystal growth using tri-methyl-aluminum (TMA) as Al source is proposed as shown in the central configuration of Fig. 2.35. In this configuration, the feeding of TMA allows a more precise control of the Al flux into the growth cell. In addition, the use of high purity TMA can reduce the unintentional doping concentration. A major challenge during feeding of TMA into the hot growth cell is the pipe aperture narrowing or even blockade by graphite and related aluminum compound deposition on the walls after long run as shown in the right of Fig. 2.35.

Figure 2.36 showsan optical transmission image of a longitudinal cut of a 6H-SiC crystal grown on *c*-face 6H-SiC seed by M-PVT using TMA as Al source. The total gas flux was kept constant, and the relative values of TMA were varied in the following sequence: 0%, 33%, 0%, 66%, 0%, and 100%. The dark stripes correspond to 100%, 66%, and 33% of TMA, respectively. The black stripe is related to an unintentional high TMA flux when turning on the dopant supply for the first time. It was found that different Al incorporation levels from the low to

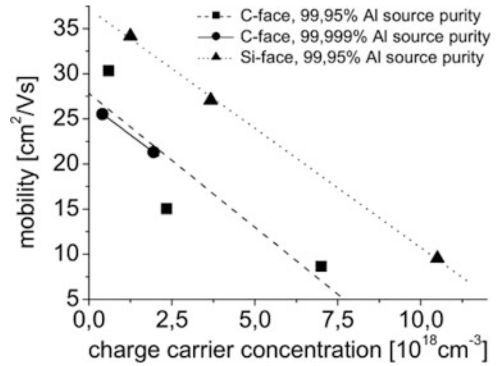


Fig. 2.37 Charge carrier mobility versus charge carrier concentration for a number of 6H-SiC crystals grown on *c*-face and Si-face SiC seeds

Table 2.3 Result of SIMS, Raman spectroscopy, and resistivity measurement of various crystals grown with Al-N co-doping

Growth no.	Al concentration (cm^{-3})	N concentration (cm^{-3})	Al/N	Dominant polytype	Carrier concentration	Resistivity (mΩ cm)
1	1.8×10^{-20}	1.5×10^{-20}	1.2	4H	3.0×10^{19}	86
2	3.1×10^{-20}	2.3×10^{-20}	1.3	4H	4.0×10^{19}	88
3	2.6×10^{-20}	1.8×10^{-20}	1.4	4H	4.0×10^{19}	97
4	1.5×10^{-20}	1.3×10^{-20}	1.5	6H	–	68

mid-10^{20} cm^{-3} could be achieved in SiC crystals by M-PVT using TMA as the Al source.

From a kinetic viewpoint, *c*-face is unfavorable for aluminum incorporation and favorable for nitrogen incorporation because the Al and N occupy the Si-lattice site and C-lattice site, respectively. The background N often causes the compensation of acceptors in p-type SiC. Even if the compensation is only in the range of 3–5%, it leads to a pronounced reduction of charge carrier mobility and conductivity. Figure 2.37 shows the influence of seed polarity on the compensation of acceptor. In case of Si-face seed, unintentional acceptor compensation of aluminum is much suppressed compared to the use of Si-face seed. From this figure, we can see clearly that the suppression of compensation causes the increase of the charge carrier mobility and further the conductivity increase by more than factor 2.

Recently, low-resistivity p-type 4H-SiC crystals were grown by sublimation using aluminum and nitrogen co-doping [48]. The crystal growth was performed by a two-zone heating furnace, which has two RF coils for heating high purity SiC source material and Al_4C_3. Table 2.3 shows representative results of SIMS, Raman spectroscopy, and resistivity measurement for the grown crystal. The lowest resistivities obtained for 4H and 6H-SiC were 86 mΩ cm and 68 mΩ cm, respectively.

The relation of Al and N concentrations of grown crystals is plotted in Fig. 2.38. It was found that Al/N = 1:1 line acted as a border of n-type and p-type. When the Al/N is larger than 1, the crystal exhibits the p-type electrical characteristics and vice versa.

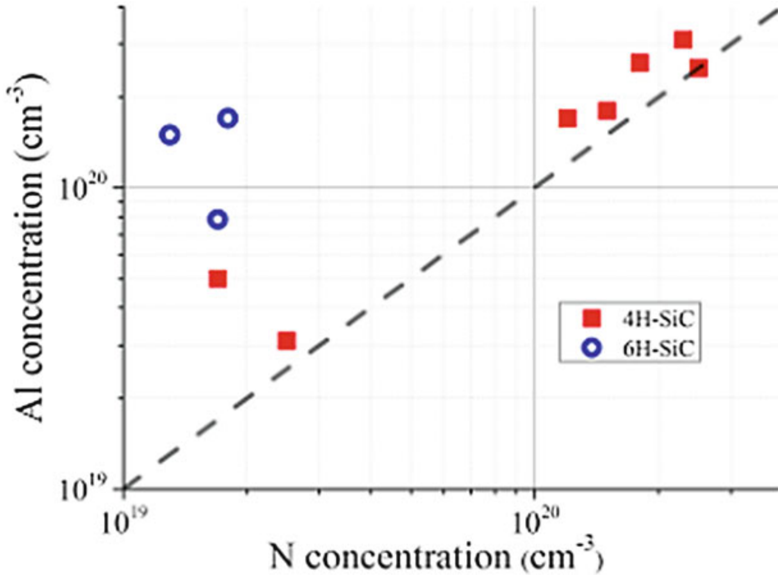


Fig. 2.38 Al and N concentrations measured by SIMS. The guide line show the Al/N = 1:1 line, as a border of n-type and p-type. Notation of 4H and 6H indicates the dominant polytypes of grown crystals

2.5.3 Semi-insulating

High-resistivity wafers are generally used fabrication of SiC- or GaN-based high-frequency devices to minimize the parasitic capacitances between the terminals, including the ground. Because it is very difficult to reduce the background dopant density below 10^{10} cm^{-3} by purification processes, compensation of dopants is often used to decrease the density of free carriers in the bands. In SiC, vanadium was the first element used as a compensation center to create semi-insulating wafers. Vanadium is an amphoteric impurity in SiC. It acts as an acceptor-like trap in n-type SiC and a donor-like trap in p-type SiC.

Vanadium deep levels in SiC have been identified by Schneider et al. [49]. Two deep levels are formed by vanadium in 6H-SiC: a V^{3+}/V^{4+} acceptor level about 0.8 eV below the conduction band and a V^{4+}/V^{5+} donor level approximately in the middle of the bandgap, i.e., about 1.5 eV.

Assuming that the donors (mainly nitrogen), acceptors (aluminum, boron, etc.), and vanadium are present simultaneously in the SiC crystals in electrically active concentrations N_D, N_A, and N_v, respectively, four compensation regimes can appear in 6H-SiC.

1. $N_V > N_D - N_A > 0$, vanadium compensates shallow donors which may be themselves partially compensated by acceptors.

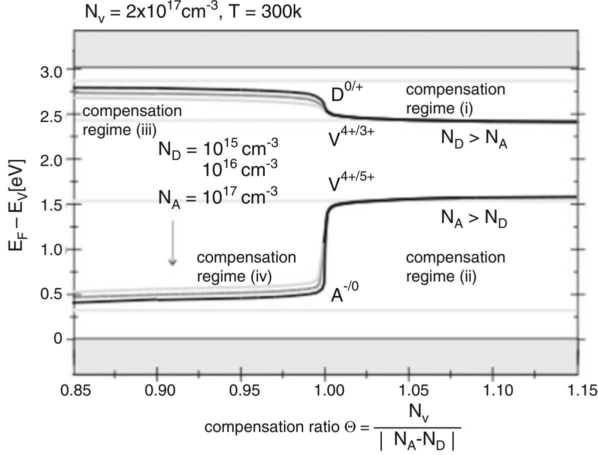


Fig. 2.39 Dependence of the Fermi level on the compensation ratio Θ for different shallow impurity concentrations N_A and N_D in vanadium-doped 6H-SiC

2. $N_V > N_A - N_D > 0$, vanadium compensates shallow acceptors which may be themselves partially compensated by donors.
3. $N_D > N_V + N_A$, domination of shallow donors lead to n-type conducting behavior, $\Theta < 1$.
4. $N_A > N_V + N_D$, domination of shallow acceptors leads to p-type conducting behavior, $\Theta < 1$.

Figure 2.39 shows the position of the Fermi level calculated from the charge carrier neutrality equation

$$n + N_A^- + N_{V(3+)} = p + N_D^+ N_{V(5+)} \tag{2.5}$$

as a function of $\Theta = N_V/|N_D - N_A|$ for different $N_D - N_A$ [50]. As long as vanadium compensates all other impurities as in regimes (1) and (2), semi-insulating SiC will be obtained. Another key condition for the preparation of semi-insulating SiC is that N_V cannot exceed the vanadium solubility limit.

V-doped semi-insulating 6H-SiC bulk single crystals have been grown by sublimation method from different research group. Bickermann et al. [50] found that if vanadium is added as a solid source to the SiC powder, it quickly exhausts during growth. Figure 2.40 is a scanning image of a longitudinal cut of a crystal grown with a vanadium content of 0.32 wt % in the source material. We can see that at the first stage, serious vanadium precipitation occurred. Following the crystal growth preceding, the vanadium concentration was gradually decreased, and the vanadium precipitation particles became smaller in size, but precipitation density does not change significantly. From GDMS measurements at the transition region

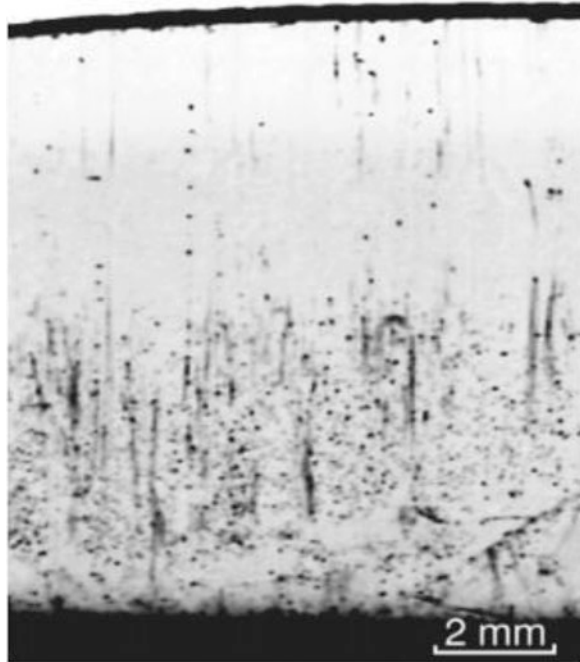


Fig. 2.40 The scanning image of a longitudinal cut 6H-SiC with vanadium doping. Semi-insulating 6H-SiC was grown by sublimation method using the solid vanadium source

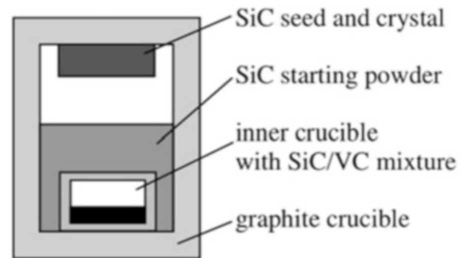


Fig. 2.41 Schematic illustration of the inner crucible located inside the growth container

from precipitated to non-precipitated areas, the vanadium solubility in SiC was confirmed to be about 4×10^{17} cm^{-3}.

In order to increase the semi-insulating yield of the grown crystals and avoid vanadium precipitation or depletion, vanadium concentrations in SiC crystals have to be lower than the solubility but higher than N_D in the whole crystal volume. To realize the vanadium uniform doping in SiC crystal, Bickermann et al. [50] used an inner crucible in which the SiC/VC mixture was filled as shown in Fig. 2.41. In this case, vanadium evaporation rate decreases as the container gets "sealed" in the early stages of growth due to SiC sublimation. A dense SiC/VC mixture sublimes at the top of the inner crucible and acts as an infinite vanadium source with nearly constant supply during SiC crystal growth. Therefore, semi-insulating, precipitate-free SiC crystals can be grown using the inner container doping method. Crystal volume yield is about 80%. The predominantly nitrogen-doped layer forming at the

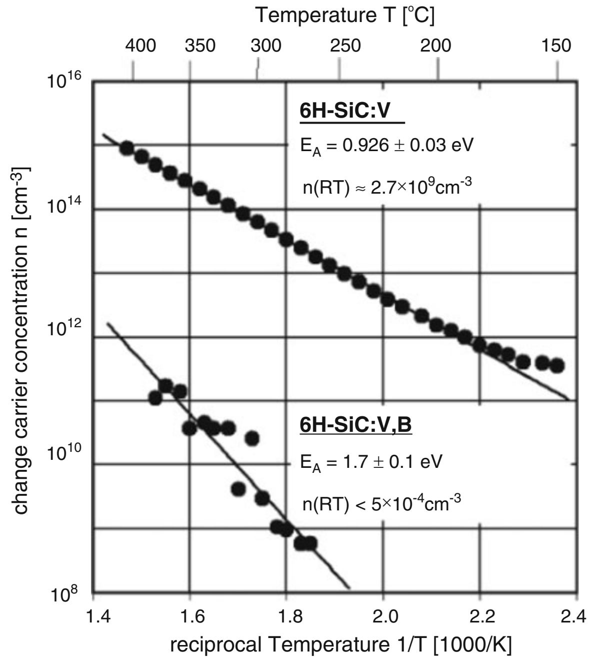


Fig. 2.42 Hall effect measurements of a V-doped and V-B co-doped 6H-SiC crystals

early stages of growth expanded to about 20% of the crystal volume. The vanadium concentration is about 5×10^{17} cm^{-3} near the seed and 2×10^{17} cm^{-3} at the end of growth, respectively. It implies that vanadium uniform doping has been realized. Similarly, V-B co-doping semi-insulating SiC crystals can be grown by using the inner container.

Figure 2.42 shows the Hall effect measurements of a V-doped and a V-B co-doped 6H-SiC crystals. For the V-doped crystal, the thermal activation energies are as high as 926 meV. It confirms that the vanadium compensates all shallow nitrogen donors. Extrapolation to room temperature gives the specific resistivities between 2×10^9 and 6×10^{10} Ω cm.

To overcome the difficulty in vanadium doping, semiconducting character could be also achieved by the use of intrinsic point defects. Therefore, high purity semi-insulating (HPSI) SiC was expected. The development of a semi-insulating SiC material requires two key components. First, a deep electronic level is necessary to trap either electrons or holes and to supply a large activation barrier to their subsequent release. Second, shallow levels are required to supply compensation to the deep electronic level so that the Fermi level can be pinned to the deep electronic level. In high purity SiC, the shallow electronic levels are mainly the boron and nitrogen. The deep electronic levels are vacancies.

The main difficulty for the growth of high purity SiC is the control of impurity incorporation in the crystal during growth. The metallic impurities can be easily eliminated by the high-temperature halogenation. But the nitrogen and boron are

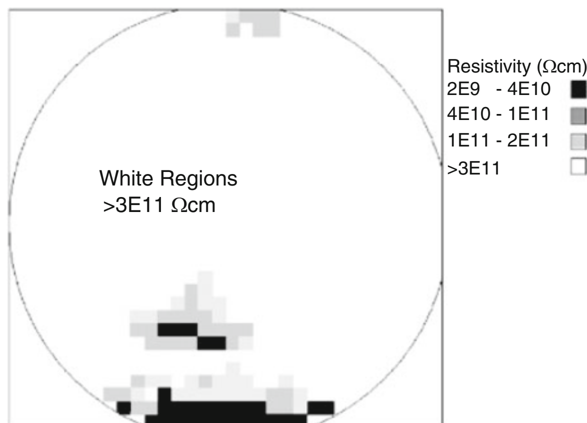


Fig. 2.43 High-resolution resistivity map of a 2″ diameter high purity semi-insulating 4H-SiC

difficult to reduce. Nitrogen comes from the absorbed air of the graphite parts and insulation. Boron is the accompanying product of the graphite. Therefore, the purification of graphite parts, insulation, and source is the critical technology for the growth of high purity SiC crystal. At early research work, Augustine et al. attempted to grow high purity SiC single crystals using sublimation method [51]. Unfortunately, the high purity SiC crystal did not exhibit semi-insulating electrical character due to the impurity contamination. Glow discharge mass spectroscopy (GDMS) measurements reveal that the metallic impurity concentrations are lower than the 1×10^{15} cm^{-3}, while the boron concentration is as high as 6.0×10^{16} cm^{-3}. Crystals exhibit resistivities in the 10^{3} Ω cm range and are p-type due to residual high concentration of boron. It failed to obtain the high purity semi-insulating SiC crystals.

Jenny et al. [52, 53] reported the successful growth of high purity semiconducting 4H-SiC crystals by sublimation method. High-resolution resistivity map of a 2 in. diameter 4H-SiC was shown in Fig. 2.43. The entire wafer is semi-insulating with resistivity greater than 2×10^{9} Ω cm. More than 80% of the wafer area has a resistivity $>3 \times 10^{11}$ Ω cm.

Secondary ion mass spectroscopy detection for the HPSI indicated that the only elements were nitrogen (2×10^{16} cm^{-3}) and boron (7×10^{15} cm^{-3}), and the concentrations of all other elements were below the SIMS detection limits or below the instrument background.

For examining electronic levels in semiconductors, Hall effect is an effect tool. Using the technique, we can determine several important electronic parameters, including the activation energy of the electronic level, the concentration of the principal defect, and the total net compensation. For the HPSI samples, the Hall effect is not suitable due to the extremely low mobility of the sample. Figure 2.44 shows the temperature-dependent resistivities of five HPSI samples. From the resistivity versus temperature, the obtained activation energies are 0.9, 1.1, 1.2,

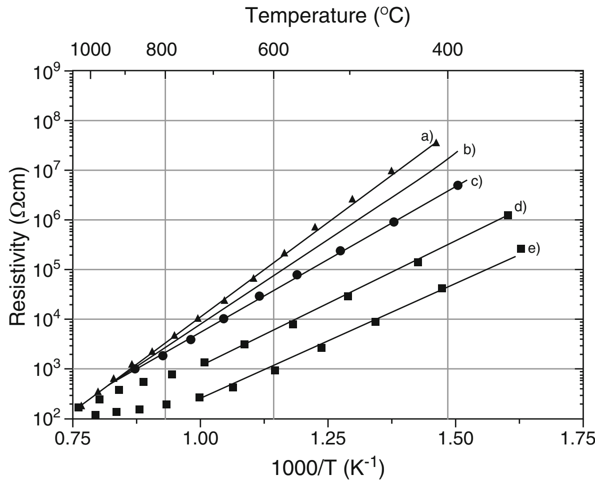


Fig. 2.44 Temperature-dependent resistivities for five HPSI samples whose activation energies are (**a**) 1.53 eV, (**b**) 1.33 eV, (**c**) 1.19 eV, (**d**) 1.06 eV, and (**e**) 0.90 eV

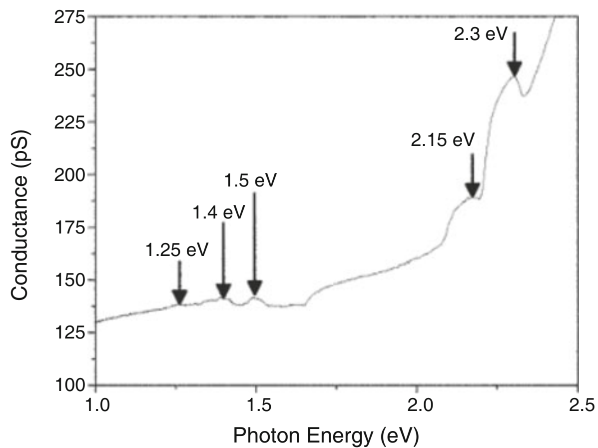


Fig. 2.45 Admittance versus photon energy plot that reveals the presence of five distinct energy levels

1.35, and 1.5 eV. Therefore, several defects are responsible for the semi-insulating character in the HPSI samples.

To further confirm the existence of multiple deep levels in HPSI, optical admittance spectroscopy (OAS) was used to measure the admittance of HPSI sample.

Figure 2.45 shows the OAS data of HPSI samples. It reveals that the activation energies for several deep levels are 1.25, 1.4, 1.5, 2.15, and 2.3 eV.

For activation energies greater than half of the bandgap, the bandgap energy (3.2 eV for 4H-SiC) has to be subtracted so that the data can be compared with the data obtained by other characterization techniques. Therefore, the actual activation

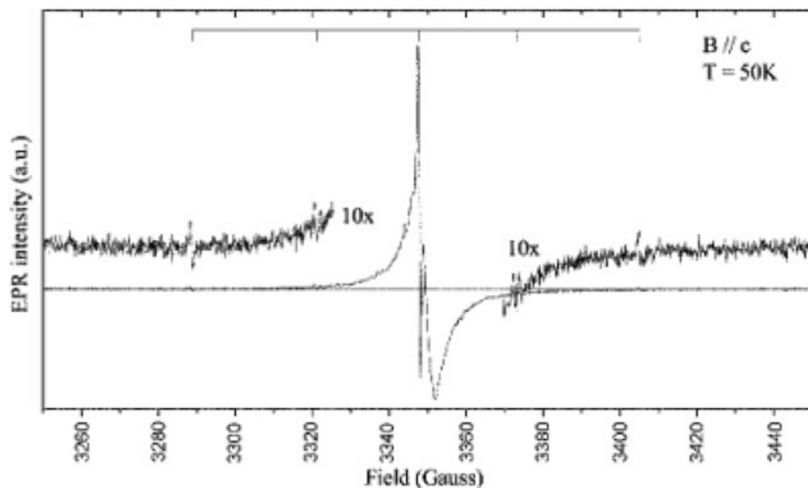


Fig. 2.46 The EPR spectrum of a 4H-SiC HPSI sample whose Fermi level was pinned to the 1.5 eV level and exhibits the carbon vacancy

energies are 0.9, 1.05, 1.25, 1.4, and 1.5 eV after the bandgap energy subtraction, which are very close to those obtained by temperature-dependent resistivity. The above two-group data proves that the source of the deep levels is probably to be intrinsic in nature.

Figure 2.46 is an electron paramagnetic resonance (EPR) spectrum of a sample exhibiting the activation energy of 1.5 eV. The large sharp peak with two hyperfine doublets is the main feature in the spectrum. It was identified as a carbon vacancy. The fact that defect is present in SI material suggests that it is electrically active and is responsible for at least one of the defects observed in the temperature-dependent resistivity measurements.

In addition, the SI material has a high thermal stability. After the HPSI wafers were subjected to 1650 °C annealing, for 90 min, no degradation in the SI character was observed in the annealed HPSI wafer. SI character preservation makes the HPSI wafers suitable for the application as ideal substrate for microwave devices.

2.6 Processing of Large-Diameter SiC Wafers

The processing from ingot to wafer for SiC is same as that for other semiconductors. SiC single crystal ingots are generally grown on {0 0 0 1} seed. The typical ingots are cylindrical in shape with a length of 20–30 mm. The crystallographic orientations of the ingots such as <0 0 0 1>, <1 1 −2 0>, and <1 0 −1 0> are determined by X-ray diffraction. Then the ingots are sliced into a number of wafers which were finally lapped, polished, and cleaned.

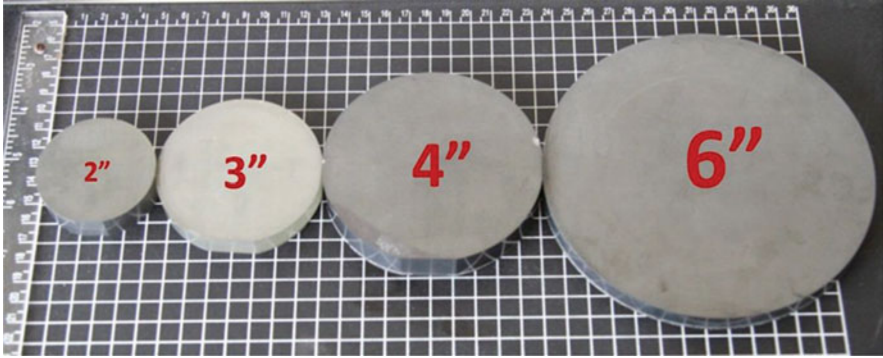


Fig. 2.47 As-grown SiC single crystal boules (Provided by Dr. Yan Peng at Shandong University)

SiC single crystal substrates are considered to be suitable for thin film growth of semiconductive GaN with wide energy bandgaps [54], because the lattice mismatch between SiC and GaN is quite small (3.5%) compared with sapphire substrates (16.1%) [55]. The quality of the deposition films is strongly dependent on the quality of substrates. Therefore, the processing of SiC wafers is extraordinarily important for film growth. However, the hardness of SiC is very closer to that of diamond, which makes it greatly difficult to process large-diameter SiC crystals. In addition, SiC substrate is very sensitive to surface defects resulting from lapping and polishing, which may propagate into an epitaxial layer and degrade device quality. Since MP achieves material removal through plastic deformation, scratches and subsurface damage layer containing dislocations are unavoidable [56]. Research on the epitaxial growth of 4H-SiC has shown that scratches are the primary contributors to polytype inclusions in the epilayers [57]. The polishing process of SiC substrates [51, 58–60] was investigated extensively. The removal mechanism of scratches in MP and physical and chemical process in CMP were analyzed. KOH etching and HRXRD were applied to evaluate the subsurface damage of SiC substrates. The effects of MP and CMP on the surface roughness were assessed. Three main procedures of SiC wafer processing were introduced. Variations of surface residual stresses during mechanical processing could be assessed by HRXRD.

SiC single crystals were grown by the sublimation method. Figure 2.47 is the image of as-grown SiC single crystals. The crystal boule was sliced into a number of wafers by diamond wires. Surface morphologies of polished wafers were observed by means of AFM and optical microscope. High-resolution X-ray diffractometer and KOH etching were used to assess the structural perfection of the wafer. Step profilometer and flatness measurement system were used to investigate the surface roughness and flatness. The SiC wafer processing includes the following steps.

2.6.1 Crystal Boule Slicing

It is very significant to slice high-quality SiC crystals into thin wafers with minimum warp, uniform thickness, and low kerf loss; otherwise it will bring great difficulty for succedent lapping and polishing. This has revitalized many interests in wire saw machining technology [58]. In general, diamond wire saw was used to slice SiC boule into wafers. The total thickness variation is less than 30 μm with warp about 20 μm for 2 in. wafers.

2.6.2 Lapping

Lapping is the second step for machining SiC in large-scale production. However, the lapping of silicon carbide is difficult because of its low fracture toughness, making it very sensitive to cracking [59]. Lapping process involves many parameters such as plate speed, pressure, grit size, abrasive density, etc. Thus, efficient lapping requires strict selection for operating parameters to maximize removal rate while controlling surface integrity.

Lapping plate is a cast-iron disk, its rotation speed is 40–70 rpm, and the applied pressure is 50–200 g/cm^2. The abrasive (B_4C) grain size is between 100 and 20 μm. The SiC material removal rate (MRR) is 5–20 μm/h owing to its high hardness and high wear resistance. MRR is increscent with the increasing of abrasive grit, density, plate speed, and pressure. However, a very high B_4C concentration is found to reduce the removal rate [60].

After lapping,the surface unflatness is 6 μm as shown in Fig. 2.48. Figure 2.49 shows the optical microscopic image of lapping surface. It can be seen that there exist lots of pits; the surface roughness R_a is about 100 nm after lapping. Due

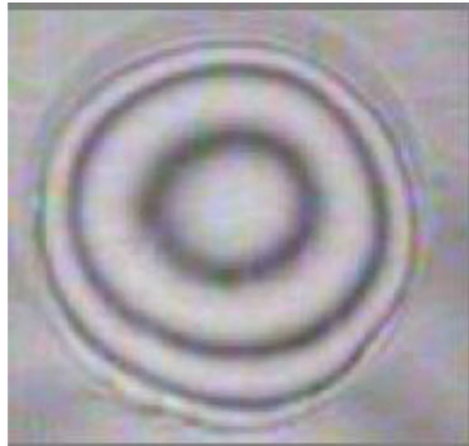


Fig. 2.48 Surface unflatness of SiC wafer after lapping (Provided by Dr. Yan Peng at Shandong University)

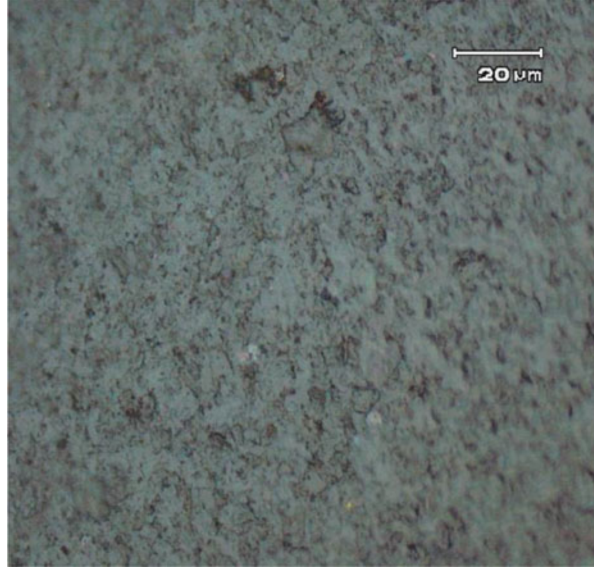


Fig. 2.49 Optical microscopic image of SiC wafer surface after lapping (Provided by Dr. Yan Peng at Shandong University)

to the great abrasive grit of lapping, it causes serious surface damage and large residual stresses. X-ray rocking curve measurement of (0 0 0 4) reflection for the wafer indicated that the full-width at the half-maximum (FWHM) is 122.4 arcs after lapping.

In the whole machining process, each step is very important for the successive processing. In order to reduce the total manufacturing time, it is preferable to obtain better ground surfaces, even if this takes longer lapping time [61].

2.6.3 Mechanical Polishing

MP is an important process aimed to remove the damaged layer caused by lapping to make a good surface and to amend the surface geometry exactly. The mechanism of SiC material removal by finer grit; harder abrasives, such as B_4C; and diamond in MP process actually includes the formation of mechanical microfractures and then the removal of these microfractures because of higher hardness of the abrasive and inherent hardness of the workmaterial [62].

The surface roughness after MP is $R_a = 3.1$ nm (measured by step profilometer). As shown in Fig. 2.50, the surface unflatness is 2 μm. Compared with surface quality after lapping, the surface unflatness decreased further after MP.

The polishing procedure was generally performed by diamond-based polishing slurries with decreasing grain size. A large number of scratches on the surface could be observed by AFM after MP. These scratches spread out in random directions with the depth in the range of 5–8 nm as shown in Fig. 2.51. This also indicates

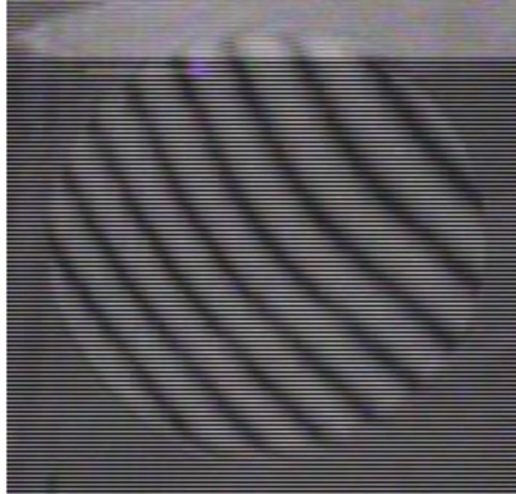


Fig. 2.50 Surface unflatness of SiC wafer after MP (Provided by Dr. Yan Peng at Shandong University)

that the material removal in MP procedure is dominant by the formation of brittle microfracture on a submicroscopic scale.

For both the mechanical lapping and polishing, subsurface damage was formed by harder abrasives. The subsurface damage has been found to extend in a depth range from one-half to one-seventy-fifth of the abrasive slurry particle size [63]. KOH etching was used to identify the subsurface damage as a part of the optimization of CMP process. Figure 2.52 displays the full-width at the half-maximum (FWHM) of (0004) reflection rocking curve of the SiC surface etched by KOH after MP with 2 μm diamond powder. It can be seen that when the etched depth reaches about 0.77 μm, the FWHM tends to keep constant. Thus, the damage depth of the surface can be considered to be about 0.77 μm.

2.6.4 Chemo-mechanical Polishing

CMP can be used to finish hard, brittle workmaterials with extremely smooth and damage-free surfaces. It depends on both chemical and mechanical effectiveness of the abrasive and the environment with respect to the workmaterial. In MP, diamond is harder than SiC; although the surface defects can be minimized by using very fine diamond particles, they cannot be completely eliminated [64]. Therefore, to produce extremely smooth and damage-free surface, further polishing process must be carried on. CMP was first demonstrated by Yasunaga et al. for polishing single crystal silicon using a soft abrasive ($BaCO_3$) [65]. Later on, this method was widely used to polish other crystal materials.

Theoretically any abrasive that can react with the workmaterial in a given environment and form a reaction product can be used for CMP [59]. For SiC CMP, the selected abrasive is SiO_2 which is much softer than SiC. The grit size of SiO_2 is 32 nm.

Fig. 2.51 AFM micrograph of the surface after MP ($5 \times 5\ \mu m^2$) (Provided by Dr. Yan Peng at Shandong University)

The wafer surface after CMP has a final surface roughness $R_a = 0.18$ nm (measured by AFM). Figure 2.53 is the AFM image of the surface finished by CMP, it reveals that the surface is extremely smooth, and there are no any scratches and other surface defects. Chemical reactions are performed between suspended silicon bonds in SiC and the alkaline (PH > 10) slurry of colloidal silica. The main chemical equation is as follows:

$$Si + 2\,NaOH + H_2O \rightarrow Na_2SiO_3 + 2\,H_2 \uparrow \qquad (2.6)$$

The reaction product Na_2SiO_3 is soluble and can be removed easily from SiC surface by subsequent mechanical action by SiO_2. Chemical reaction will continue

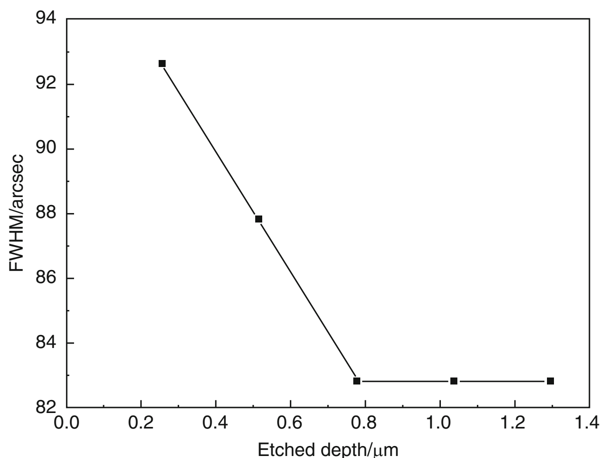


Fig. 2.52 The FWHM of (0004) reflection rocking curve of the surface etched by KOH after MP with 1 μm diamond powder (Provided by Dr. Yan Peng at Shandong University)

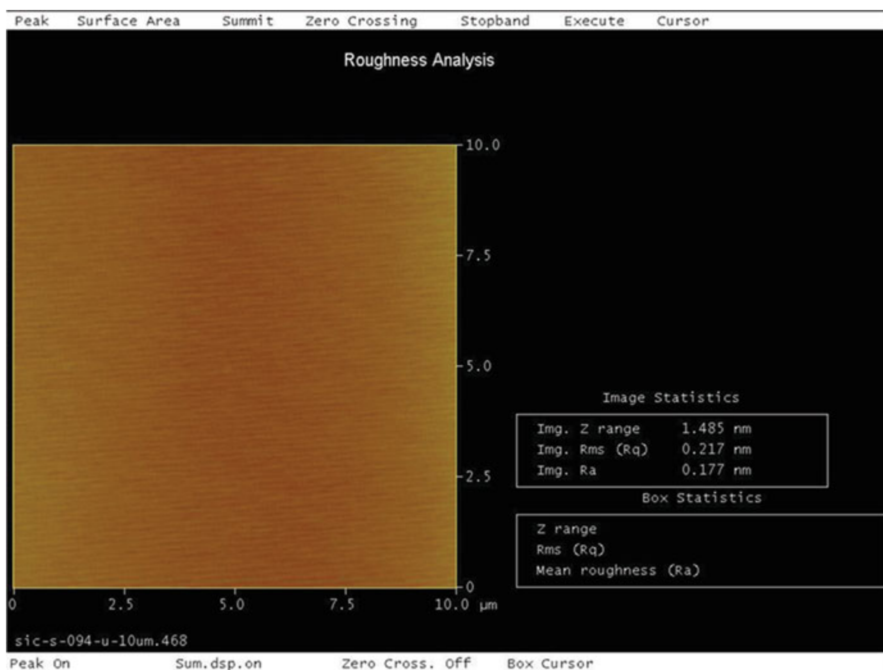


Fig. 2.53 AFM image of the SiC wafer surface finished by CMP (10 × 10 μm) (Provided by Dr. Yan Peng at Shandong University)

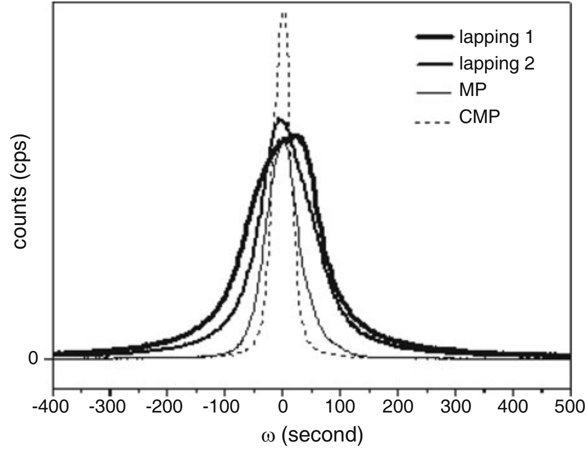


Fig. 2.54 Rocking curves of the SiC wafer surface in each machining process (Provided by Dr. Yan Peng at Shandong University)

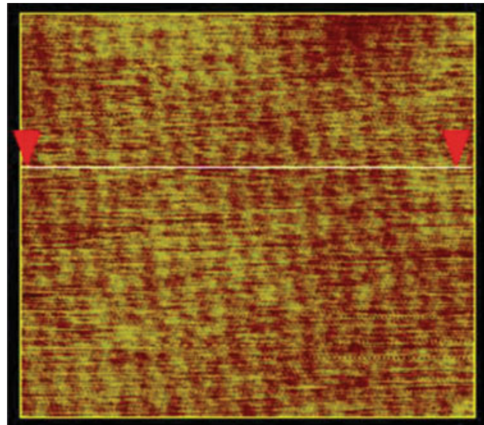


Fig. 2.55 AFM image of the CMP surface after KOH etching (Provided by Dr. Yan Peng at Shandong University)

after the passivating layers are removed [63]. Since material removal by this mechanism does not depend on the hardness but on the chemical potentials, it is possible to remove material by abrasives substantially softer than the workmaterial [63].

By HRXRD analysis shown in Fig. 2.54, the FWHM of (0004) reflection rocking curve of SiC wafer surface finished by CMP is 39.4 arcs which decreases much more than that after lapping. This indicates thin subsurface damage layer, good crystal lattice integrity, and low residual stresses in SiC wafer after CMP. From Fig. 2.54, it can be seen that FWHM falls down with each machining process. It proves that the damage layer and residual stresses have been minimized when the grain size of the abrasive decreases. The subsurface damage has been found to extend from depths ranging from one-half to one-seventy-fifth of the abrasive slurry size [64]. No scratches were visible on surfaces after KOH etching as shown in Fig. 2.55.

Three main machining processes of 2 in. SiC wafers were introduced. Slicing marks can be removed step by step by lapping and polishing. Lapping causes great residual stresses and deep damage layer which can be reduced gradually with subsequent polishing processes. Mechanical polishing produced smooth surface with a large number of scratches. These scratches can be effectively removed by CMP. After CMP, extremely smooth and low damage layer surface with roughness $R_a = 0.3$ nm was obtained. FWHM falls down with each machining process confirming that the surface damage layer and residual stresses minimize when the grain size of abrasive decreases. By the three main machining processes mentioned above, the final surface has low residual stresses and fine surface finish.

In summary, we introduce the SiC single crystal growth and substrate technologies in this chapter. It is difficult to reflect fully the status of SiC material research and development. Recently, new SiC growth technologies such as solution method and high-temperature chemical vapor deposition are well developed. However, we still hope that the contents in this chapter are helpful for SiC crystal grower and substrate processing technician.

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