Chapter 1
Introduction to Ultra-Low Power ECG Processor

1.1 Motivation

Health monitoring is becoming increasingly vital to the modern day community since life expectancy has risen and healthcare costs are increasing [1]. The death count due to cardiac problems is the highest when compared to other diseases [2]. Hence, there is a demand for low cost and reliable wearable biomedical sensors capable of monitoring patients and connecting them to their doctors before they reach critical situations. Wearable biomedical devices include heart rate sensors, ExG sensors, and blood glucose monitors. These portable devices are mobile and battery powered, which place a strict requirement on the power budget of the devices.

Electrocardiogram (ECG) is a bio-signal which represents electrical activity of the heart. It is widely applied in the medical field, due to its non-invasiveness and its capability of detecting cardiac diseases. ECG is normally recorded in the hospital or clinical centers in which the patient needs to stay in the hospital for hours or days. Portable or ECG telemetry devices have enabled patients to monitor their ECG, record ECG data, and transfer it to the hospital. The transferred data is processed in health centers for any abnormalities. Recent developments in Internet of Things (IoT) have enabled continuous healthcare monitors to partially process and transmit data. Developing IoT healthcare devices has multiple design challenges and trade-offs. The main constraint of wearable IoT sensor is energy dissipation due to the limited battery-energy. Efforts have been made to power IoT devices through energy harvesting sources [3], in which the system needs to operate at ultra-low power consumption. There is a trade-off between local processing and data transmission. Most of the raw data could be transmitted, whereas the local processing is limited to minimal function. In this scenario, complex computations are performed in mobile phones or PCs. Another option is to integrate ultra-low power accelerators and extract certain features. Thus, the transmitted data is minimized as it transmits only

T. Tekeste Habte et al., *Ultra Low Power ECG Processing System for IoT Devices*, Analog Circuits and Signal Processing,
https://doi.org/10.1007/978-3-319-97016-5_1

processed data and transmits raw data during critical situations. This configuration saves the energy dissipation from the energy-hungry transmitters.

There is huge interest in the literature on ultra-low power processors or accelerators that could be integrated into IoT healthcare devices. General-purpose processors or micro-controllers dissipate more power relative to custom designed digital signal processors, which makes them unsuitable for most ultra-low power wearable devices that target long lifetime. It is desirable to design application specific chips that meet the desired performance in energy constrained configuration.

The rest of this chapter presents the design challenges and ultra-low power techniques followed by the book contribution.

1.2 Design Challenges and Ultra-Low Power Techniques

A typical wearable ECG IoT device is shown in Fig. 1.1. It consists of electrodes (to collect the analog ECG data), analog front end (to amplify and digitize the ECG signal), digital processor (to process digitized data), power management unit (to provide and control power), and wireless transmitter (to send data to remote device) [3]. For this system to have long lifetime operation, the power budget is limited to the microwatt range. It is mandatory that the power management unit controls the power sequence for each of the modules. Since the transmitter is the most power hungry modules, it should operate for short duration depending on the design requirements. Another part which consumes substantial amount of power is the digital processor, which could be a general-purpose CPU or custom designed accelerators.

In this research work, an ECG processor which consists of all the digital circuitry is designed and implemented. The digital processor which is shown in Fig. 1.1 is contrition of this research as part of an integrated IoT ECG device. In order to realize an ultra-low power ECG processor, the design challenges are summarized into two categories: architectural choices and circuit design techniques.

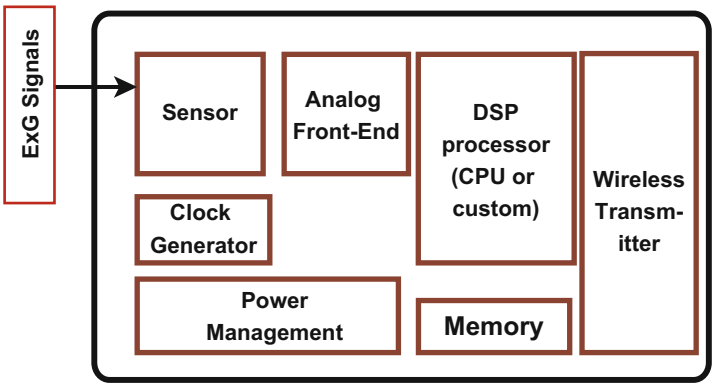

Fig. 1.1 ECG node for IoT healthcare system

The architectural choice is determined by the required application and the available power budget. The digital processor is designed in order to minimize the power consumption and energy dissipation. There are multiple ways of implementing a digital system either by utilizing a central processing unit (CPU) or by developing fully custom design. Hardware accelerators, specific to an algorithm or application, are more computationally and energy efficient. An algorithm implemented in an ASIC is more energy efficient than an algorithm implemented in a general-purpose processor or even low-power micro-controllers. Integrating a CPU along with custom accelerators provides a balance between energy efficiency and flexibility. Efforts have been made to minimize the energy consumption both at the architectural level and at the device level while attaining the desired application performance [4, 5]. ECG sensing devices have been researched and ECG signal contains wave components such as QRS complex, T-wave, and P-wave. The QRS complex is the dominant part with highest slope and magnitude. The ECG wave components (QRS complex, T-wave, and P-wave) along with their peaks and edges are termed as ECG features. Several ultra-low power ECG processing architectures were reported for application in QRS detection [6–11], full ECG feature extraction [12, 13], and ECG classification [8, 12]. Some of these architectures comprise a CPU [7] that consumes relatively higher power. Others are more energy efficient and have fully custom designs. Most of the reported QRS detection architectures are based on wavelet transform [6, 8–10]. Wavelet transform is robust in detecting QRS complex, however, its implementation requires multiscale decomposition using a cascade of filters. Others have reported QRS detection architectures based on an algorithm known as Pan and Tompkins (PAT) [11, 12]. The PAT algorithm is based on filtering, differentiation, squaring, and moving integral. All of these operations require hardware-intensive computations. Wavelet transform using multiscale decomposition has been applied also for full ECG feature extraction [13]. Time domain signal analysis is applied [12] for full feature extraction. The challenge in QRS detection or ECG feature extraction is to attain the desired performance at the lowest possible power consumption. That is why appropriate architectural choice is necessary.

Circuit design techniques that minimize the energy consumption are widely explored and implemented in current state-of-the-art portable medical devices. These techniques include voltage scaling, voltage islands, power gating, clock gating, and the use of deeply scaled nodes.

The total power consumption in an ultra-low power digital system can be represented by Eq. (1.1). According to this expression, the factors that affect the total power consumption are:

$$P_{Total} = \sum (\alpha_i \times C_i) \times f \times V^2 + \beta \times I_{leakage} \times V \tag{1.1}$$

- C_i: load capacitance
- V: supply voltage

- f: operating frequency
- α_i: switching activity factor
- β: leakage factor

Each of the above factors could be reduced to minimize the total power consumption. Firstly, the load capacitance depends on the technology, and it could not be altered as long as the same standard cell library is used. Secondly, scaling the supply voltage will reduce the power. The dynamic power is minimized quadratically and the leakage power is minimized exponentially with the supply voltage. It is an effective technique; although, there are constraints to limit the supply voltage. These constraints are the minimum operating voltage of SRAM and the timing requirement of the design. Thirdly, the operating frequency must be optimized and is determined by the architecture of the system. Thus, choosing an optimum frequency would enable further reduction in power consumption. Reducing the operating frequency will reduce the dynamic power as represented in Eq. (1.1). Fourthly, the switching activity factor depends on the architecture, and it could be altered by applying clock gating. Certain blocks could be clock gated whenever they are not used. Hence, applying a combination of the above techniques would enable the system to achieve the minimum average power consumption and henceforth the lowest energy consumption. Lastly, the leakage factor could be reduced by utilizing low-leakage standard cell library. Certain parts of the design could be power gated in case they are not used at certain time slots, as power gating reduces the leakage.

The digital processor could be powered from energy harvesting devices or battery. In recent developments, energy harvesting circuits were capable of powering full SoC that includes analog front end, digital processor, and a transmitter [14]. It is necessary that the power consumption remains within the power limit of the energy harvester. If the system is operating at its lowest energy dissipation, it would have a long lifetime. Hence, the proposed approaches would investigate achieving lowest possible power consumption and minimum energy dissipation.

1.3 Book Contribution and Organization

The main objective of this research work was to design an ultra-low power ECG processor for IoT healthcare devices. Ultra-low power operation was achieved through novel architectural choices and ultra-low power circuit design techniques. In this book, two chips were fabricated and tested. The fabricated chips process ECG signals in order to extract features and classify ECG beats for cardiac autonomic neuropathy (CAN) severity. Moreover, an improved architecture for ventricular arrhythmia (VA) prediction is proposed. The designed chips were purely digital circuits operating in the nano-watt range. The main system components are shown in Fig. 1.2 and include ECG processing accelerators to extract and classify ECG beats, custom designed control FSM that controls the overall chip functions, memory to store temporary data, and digital interface for external communication. Full-custom design techniques resulted in a much lower power dissipation than did the incorporation of a general-purpose processing unit.

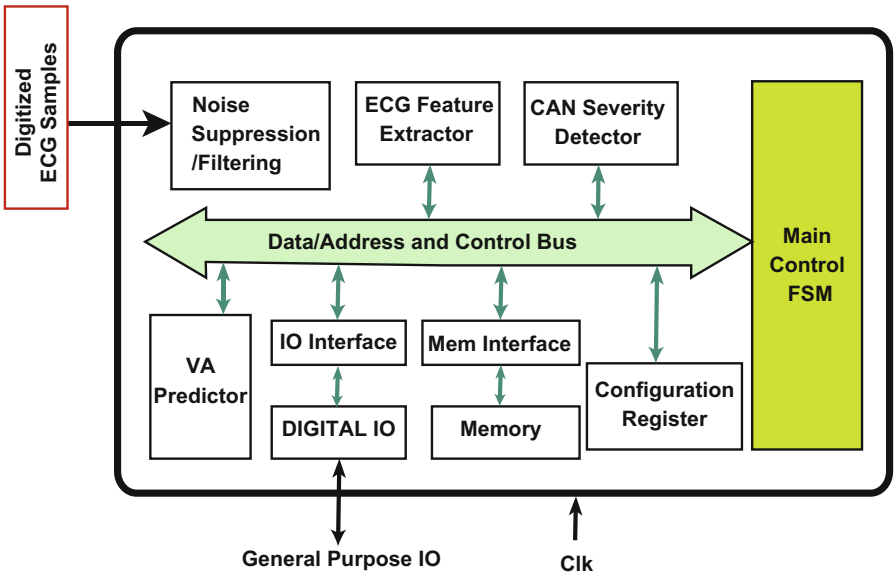

Fig. 1.2 Integrated biomedical processing platform

The contributions of the book work could be summarized as follows.

1. Combined CLT and DWT-based ECG processor (Chap. 3)
   - A combination of CLT and DWT architectures for full ECG feature extraction, where each technique is chosen for its advantages in reducing hardware resources without affecting the desired performance.
   - Developed a pipelined architecture for CLT which reduces the required resource by 32× when compared to conventional straightforward implementation of CLT.
   - Designed and implemented ultra-low power techniques such as clock gating and voltage scaling. Through such techniques, the fabricated chip consumed only 642 nW at 0.6 V and at a frequency of 7.5 kHz.
2. Ultra-low power QRS detection architecture (Chap. 4)
   - An ultra-low power QRS detection architecture was designed that is capable of detecting QRS at sensitivity and predictivity of 99.37% and 99.38%, respectively.
   - Absolute Value Curve Length Transform was proposed, where the required hardware resources are minimized.
   - Synthesized QRS detection system consumed 6.5 nW when operated at 1 V and at 250 Hz.
   - A lossless compression architecture that enabled reduced transmitted data for IoT transmitters was implemented.

3. Ultra-low power CAN detection and VA prediction architecture (Chap. 5)

   - On-chip full ECG feature extraction that utilizes ACLT for QRS detection and low-pass differentiation for other ECG features was implemented.
   - Real-time classification of CAN severity is enabled through on-chip classification of CAN severity.
   - Fabricated chip that extracts full ECG features and detects CAN severity that consumed only 75 nW at 0.6 V.
   - Improved hardware architecture for VA prediction is presented, which achieves a reduction in the required area by 16.0% and in power consumption by 62.2%.

1.3.1 Book Organization

The remainder of this book is organized as follows. Chapter 2 discusses background about ECG processing algorithms and biomedical sensing platforms. Chapter 2 presents existing algorithms, their drawbacks, and analysis. Chapter 3 presents an ECG feature extraction SoC based on combined curve length transform and discrete wavelet transform. Chapter 3 discusses the merits of each of these transforms in ECG processing. Moreover, it presents ultra-low power techniques along with the measured results. In Chap. 4, an energy efficient QRS detection architecture along with a compression architecture is proposed. Chapter 5 discusses an ECG processor aimed at CAN detection. The SoC performs full ECG extraction and on-chip CAN detection. Measured results are presented along with comparison with literature. Chapter 6 concludes the book.